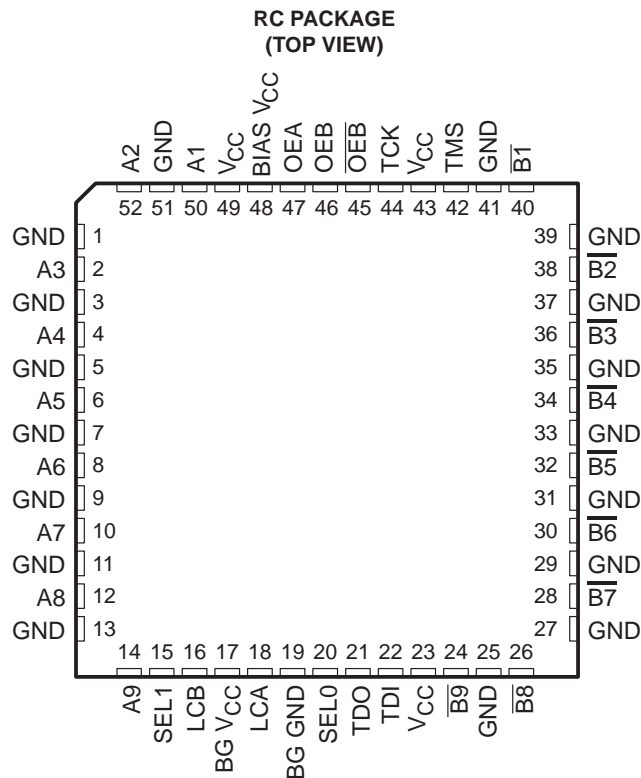


# SN74FB2031 9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

SCBS176K – NOVEMBER 1991 – REVISED SEPTEMBER 1999

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL)  $\bar{B}$  Port**
- **Open-Collector  $\bar{B}$ -Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **High-Impedance State During Power Up and Power Down**
- **BIAS  $V_{CC}$  Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **$\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**
- **Packaged in Plastic Quad Flatpack**



## description

The SN74FB2031 device is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. It is specifically designed to be compatible with IEEE Std 1194.1-1991.

The  $\bar{B}$  port operates at BTL-signal levels. The open-collector  $\bar{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\bar{OEB}$ ) are provided for the  $\bar{B}$  outputs. When OEB is low,  $\bar{OEB}$  is high, or  $V_{CC}$  is less than 2.1 V, the  $\bar{B}$  port is turned off.

The A port operates at TTL signal levels. The A outputs reflect the inverse of the data at the  $\bar{B}$  port when the A-port output enable (OEA) is high. When OEA is low or  $V_{CC}$  is less than 2.1 V, the A outputs are in the high-impedance state.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
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### description (continued)

Pins are allocated for the 4-wire IEEE Std 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

BG  $V_{CC}$  and BG GND are the supply inputs for the bias generator.

The SN74FB2031 is characterized for operation from 0°C to 70°C.

### Function Tables

#### TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

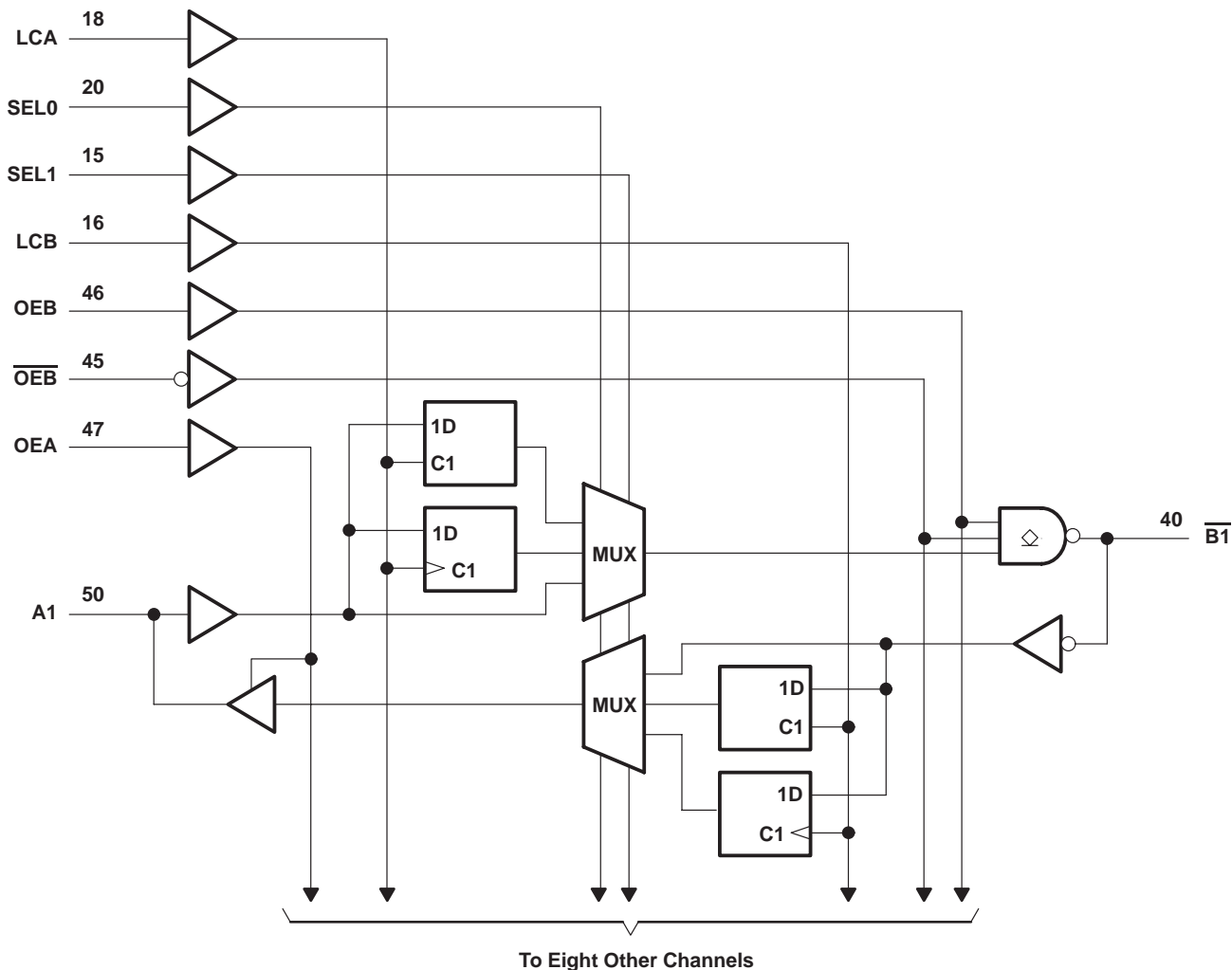
#### STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

#### SELECT

SEL1	SEL0	MUX A→B	MUX B→A
0	0	Latch	Latch
0	1	Through	Through
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ : Except $\overline{B}$ port .....	-1.2 V to 7 V
$\overline{B}$ port .....	-1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, $V_O$ .....	-0.5 V to 3.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ : Except $\overline{B}$ port .....	-40 mA
$\overline{B}$ port .....	-18 mA
Current applied to any single output in the low state, $I_O$ : A port .....	48 mA
$\overline{B}$ port .....	200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1) .....	44°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

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### recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
$V_{CC}$ , BIAS $V_{CC}$ , BG $V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$\bar{B}$ port	1.62	2.3	V
		Except $\bar{B}$ port	2		
$V_{IL}$	Low-level input voltage	$\bar{B}$ port	0.75	1.47	V
		Except $\bar{B}$ port		0.8	
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current	A port		24	mA
		$\bar{B}$ port		100	
$T_A$	Operating free-air temperature	0		70	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$\bar{B}$ port	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
	Except $\bar{B}$ port	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -40\text{ mA}$			-0.5	
$V_{OH}$	A port	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$				V
			$I_{OH} = -3\text{ mA}$	2.5	3.3		
$V_{OL}$	A port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 20\text{ mA}$				V
			$I_{OL} = 24\text{ mA}$		0.35	0.5	
	$\bar{B}$ port	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 80\text{ mA}$	0.75		1.1	
			$I_{OL} = 100\text{ mA}$			1.15	
$I_I$	Except $\bar{B}$ port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			50	$\mu\text{A}$
$I_{IH}^\ddagger$	Except $\bar{B}$ port	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{IL}^\ddagger$	Except $\bar{B}$ port	$V_{CC} = 5.5\text{ V}$	$V_I = 0.5\text{ V}$			-50	$\mu\text{A}$
	$\bar{B}$ port		$V_I = 0.75\text{ V}$			-100	
$I_{OZH}$	A port	$V_{CC} = 2.1\text{ V to } 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZL}$	A port	$V_{CC} = 2.1\text{ V to } 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50	$\mu\text{A}$
$I_{OZPU}$	A port	$V_{CC} = 0\text{ to } 2.1\text{ V}$ ,	$V_O = 0.5\text{ V to } 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZPD}$	A port	$V_{CC} = 2.1\text{ V to } 0$ ,	$V_O = 0.5\text{ V to } 2.7\text{ V}$			-50	$\mu\text{A}$
$I_{OH}$	$\bar{B}$ port	$V_{CC} = 0\text{ to } 5.5\text{ V}$ ,	$V_O = 2.1\text{ V}$			100	$\mu\text{A}$
$I_{OS}^\S$	A port	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-30		-150	mA
$I_{CC}$	A port to $\bar{B}$ port	$V_{CC} = 5.5\text{ V}$ ,	$I_O = 0$			78	mA
	$\bar{B}$ port to A port					78	
$C_i$		$V_I = 0.5\text{ V or } 2.5\text{ V}$			4.5		pF
$C_{io}$	A port	$V_O = 0.5\text{ V or } 2.5\text{ V}$			8.5		pF
	$\bar{B}$ port per IEEE Std 1194.1-1991	$V_{CC} = 0\text{ to } 5.5\text{ V}$				6	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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## live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 4.5 V	$V_B = 0$ to 2 V,	$V_I$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V	450		$\mu A$
	$V_{CC} = 4.5$ V to 5.5 V			10		
$V_O$	$\bar{B}$ port	$V_{CC} = 0,$	$V_I$ (BIAS $V_{CC}$ ) = 5 V	1.62	2.1	V
$I_O$	$\bar{B}$ port	$V_{CC} = 0,$	$V_B = 1$ V,	$V_I$ (BIAS $V_{CC}$ ) = 4.5 V to 5.5 V		$\mu A$
		$V_{CC} = 0$ to 5.5 V,	OEB = 0 to 0.8 V	100		
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V	100		

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				MIN	MAX	UNIT
$f_{clock}$	Clock frequency			150		MHz
$t_w$	Pulse duration		LCA or LCB	3.3		ns
$t_{su}$	Setup time	Clock mode	Data before LCA $\uparrow$	1.4		ns
			Data before LCB $\uparrow$	2.8		
		Latch mode	Data before LCA $\uparrow$	1.1		
			Data before LCB $\uparrow$	2.4		
$t_h$	Hold time	Clock mode	Data after LCA $\uparrow$	0.6		ns
			Data after LCB $\uparrow$	0		
		Latch mode	Data after LCA $\uparrow$	0.9		
			Data after LCB $\uparrow$	0		



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## 9-BIT TTL/BTL ADDRESS/DATA TRANSCEIVER

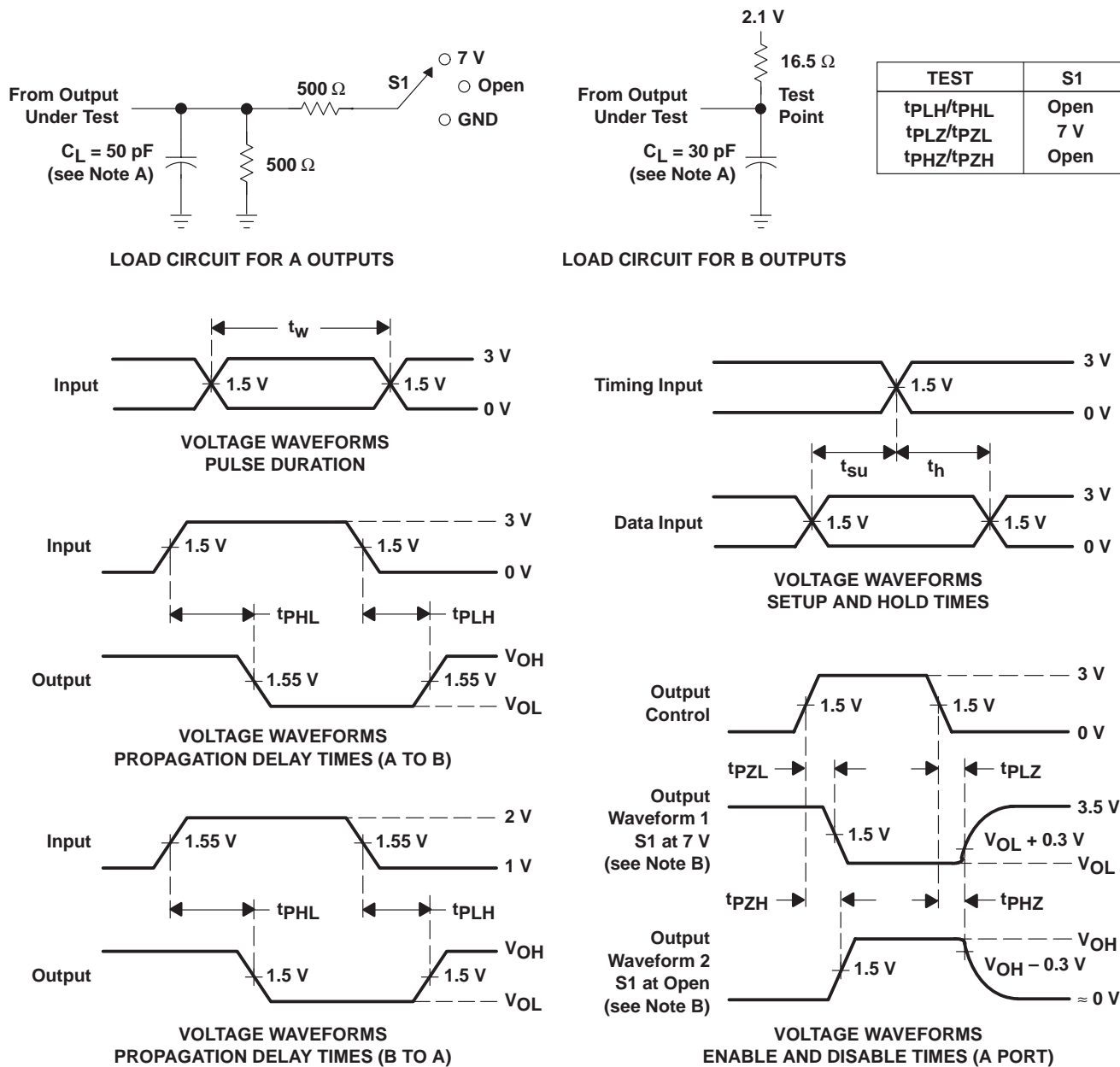
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			150			150		MHz
t <sub>PLH</sub>	A (through mode)	$\bar{B}$	3.7	4.5	5.9	3.2	6.6	ns
t <sub>PHL</sub>			2.9	4	5.7	2.6	5.9	
t <sub>PLH</sub>	A (transparent)	$\bar{B}$	4.1	5	6.5	3.6	7.3	ns
t <sub>PHL</sub>			3.3	4.5	6.1	3	6.5	
t <sub>PLH</sub>	LCA	$\bar{B}$	4.5	5.4	7	3.9	7.8	ns
t <sub>PHL</sub>			4	5.1	6.7	3.4	7.4	
t <sub>PLH</sub>	LCB	A	2.8	3.7	4.7	1.9	6	ns
t <sub>PHL</sub>			2.5	3.4	4.9	1.8	5.5	
t <sub>PLH</sub>	SEL1 or SEL0	A	2.5	3.8	5.3	1.9	6.3	ns
t <sub>PHL</sub>			2.2	3.5	5.1	1.6	5.6	
t <sub>PLH</sub>	SEL1 or SEL0	$\bar{B}$	4.1	5.3	6.9	3.7	7.8	ns
t <sub>PHL</sub>			3.7	5.2	6.9	3.3	7.7	
t <sub>PLH</sub>	$\bar{B}$ (through mode)	A	3.1	4	5.6	2.2	7.1	ns
t <sub>PHL</sub>			2.6	3.4	4.9	1.4	5.7	
t <sub>PLH</sub>	$\bar{B}$ (transparent)	A	3.3	4.2	5.9	2.4	7.6	ns
t <sub>PHL</sub>			2.8	3.9	5.5	1.8	6.3	
t <sub>PLH</sub>	OEB or $\overline{OEB}$	$\bar{B}$	3.7	4.6	6.1	3.2	6.7	ns
t <sub>PHL</sub>			2.9	4.3	5.8	2.5	6.4	
t <sub>PZH</sub>	OEA	A	2.3	3.1	4.5	1.6	5	ns
t <sub>PZL</sub>			1.9	2.7	4.1	1.6	4.4	
t <sub>PHZ</sub>	OEA	A	2.2	3.1	4.5	1.5	5.2	ns
t <sub>PLZ</sub>			2.5	3.3	4.9	2	5.2	
t <sub>sk(p)</sub>	Pulse skew	A	$\bar{B}$			0.5		ns
		$\bar{B}$	A			0.3		
t <sub>sk(o)</sub>	Pulse skew	A	$\bar{B}$			0.2		ns
		$\bar{B}$	A			0.3		
t <sub>t</sub>	Transition time, $\bar{B}$ outputs (1.3 V to 1.8 V)		0.6	2	2.8	0.4	2.9	ns
	Transition time, $\bar{A}$ outputs (10% to 90%)		0.5	3.5	4.7	0	5.4	
$\bar{B}$ -port input pulse rejection			1			1		ns



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ ; BTL inputs: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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