DESCRIPTION

The A24C32 provides 32768 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 4096 bytes.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The A24C32 is available in SOP8, TSSOP8, DFN8, DIP8, SOT-25 and TSOT-25 packages.

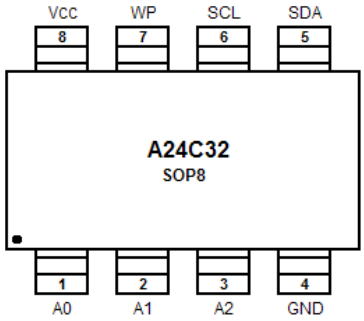
ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ: 2,500pcs/Reel SPQ: 100pcs/Tube	M8	A24C32M8R-Z
		A24C32M8U-Z
		A24C32M8VR-Z
		A24C32M8VU-Z
TSSOP8 SPQ: 3,000pcs/Reel SPQ: 100pcs/Tube	TMX8	A24C32TMX8R-Z
		A24C32TMX8U-Z
		A24C32TMX8VR-Z
		A24C32TMX8VU-Z
DFN8 SPQ: 3,000pcs/Reel	J8	A24C32J8R-Z
		A24C32J8VR-Z
DIP8 SPQ: 50pcs/Tube	P8	A24C32P8U-Z
		A24C32P8VU-Z
SOT-25 SPQ: 3,000pcs/Reel	E5	A24C32E5R-Z
		A24C32E5VR-Z
TSOT-25 SPQ: 3,000pcs/Reel	TE5	A24C32TE5R-Z
		A24C32TE5VR-Z
Note	Z: Temperature: A : -40℃ to +85℃ B : -40℃ to +105℃ C : -40℃ to +125℃ V: Halogen free Package R: Tape & Reel U: Tube	
AiT provides all RoHS products		

FEATURES

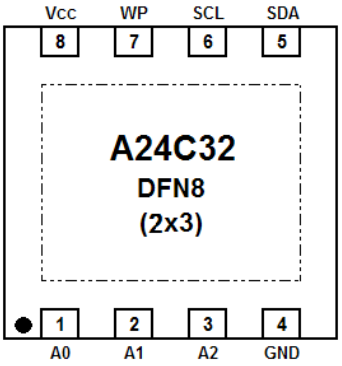
- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  32 Kbits (4Kbytes) of EEPROM
  Page size: 32 bytes
- Extended Temperature Range
  A : -40℃ to +85℃
  B : -40℃ to +105℃
  C : -40℃ to +125℃
- Single supply voltage and high speed:
  1.7V-5.5V/400kHz
  2.5V-5.5V/1MHz
  Random and sequential Read modes
- Write:
  Byte Write within 3 ms
  Page Write within 3 ms
  Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-reliability
  Endurance: 1 Million Write Cycles
  Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  HBM 5000V
- Available in SOP8, TSSOP8, DFN8, DIP8, SOT-25 and TSOT-25 packages

PIN DESCIPTION

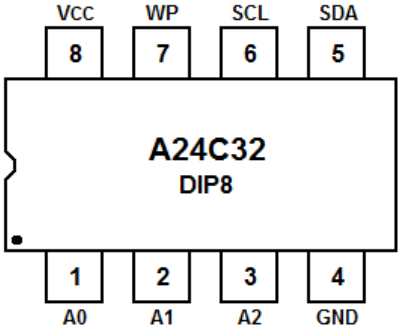


Top View

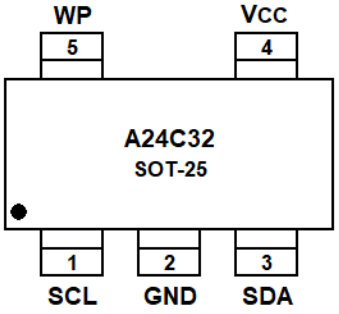
Top View



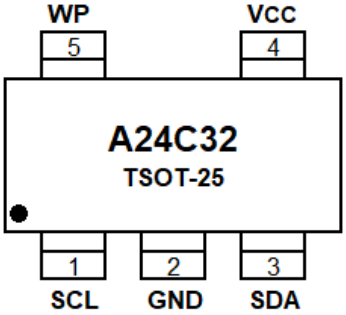
Top View



Top View



Top View



Top View

Pin #						Symbol	Type	Functions
SOP8	TSSOP8	DFN8	DIP8	SOT-25	TSOT-25			
1	1	1	1	-	-	A0	I	Address Inputs
2	2	2	2	-	-	A1	I	Address Inputs
3	3	3	3	-	-	A2	I	Address Inputs
4	4	4	4	2	2	GND	P	Ground
5	5	5	5	3	3	SDA	I/O	Serial Data
6	6	6	6	1	1	SCL	I	Serial Clock Input
7	7	7	7	5	5	WP	I	Write Protect
8	8	8	8	4	4	V_{CC}	P	Power Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input / Output Voltage	GND-0.3V ~ V_{CC} +0.3V
Operating Ambient Temperature	-40℃~ +85℃
Storage Temperature	-65℃ ~ +150℃
Electrostatic Pulse (Human Body Model)	5000V

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

Applicable over recommended operating range form, T_A = 25℃, f = 1.0MHz, V_{CC} = +1.7V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input / Output Capacitance (SDA)	$C_{I/O}$	V_{IO}=0V	-	-	8	pF
Input Capacitance (A0, A1, A2, SCL)	C_{IN}	V_{IN}=0V	-	-	6	pF

AC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range form, unless otherwise noted

A24C32-A	T_A = -40℃ to +85℃	V_{CC} = +1.7V to +5.5V@400kHz
A24C32-B	T_A = -40℃ to +105℃	V_{CC} = +2.5V to +5.5V@1MHz
A24C32-C	T_A = -40℃ to +125℃	C_L= 100pF

Parameter	Symbol	1.7V≤V_{CC}<2.5V			2.5V≤V_{CC}<5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	f_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.3	-	-	0.5	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.26	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t_{AA}	-	-	0.9	-	-	0.45	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.3	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD.STA}$	0.6	-	-	0.25	-	-	μs
Start Setup Time	$t_{SU.STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	-	100	-	-	ns
Input Rise Time[NOTE1]	t_R	-	-	0.3	-	-	0.12	μs
Input Fall Time[NOTE1]	t_F	-	-	0.3	-	-	0.12	μs
Stop Setup Time	$t_{SU.STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	1.9	3	-	1.9	3	ms
5.0V, 25℃, Byte Mode[NOTE1]	Endurance	1M	-	-	1M	-	-	Write Cycle

DC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range form, unless otherwise noted

A24C32-A	T_A = -40℃ to +85℃	V_{CC} = +1.7V to +5.5V@400kHz
A24C32-B	T_A = -40℃ to +105℃	V_{CC} = +2.5V to +5.5V@1MHz
A24C32-C	T_A = -40℃ to +125℃	C_L= 100pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	@400kHz	1.7	-	5.5	V
		@1MHz	2.5	-	5.5	V
Supply Current V_{CC} = 5.0V	I_{CC}	Read at 400kHz	-	0.14	0.3	mA
		Write at 400kHz	-	0.28	0.5	mA
Supply Current V_{CC} = 5.0V	I_{SB1}	V_{IN} = V_{CC} or V_{SS}	-	0.03	0.5	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or V_{SS}	-	0.10	1.0	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or V_{SS}	-	0.05	1.0	μA
Input Low Level	V_{IL1}	V_{CC} = 1.7V to 5.5V	-0.3	-	V_{CC}x0.3	V
Input High Level	V_{IH1}	V_{CC} = 1.7V to 5.5V	V_{CC}x0.7	-	V_{CC}+0.3	V
Output Low Level V_{CC} = 1.7V	V_{OL1}	I_{OL} = 0.15mA	-	-	0.2	V
Output Low Level V_{CC} = 5.0V	V_{OL2}	I_{OL} = 3.0mA	-	-	0.4	V

NOTE1: This parameter is characterized and is not 100% tested.

NOTE2: AC measurement conditions: R_L(connects to V_{CC}): 1.3k

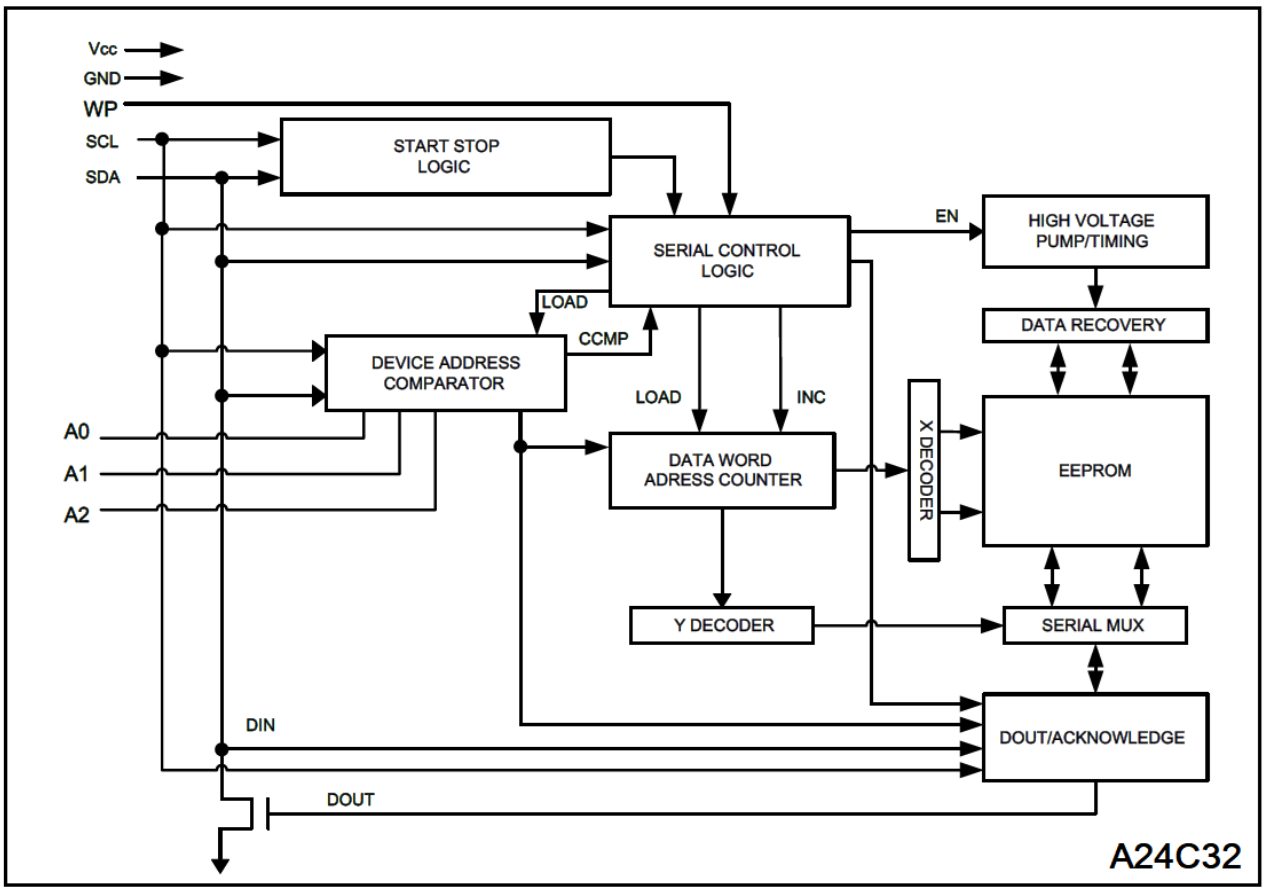
Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}

Input rise and fall time: 50ns

Input and output timing reference voltages: 0.5V_{CC}

The value of RL should be concerned according to the actual loading on the user's system.

BLOCK DIAGRAM



DETAILED INFORMATION

DEVICE/PAGE ADDRESSES (A2 , A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the A24C32. Eight 32k devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-OR'ed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The A24C32 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following Table 1.

Table1: Write Protect

WP Pin Status	A24C32
At V_{CC}	Full (32k) Array
At GND	Normal Read/Write Operations

FUNCTIONAL DESCRIPTION

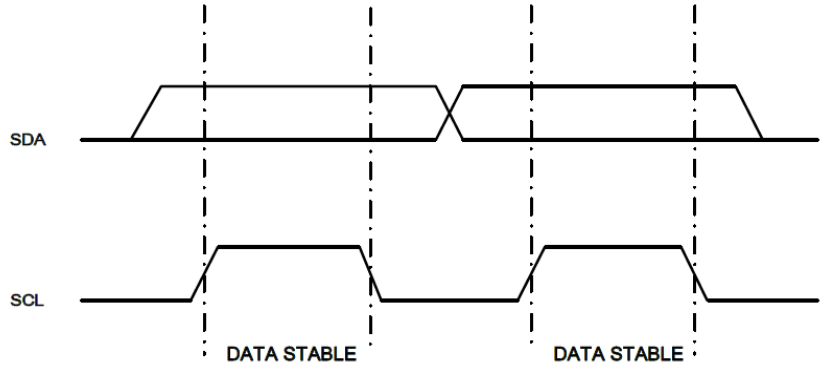
1. Memory Organization

A24C32 , 32k SERIAL EEPROM: Internally organized with 128 pages of 32 bytes each, the 32k requires a 12-bit data word address for random word addressing.

2. Device Operation

CLOCK AND DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin can change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

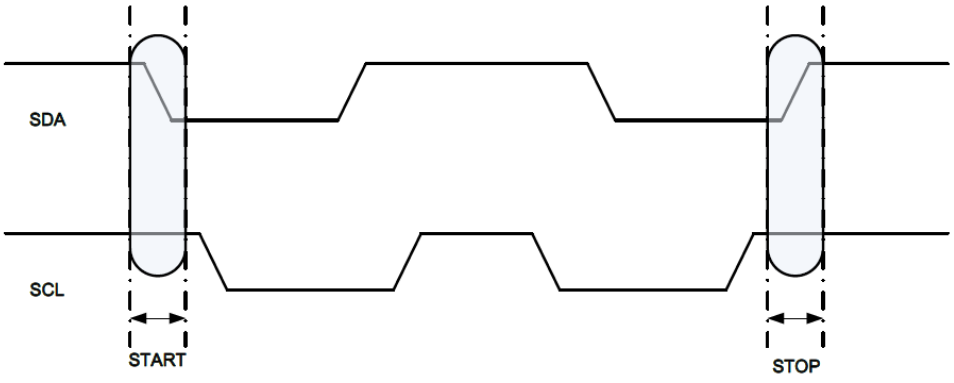
Figure 1 Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

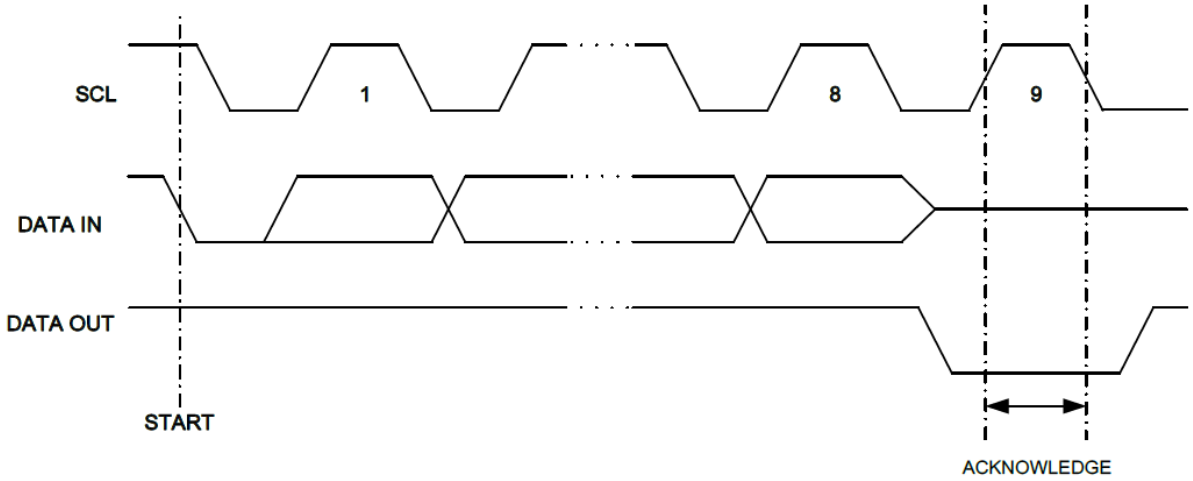
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. (see Figure 2).

Figure 2 Start and Stop Definition



ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3 Output Acknowledge



STANDBY MODE: The A24C32 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

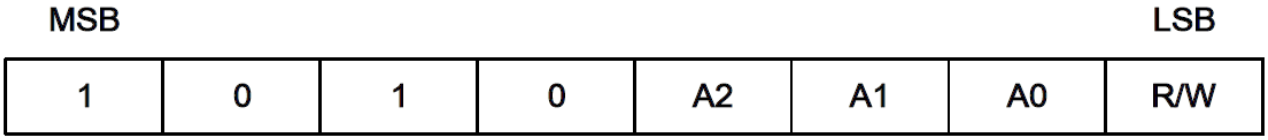
MEMORY RESET: After the protocol is interrupted, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

3. Device Addressing

The 32k EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4).

Figure 4 Device Address



The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 32k EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to standby state.

DATA SECURITY: The A24C32 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address (see Table 2 & Table 3) following the device address word and acknowledgment. Upon receipt of every 8-bit address, the EEPROM will respond with a "0" and then send 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the master device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, in order to save the data in the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

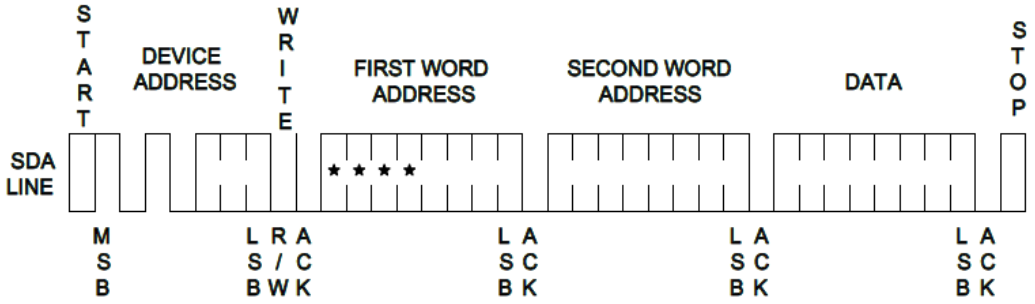
Table 2 First Word Address

B15	B14	B13	B12	B11	B10	B9	B8

Table 3 Second Word Address

B7	B6	B5	B4	B3	B2	B1	B0

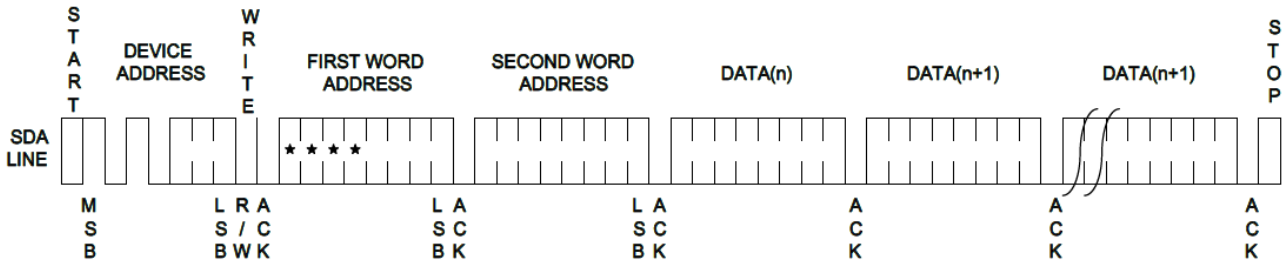
Figure 5 Byte Write



Note.1*=DON'T CARE bits

PAGE WRITE: The Page Write mode allows up to 32 bytes to be written in a single Write cycle. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

Figure 6 Page Write



Note.1*=DON'T CARE bits

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

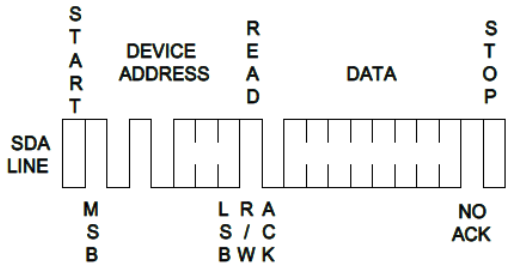
ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read and sequential read.

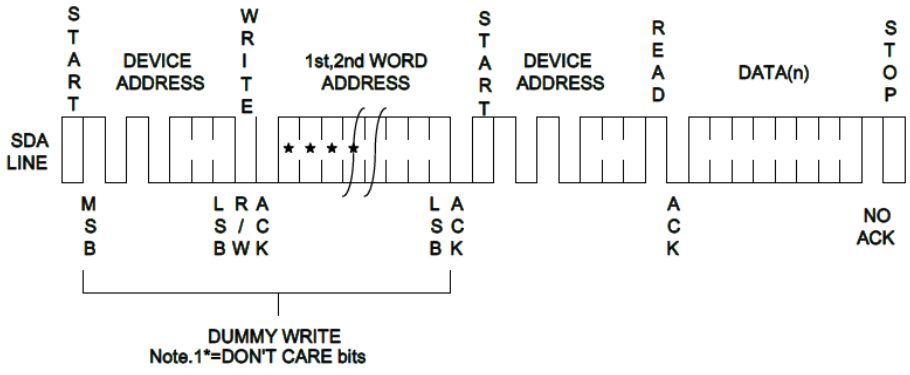
CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (see Figure 7).

Figure 7 Current Address Read



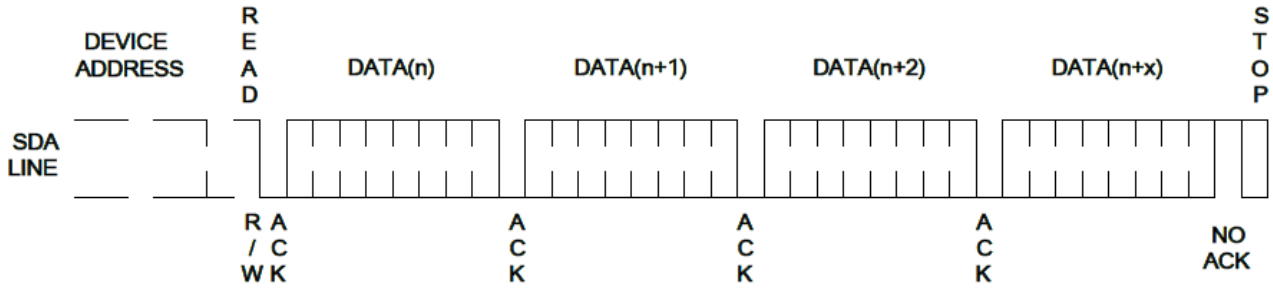
RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).

Figure 8 Random Read



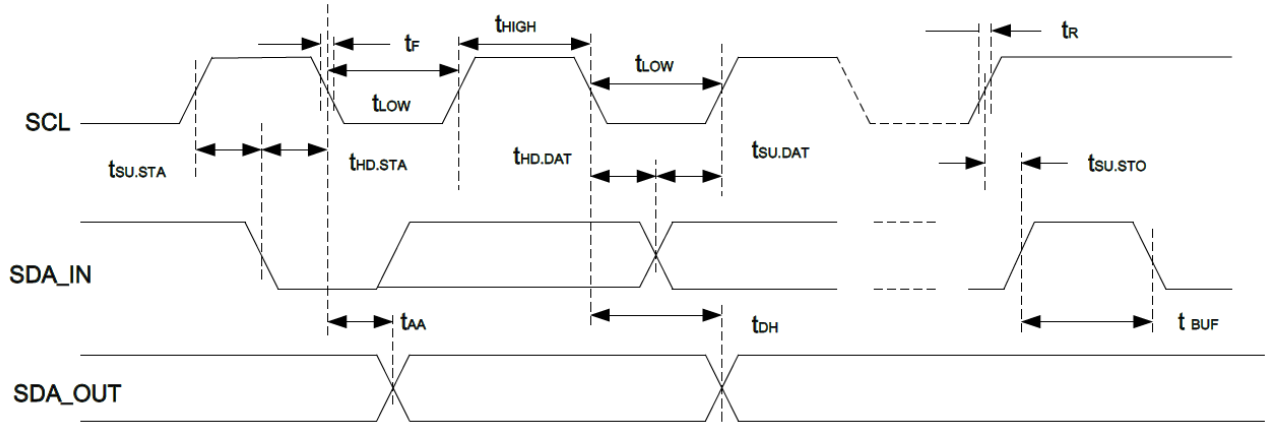
SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9)

Figure 9 Sequential Read



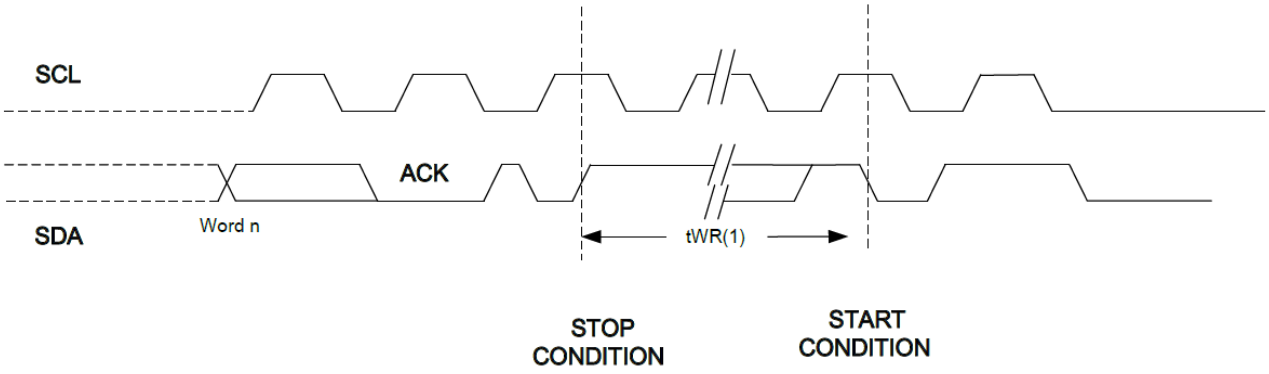
BUS TIMING

Figure 10 SCL: Serial Clock, SDA: Serial Data I/O



WRITE CYCLE TIMING

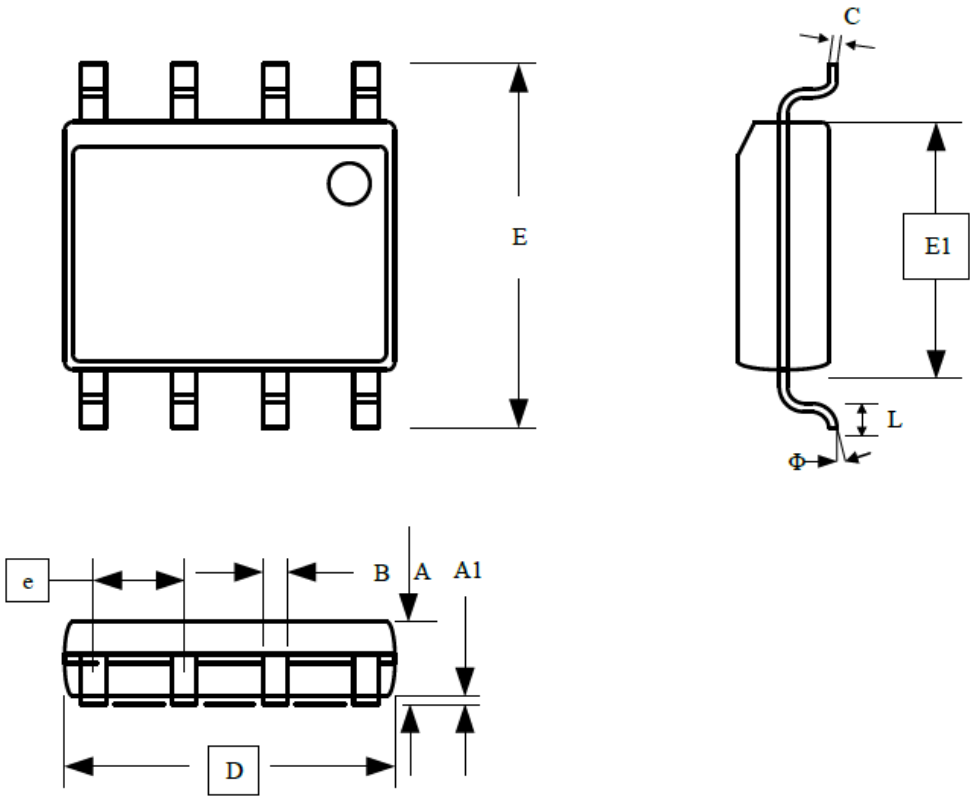
Figure 11 SCL: Serial Clock, SDA: Serial Data I/O



NOTE: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

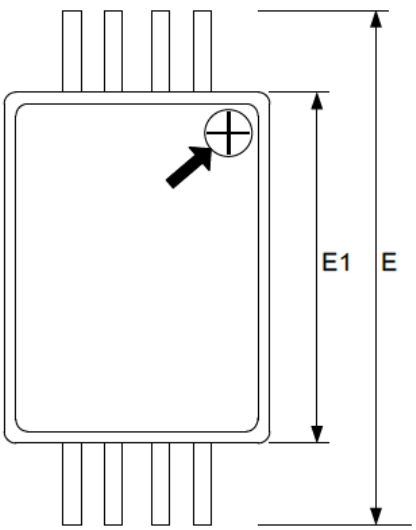
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)

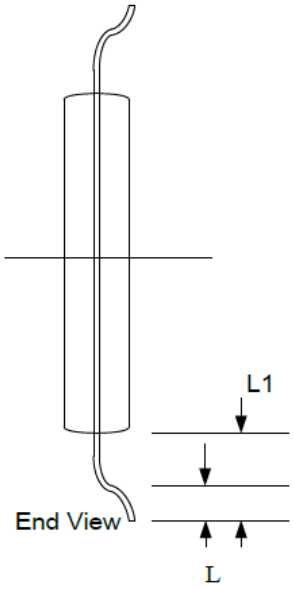


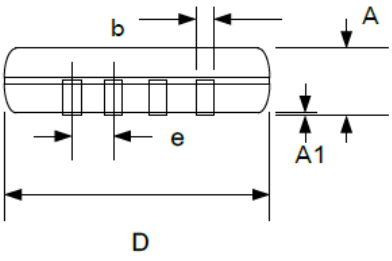
Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.23
B	0.39	0.48
C	0.21	0.26
D	4.70	5.10
E1	3.70	4.10
E	5.80	6.20
e	1.27 BSC	
L	0.50	0.80
θ	0°	8°

Dimension in TSSOP8 Package (Unit: mm)



Top View

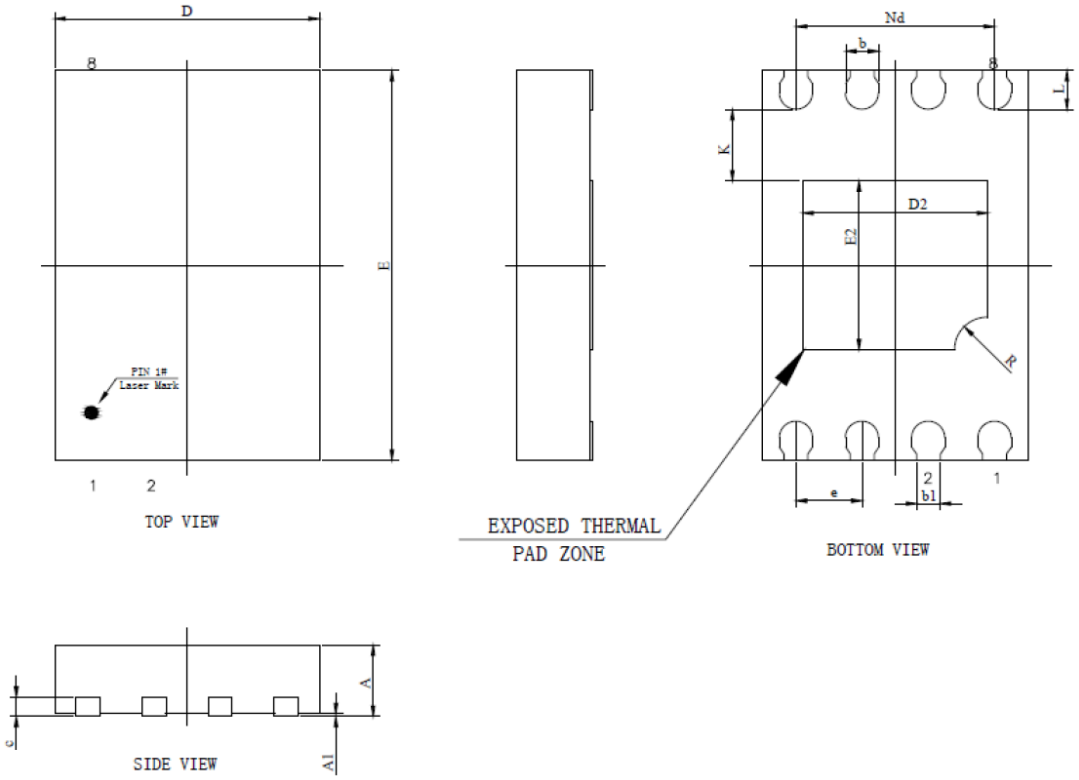




Side View

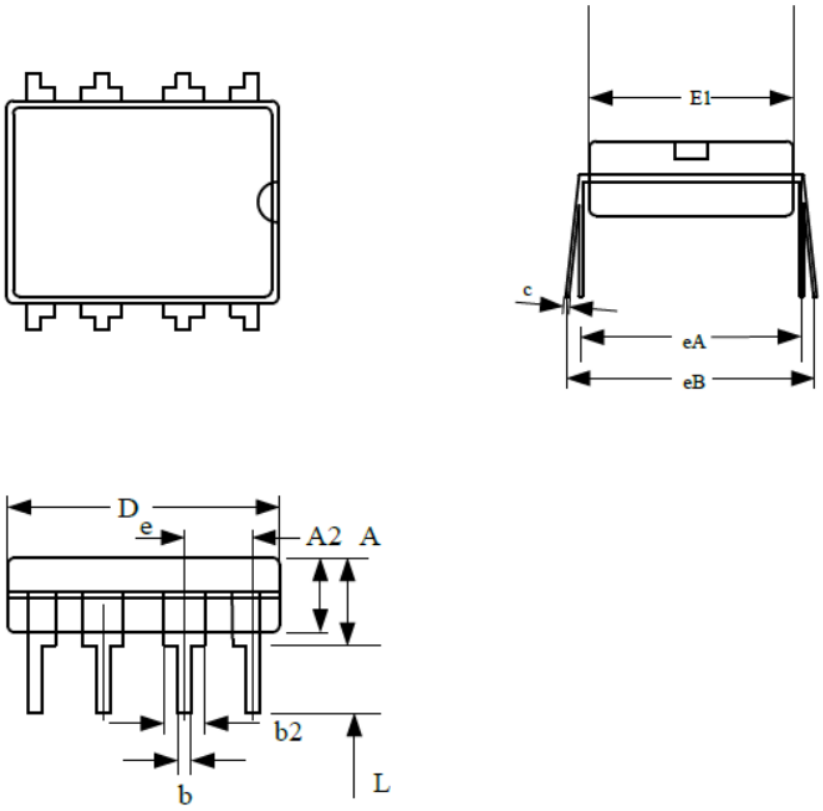
Symbol	Min	Max
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
A	-	1.20
A1	0.05	0.15
b	0.21	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	

Dimension in DFN8 (Unit: mm)



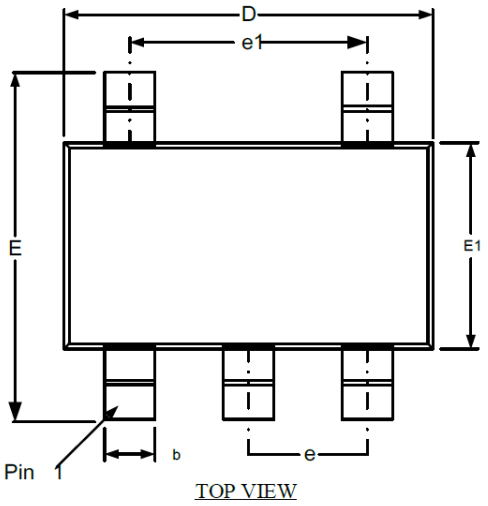
Symbol	Min	Max
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
b1	0.18 REF	
c	0.152 REF	
D	1.90	2.10
D2	1.30	1.50
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.20	1.40
L	0.25	0.35
R	0.20	0.30
K	0.55 REF	

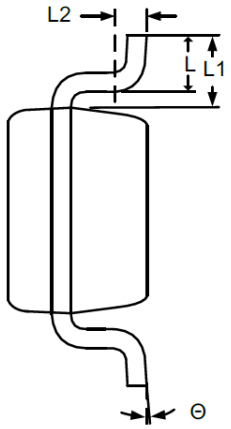
Dimension in DIP8 (Unit: mm)

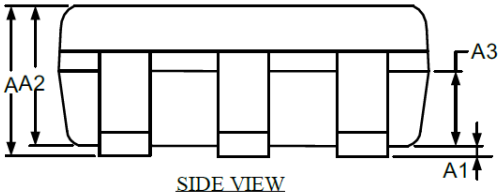


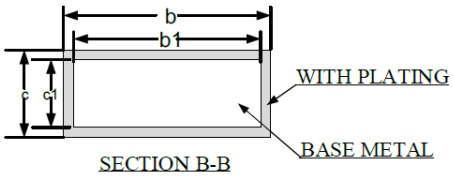
Symbol	Min	Max
A	3.60	4.00
A2	3.20	3.40
b	0.44	0.53
b2	1.52 BSC	
c	0.24	0.32
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.30
L	3.00 BSC	

Dimension in SOT-25 (Unit: mm)



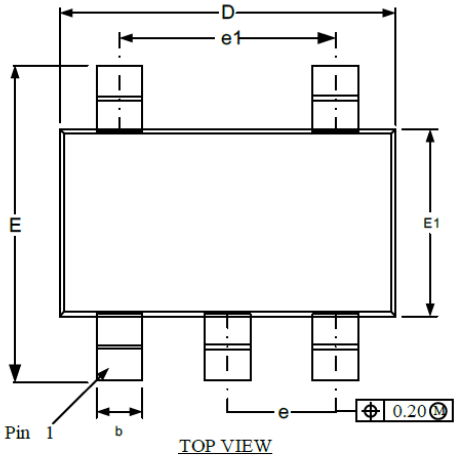


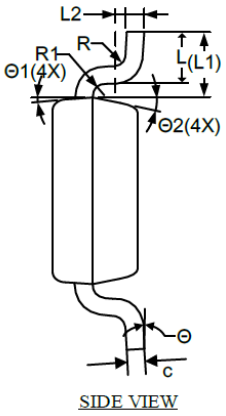


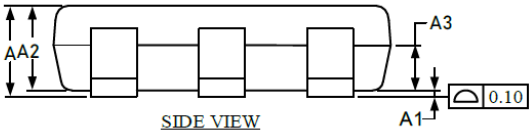


Symbol	Min.	Max.
A	-	1.35
A1	0.04	0.15
A2	1.00	1.20
A3	0.55	0.75
b	0.38	0.48
b1	0.37	0.43
c	0.11	0.21
c1	0.10	0.16
D	2.72	3.12
E	2.60	3.00
E1	1.40	1.60
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.575 REF	
L2	0.258 BSC	
θ	0°	8°

Dimension in TSOT-25 (Unit: mm)







Symbol	Min.	Max.
A	-	0.90
A1	0.00	0.10
A2	0.65	0.85
A3	0.35	0.45
b	0.30	0.50
c	0.14	0.20
D	2.85	3.05
E	2.65	2.95
E1	1.60	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60
L1	0.575 REF	
L2	0.258 BSC	
R	-	0.25
R1	-	0.25
θ	0°	8°
θ1	3°	7°
θ2	10°	14°

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