

ACT-D1M96S High Speed 96 MegaBit 3.3V Synchronous DRAM Multichip Module

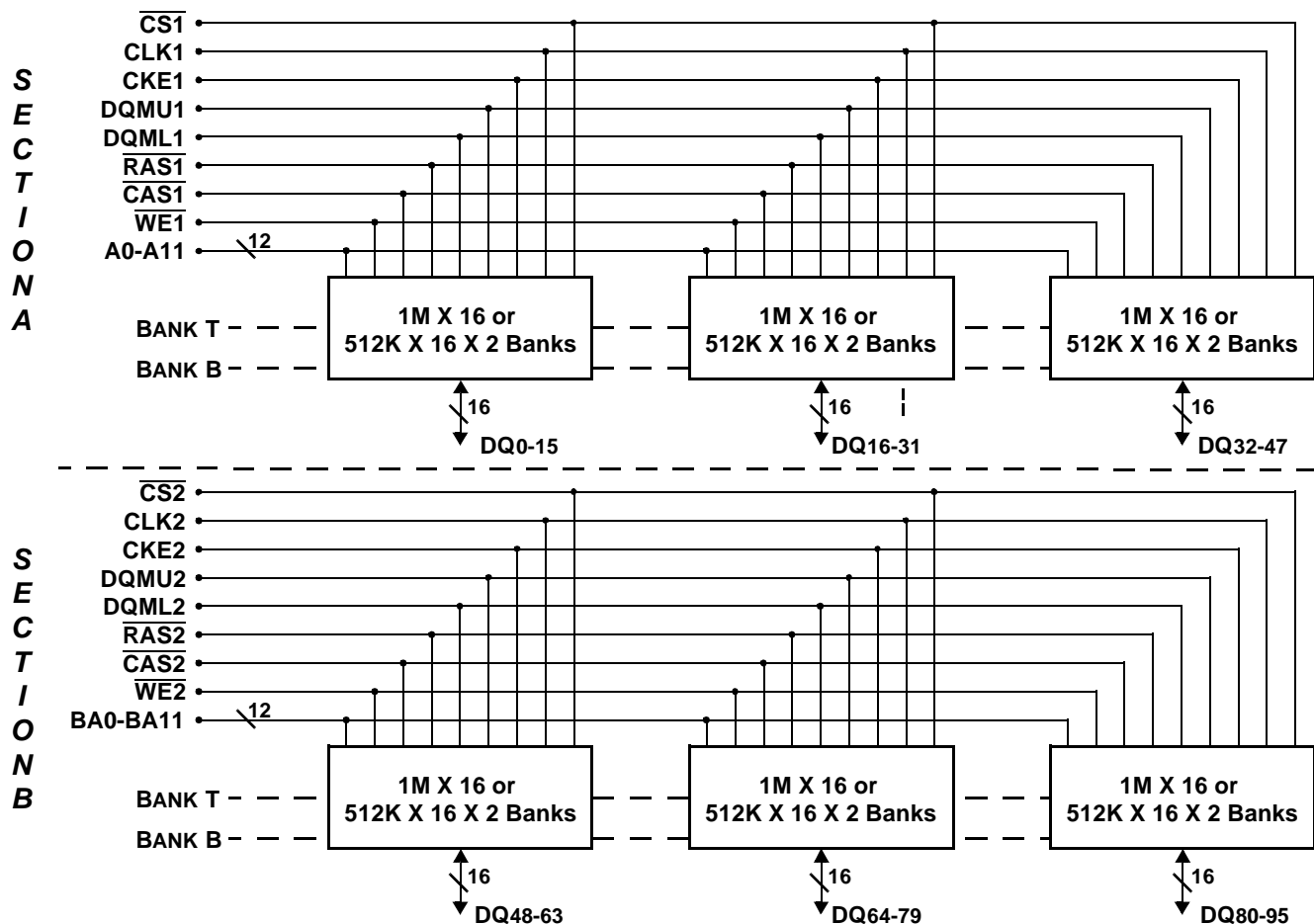
Features

- 6 Low Power Micron 1M X 16 Synchronous Dynamic Random Access Memory Chips in one MCM
- User Configurable as "2" Independent 512K X 48 X 2 Banks
- High-Speed, Low-Noise, Low-Voltage TTL (LVTTTL) Interface
- 3.3-V Power Supply ($\pm 10\%$ Tolerance)
- Separate Logic and Output Driver Power Pins
- Two Banks for On-Chip Interleaving (Gapless Accesses)
- Up to 50-MHz Data Rates
- CAS Latency (CL) Programmable to 2 Cycles From Column-Address Entry
- Burst Length Programmable to 4 or 8
- Pipeline Architecture
- Cycle-by-Cycle DQ-Bus Write Mask Capability With Upper and Lower Byte Control
- Chip Select and Clock Enable for Enhanced-System Interfacing
- Serial Burst Sequence
- Auto-Refresh
- 4K Refresh (Total for Both Banks)
- 200-lead CQFP, cavity-up package

General Description

The ACT-D1M96S device is a high-speed 96Mbit synchronous dynamic random access memory (SDRAM) organized as 2 independent 512K X 48 X 2 banks. All inputs and outputs of the ACT-D1M96S are compatible with the LVTTTL interface. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

BLOCK DIAGRAM



Operation

All inputs to the ACT-D1M96S SDRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0-DQ95, also are referenced to the rising edge of CLK. The ACT-D1M96S has two banks in each section that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

Five basic commands or functions control most operations of the ACT-D1M96S:

- Bank activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank deactivate
- Auto-refresh

Additionally, operations can be controlled by three methods:

- Chip select (\overline{CS}) to select/ deselect the devices
- DQMx to enable/mask the DQ signals on a cycle-by-cycle basis
- CKE to suspend (or gate) the CLK input

The device contains a mode register that must be programmed for proper operation. Table 1 through Table 3 show the various operations that are available on the ACT-D1M96S. These truth tables identify the command and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any read or write command in progress at cycle n. Access operations include the cycle upon which the read or write command is entered and all subsequent cycles through the completion of the access burst.

Burst Sequence

All data for the ACT-D1M96S is written or read in a burst fashion, that is, a single starting address is entered into the device and then the ACT-D1M96S internally accesses a sequence of locations based on that starting address. After the first access some of the subsequent accesses can be at preceding as well as succeeding column addresses, depending on the starting address entered. This sequence is programmed to follow a serial burst (see Table 4 and 5). The length of the burst can be programmed is 4 or 8. After a read burst is

complete (as determined by the programmed-burst length), the outputs are in the high-impedance state until the next read access is initiated.

Latency

The beginning data-out cycle of a read burst can be programmed to occur two CLK cycles after the read command. The delay between the READ command and the beginning of the output burst is known as \overline{CAS} latency. After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the mode-register contents.

Two-Bank Operation

The ACT-D1M96S contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank then must be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding \overline{RAS} low, \overline{CAS} high, \overline{WE} high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation).

Two-Bank Row-Access Operation

The two-bank feature allows access of information on random rows at a higher rate of operation than is possible with a standard DRAM, by activating one bank with a row address and, while the data stream is being accessed to/from that bank, activating the second bank with another row address. When the data stream to or from the first bank is complete, the data stream to or from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion.

Two-Bank Column-Access Operation

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met.

Bank Deactivation (Precharge)

Both banks can be deactivated (placed in precharge) simultaneously by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 used to select the bank to be precharged as shown in Table 1. A bank can be deactivated automatically by using A10 during a read or write command. If A10 is held high during the entry of a read or write command, the accessed bank (selected by A11) is deactivated automatically upon completion of the access burst. If A10 is held low during the entry of a read or write command, that bank remains active following the burst. The read and write commands with automatic deactivation are signified as READ-P and WRT-P.

Chip Select (\overline{CS})

\overline{CS} can be used to select or deselect the ACT-D1M96S for command entry, which might be required for multiple-memory-device decoding. If \overline{CS} is held high on the rising edge of CLK (DESL command), the device does not respond to \overline{RAS} , \overline{CAS} , or \overline{WE} until the device is selected again by holding \overline{CS} low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). The use of \overline{CS} does not affect an access burst that is in progress; the DESL command can only restrict \overline{RAS} , \overline{CAS} , and \overline{WE} input to the ACT-D1M96S.

Data Mask

The mask command or its opposite, the data-in enable (ENBL) command (see Table 3), is performed on a cycle-by-cycle basis to gate any data cycle within a write burst. DQML controls DQ0-7, DQ16-23, DQ32-39, DQ48-55, DQ64-71,

DQ80-87 and DQMU controls DQ8-15, DQ24-31, DQ40-47, DQ56-63, DQ72-79, and DQ88-95. The application of DQMx to a write burst has no latency ($nDID = 0$ cycle). During a write burst, if DQMx is held high on the rising edge of CLK, the data-input is ignored on that cycle.

CLK-Suspend

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE returns high. This is known as a CLK-suspend operation, and its execution indicates a HOLD command. The device resumes operation from the point when it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

Setting the Mode Register

The ACT-D1M96S contains a mode register in each chip that must be programmed with the CAS latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on the address lines A0-A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don't-care entries for the ACT-D1M96S. When A9 = 0, the write-burst length is defined by A0-A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding \overline{RAS} , \overline{CAS} , and \overline{WE} low and the input mode word valid on A0-A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.

Refresh

The ACT-D1M96S must be refreshed at intervals not exceeding t_{REF} (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing a read or write access to every row in both banks or 4096 auto-refresh (REFR) commands. Regardless of the method used, refresh must be accomplished before t_{REF} has expired.

Auto Refresh (REFR)

Before performing a REFR, both banks of all 6 chips must be deactivated (placed in precharge). To enter a REFR command, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must be low and $\overline{\text{WE}}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that, after 4096 REFR commands, both banks of all 6 chips of the ACT-D1M96S have been refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal auto-refresh cycle, allowing consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before tREF expires.

Power Up Initialization

Device initialization should be performed after a power up to the full Vcc level. After power is established, a 200 μ s interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

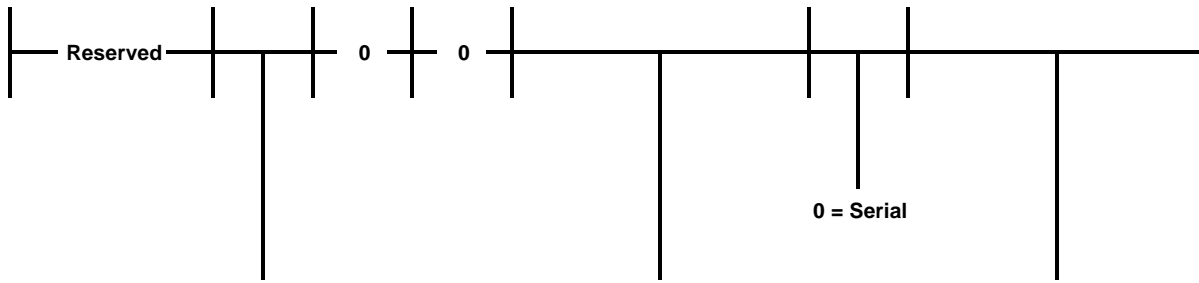
General Information for AC Timing Measurements

All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

Note: For all pin references in the General Description, both sections apply. For example, A11 signals also apply for BA11 signals.

For additional Detail Information regarding the operation of the individual chip (MT48LC1M16A1) see Micron's 524,288-WORD BY 16-BIT BY 2-BANK SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY Datasheet Revision 8/99 or contact the Aeroflex Sales Department.

| | | | | | | | | | | | |
|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| BA11 | BA10 | BA9 | BA8 | BA7 | BA6 | BA5 | BA4 | BA3 | BA2 | BA1 | BA0 |



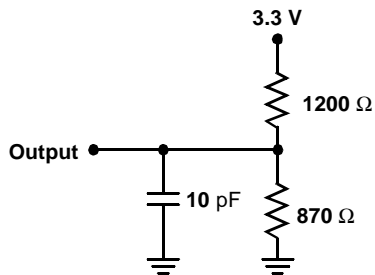
| Register Bit A9/BA9 | Write Burst Length |
|---------------------|----------------------|
| 0 | A2 - A0 BA2 - BA0 |

| Register Bits [†] | | | CAS Latency |
|----------------------------|-----------|-----------|-------------|
| A6 BA6 | A5 BA5 | A4 BA4 | |
| 0 | 1 | 0 | 2 |

| Register Bits [†] | | | Burst Length |
|----------------------------|-----------|-----------|--------------|
| A2 BA2 | A1 BA1 | A0 BA0 | |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |

NOTES:
[†] All other combinations are reserved.

Figure 1 – Mode Register Programming



AC Test Conditions

| Parameter | Typical | Units |
|-----------------------------------|-----------|-------|
| Input Pulse Level | 0.4 – 2.4 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Timing Reference | 1.5 | V |

Figure 2 – LVTTL-Load Circuit

Table 1 — Basic Command Truth Table †

| Command ‡ | State of Bank(s) | $\overline{CS1}$ $\overline{CS2}$ | $\overline{RAS1}$ $\overline{RAS2}$ | $\overline{CAS1}$ $\overline{CAS2}$ | WE1 WE2 | A11 BA11 | A10 BA10 | A9-A0 BA9-BA0 | Mne- monic |
|---|----------------------|--------------------------------------|--|--|------------|-------------|-------------|--|---------------|
| Mode register set | T = deac B = deac | L | L | L | L | X | X | A9,BA9 = V A8,BA8,A7,BA7 = 0 A6-A0,BA6-BA0 = V | MRS |
| Bank deactivate (precharge) | X | L | L | H | L | BS | L | X | DEAC |
| Deactivate all banks (precharge) | X | L | L | H | L | X | H | X | DCAB |
| Bank activate/row-address entry | SB = deac | L | L | H | H | BS | V | V | ACTV |
| Column-address entry/write operation | SB = actv | L | H | L | L | BS | L | V | WRT |
| Column-address entry/write operation with auto-deactivate | SB = actv | L | H | L | L | BS | H | V | WRT-P |
| Column-address entry/read operation | SB = actv | L | H | L | H | BS | L | V | READ |
| Column-address entry/read operation with auto-deactivate | SB = actv | L | H | L | H | BS | H | V | READ-P |
| Burst stop | SB = actv | L | H | H | L | X | X | X | STOP |
| No operation | X | L | H | H | H | X | X | X | NOOP |
| Control-input inhibit/no operation | X | H | X | X | X | X | X | X | DESL |
| Auto refresh § | T = deac B = deac | L | L | L | H | X | X | X | REFR |

NOTES:

† For execution of these commands on cycle n:

-CKE (n-1) must be high, or

-tCES and nCLE must be satisfied for clock-suspend exit.

DQMx(n) is a don't care.

‡ All other unlisted commands are considered vendor-reserved commands or illegal commands.

§ Auto-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

n = CLK cycle number, L = Logic low, H = Logic high, X = Don't care, either logic low or logic high, V = Valid, T = Bank T, B = Bank B, actv = Activated, deac = Deactivated, BS = Logic high to select bank T; logic low to select bank B, SB = Bank selected by A11 at cycle n

Table 2 — Clock Enable (CKE) Command Truth Table †

| Command ‡ | State of Bank(s) | CKE (n-1) | CKE (n) | \overline{CS} (n) | \overline{RAS} (n) | \overline{CAS} (n) | \overline{WE} (n) | Mnemonic |
|-----------------------------------|--|--------------|------------|------------------------|-------------------------|-------------------------|------------------------|----------|
| CLK suspend on cycle (n + 1) | T = access operation ¶ B = access operation ¶ | H | L | X | X | X | X | HOLD |
| CLK suspend exit on cycle (n + 1) | T = access operation ¶ B = access operation ¶ | L | H | X | X | X | X | — |

NOTES:

† For execution of these commands, A0-A11 (n) and DQMx (n) are don't cares.

‡ All other unlisted commands are considered vendor-reserved commands or illegal commands.

¶ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:

n = CLK cycle number, L = Logic low, H = Logic high, X = Don't care, either logic low or logic high, T = Bank T, B = Bank B

Table 3 — Data-Mask (DQM) Command Truth Table †

| Command ‡ | State of Bank(s) | DQML DQMU [§] (n) | Data In (n) | Data Out (n+2) | Mnemonic |
|-----------------|--|----------------------------|-------------|----------------|----------|
| — | T = deac and B = deac | X | N/A | Hi-Z | — |
| — | T = actv and B = actv (no access operation) [¶] | X | N/A | Hi-Z | — |
| Data-in enable | T = Write or B = Write | L | V | N/A | ENBL |
| Data-in mask | T = Write or B = Write | H | M | N/A | MASK |
| Data-out enable | T = Write or B = Write | L | N/A | V | ENBL |

NOTES:

† For execution of these commands on cycle n:

- CKE (n) must be high, or
- t CES and n CLE must be satisfied for clock suspend exit.

CS(n), RAS(n), CAS(n), WE(n), and A0-A11 are don't cares.

‡ All other unlisted commands are considered vendor-reserved commands or illegal commands.

§ DQML controls DQ0-7, DQ16-23, DQ32-39, DQ48-55, DQ64-71, DQ80-87 and DQMU controls DQ8-15, DQ24-31, DQ40-47, DQ56-63, DQ72-79, and DQ88-95.

¶ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:

n = CLK cycle number, L = Logic low, H = Logic high, X = Don't care, either logic low or logic high, V = Valid, M = Masked input data, N/A = Not applicable, T = Bank T, B = Bank B, actv = Activated, deac = Deactivated, write = Activated and accepting data inputs on cycle n, read = Activated and delivering data outputs on cycle (n + 2)

Table 4 — Serial 4-Word Burst Sequences

| INTERNAL COLUMN ADDRESS A1-A0, BA1-BA0 | | | | | | | |
|--|-----|-----|-----|--------|-----|-----|-----|
| DECIMAL | | | | BINARY | | | |
| START | 2ND | 3RD | 4TH | START | 2ND | 3RD | 4TH |
| 0 | 1 | 2 | 3 | 00 | 01 | 10 | 11 |
| 1 | 2 | 3 | 0 | 01 | 10 | 11 | 00 |
| 2 | 3 | 0 | 1 | 10 | 11 | 00 | 01 |
| 3 | 0 | 1 | 2 | 11 | 00 | 01 | 10 |

Table 5 – Serial 8-Word Burst Sequences

| INTERNAL COLUMN ADDRESS A2-A0, BA2-BA0 | | | | | | | | | | | | | | | |
|--|-----|-----|-----|-----|-----|-----|-----|--------|-----|-----|-----|-----|-----|-----|-----|
| DECIMAL | | | | | | | | BINARY | | | | | | | |
| START | 2ND | 3RD | 4TH | 5TH | 6TH | 7TH | 8TH | START | 2ND | 3RD | 4TH | 5TH | 6TH | 7TH | 8TH |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 001 | 010 | 011 | 100 | 101 | 110 | 111 | 000 |
| 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 010 | 011 | 100 | 101 | 110 | 111 | 000 | 001 |
| 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 011 | 100 | 101 | 110 | 111 | 000 | 001 | 010 |
| 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 100 | 101 | 110 | 111 | 000 | 001 | 010 | 011 |
| 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 101 | 110 | 111 | 000 | 001 | 010 | 011 | 100 |
| 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 110 | 111 | 000 | 001 | 010 | 011 | 100 | 101 |
| 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 111 | 000 | 001 | 010 | 011 | 100 | 101 | 110 |

Absolute Maximum Ratings¹

| Symbol | Rating | Range | Units |
|--------------------|--|-------------|-------|
| V _{CC} | Supply Voltage | -0.5 to 4.6 | V |
| V _{CCQ} | Supply Voltage range for output drivers | -0.5 to 4.6 | V |
| V _{RANGE} | Voltage range on any pin with respect to V _{SS} | -0.5 to 4.6 | V |
| T _{BIAS} | Case Temperature under Bias ² | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{SHORT} | Short-Circuit Output Current | 50 | mA |
| PW | Power Dissipation | 4.2 | W |

1. Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The temperature rise of θ_{jc} is negligible due to the low duty cycle during testing.

Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|------------------|---|---------|---------|-----------------------|-------|
| V _{CC} | Supply Voltage | 3 | 3.3 | 3.6 | V |
| V _{CCQ} | Supply Voltage range for output drivers | 3 | 3.3 | 3.6 | V |
| V _{SS} | Supply Voltage | | 0 | | V |
| V _{SSQ} | Supply Voltage range for output drivers | | 0 | | V |
| V _{IH} | Input High Voltage | 2 | | V _{CC} + 0.3 | V |
| V _{IL} | Input Low Voltage ¹ | -0.3 | | 0.8 | V |
| T _C | Operating Temperature (Case) ² | -55 | | +110 | °C |

1. V_{IL} Minimum = 1.5Vac (Pulsewidth ≤ 5ns)

2. The temperature rise of θ_{jc} is negligible due to the low duty cycle during testing.

DC Characteristics

(V_{CC} = 3.3V ±10%; T_C = -55°C to +110°C, See Notes 1 & 5)

| Parameter | Symbol | Conditions | Min | Max | Units |
|--|-----------------|--|-----|-----|-------|
| Output Low Voltage | V _{OL} | I _{OL} = 2mA | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -2mA | 2.4 | | V |
| Input current (Leakage) | I _I | 0V ≤ V _I ≤ V _{CC} + 0.3V, All other pins = 0V to V _{CC} | -10 | +10 | μA |
| Output current (Leakage) | I _O | 0V ≤ V _O ≤ V _{CC} + 0.3V, Output disabled | -10 | +10 | μA |
| Precharge standby current in non-power-down mode | ICC2N | CKE ≥ V _{IH} MIN, t _{CK} = 20ns (See note 2) | | 180 | mA |
| | ICC2NS | CKE ≥ V _{IH} MIN, CLK < V _{IL} MAX, t _{CK} = ∞ (See note 3) | | 40 | mA |

1. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

2. Control, DQ, and address inputs change state only once every 40 ns.

3. Control, DQ, and address inputs do not change (stable).

4. All I_{CC} parameters measured with V_{CC}, not V_{CCQ}.

5. The temperature rise of θ_{jc} is negligible due to the low duty cycle during testing.

Capacitance[†]
(f = 1MHz, Tc = 25°C)

| Symbol | Parameter | Min | Max | Units |
|--------|--|-----|-----|-------|
| Ci(S) | Input Capacitance, CLK Input | | 50 | pF |
| Ci(AC) | Input Capacitance, Address and Control Inputs: A0-A11, \overline{CS} , DQMx, \overline{RAS} , \overline{CAS} , \overline{WE} | | 40 | pF |
| Ci(E) | Input Capacitance, CKE Input | | 50 | pF |
| Co | Output Capacitance | | 20 | pF |

[†]Parameters Guaranteed but not tested

AC Timing^{†‡}
(Vcc = 3.3V ±0.3V, Tc = -55°C to +110°C, See Note 4)

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|---|--------|-----------------|--|--------|-------|
| Cycle time, CLK | tCK2 | CAS latency = 2 | 20 | | ns |
| Pulse duration, CLK high | tCH | | 6 | | ns |
| Pulse duration, CLK low | tCL | | 6 | | ns |
| Access time, CLK high to data out (see Note 1) | tAC2 | CAS latency = 2 | | 13 | ns |
| Hold time, CLK high to data out | tOH | | 1 | | ns |
| Setup time, address, control, and data input | tIS | | 5 | | ns |
| Hold time, address, control, and data input | tIH | | 3 | | ns |
| Delay time, ACTV command to DEAC or DCAB command | tRAS | | 72 | 100000 | ns |
| Delay time, ACTV or REFR to ACTV, MRS or REFR command | tRC | | 108 | | ns |
| Delay time ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 2) | tRCD | | 30 | | ns |
| Delay time, DEAC or DCAB command to ACTV, MRS or REFR command | tRP | | 36 | | ns |
| Delay time, ACTV command in one bank to ACTV command in the other bank | tRRD | | 24 | | ns |
| Delay time, MRS command to ACTV, MRS or REFR command | tRSA | | 30 | | ns |
| Final data out of READ-P operation to ACTV, MRS or REFR command | tAPR | | Min tRP - (CL - 1) * tCK (see Note 3) | | ns |
| Final data in of WRT-P operation to ACTV, MRS or REFR command | tAPW | | 60 | | ns |

AC Timing^{†‡} (cont.)

(V_{CC} = 3.3V ±0.3V, T_c = -55°C to +110°C, See Note 4)

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|---|-------------------|-----------------|-----|-----|-------|
| Delay time, final data in of WRT operation to DEAC or DCAB command | t _{WR} | | 20 | | ns |
| Refresh interval | t _{REF} | | | 50 | ms |
| Delay time, \overline{CS} low or high to input enabled or inhibited | n _{CDD} | | 0 | 0 | cycle |
| Delay time, CKE high or low to CLK enabled or disabled | n _{CLE} | | 1 | 1 | cycle |
| Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P | n _{CWL} | | 1 | | cycle |
| Delay time, ENBL or MASK command to enabled or masked data in | n _{DID} | | 0 | 0 | cycle |
| Delay time, ENBL or MASK command to enabled or masked data out | n _{DOD} | | 2 | 2 | cycle |
| Delay time, DEAC or DCAB, command to DQ in high-impedance state | n _{HZP2} | CAS latency = 2 | | 2 | cycle |
| Delay time, WRT command to first data in | n _{WCD} | | 0 | 0 | cycle |
| Delay time, STOP command to READ or WRT command | n _{BSD} | | | 2 | cycle |

† See Figure 2 - LVTTTL Load Circuit for load circuits.

‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES:

1. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK within the following cycle: CAS latency minus one cycle after the READ command. An access time is measured at output reference level 1.5 V.

2. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

3. CL = CAS Latency.

4. The temperature rise of θ_{jc} is negligible due to the low duty cycle during testing.

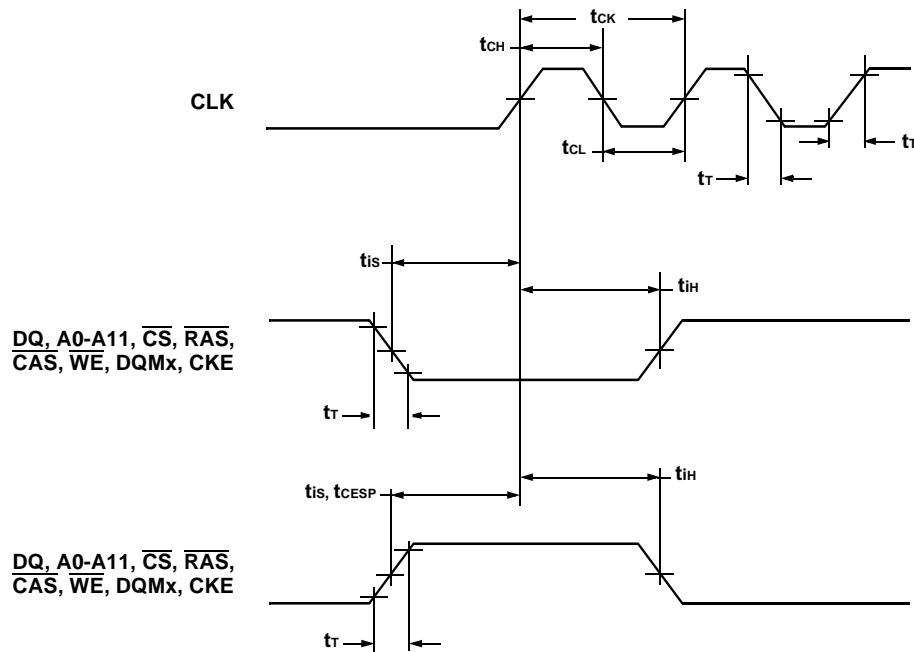


Figure 3 – Input-Attribute Parameters

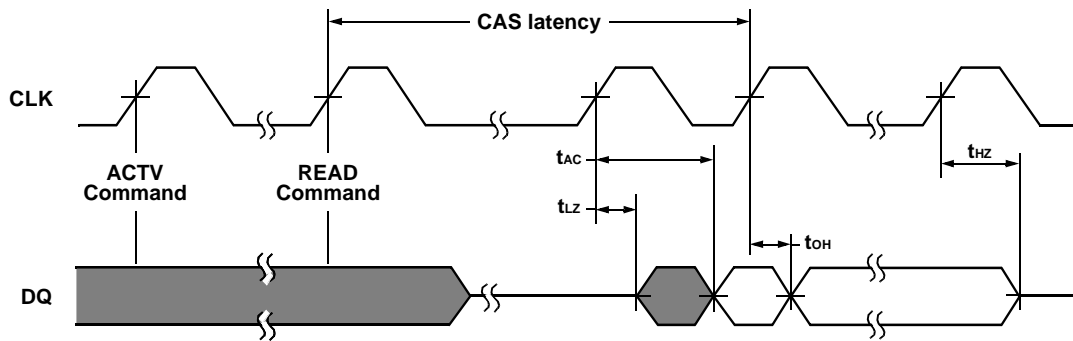


Figure 4 – Output Parameters

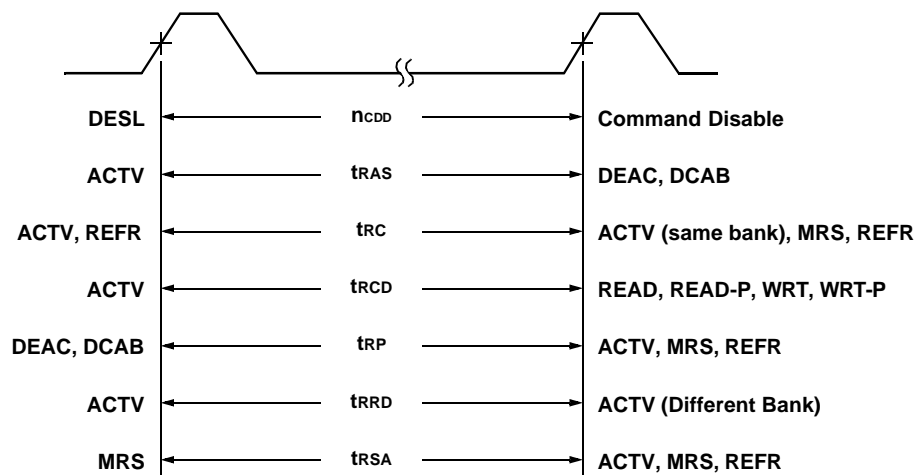
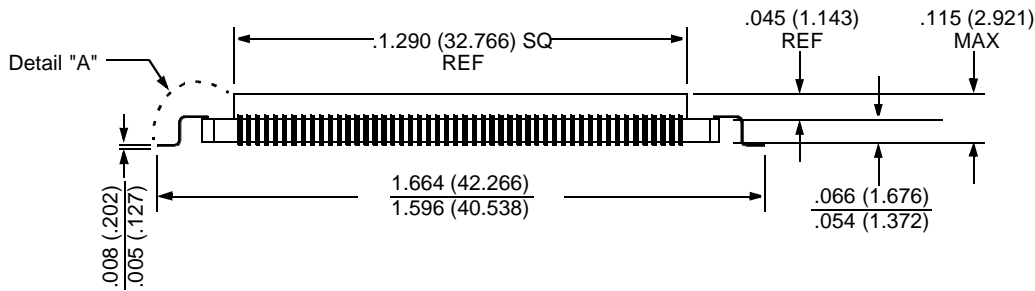
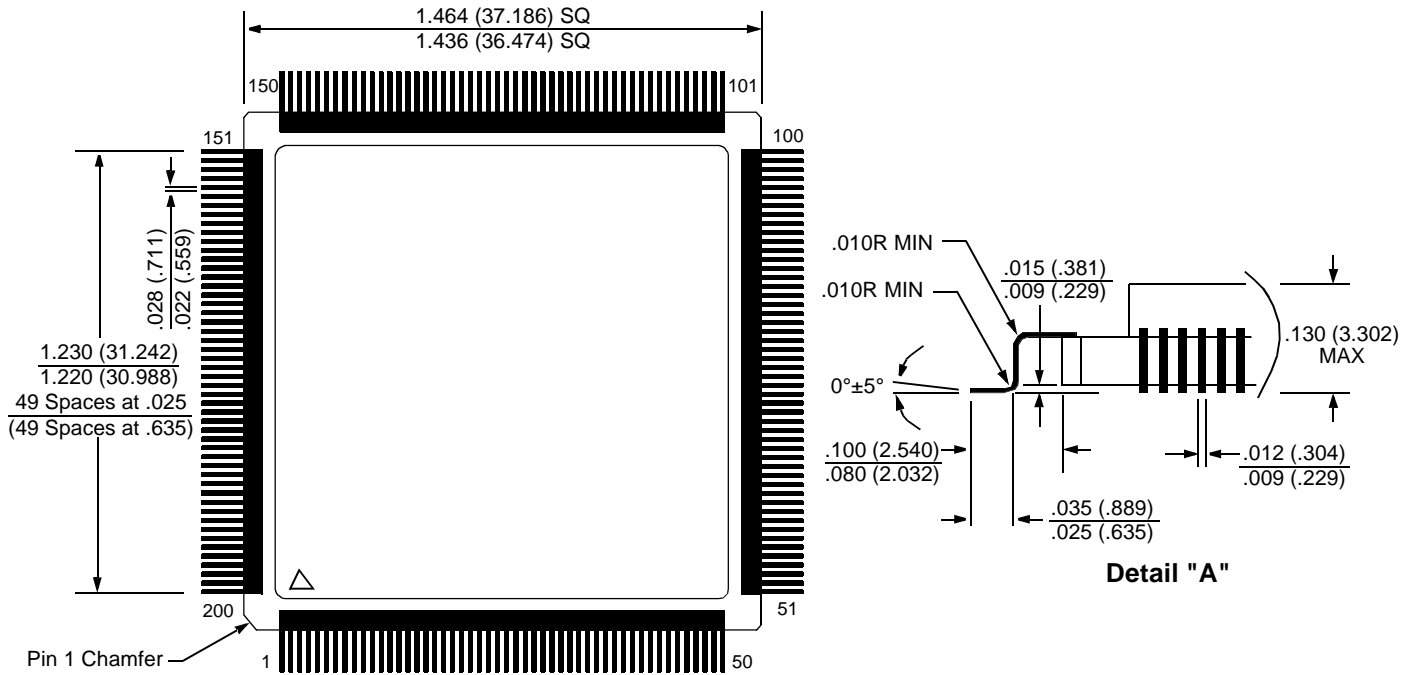


Figure 5 – Command-to-Command Parameters

Package Information – "F20" – CQFP 200 Leads



Note: 1. All Dimensions in inches (Millimeters) MAX or Typical where noted.
MIN

Pin Nomenclature

| | | | |
|---|---|------------------------------|---------------------------------|
| A0-A10 BA0-BA10 | Address Inputs A0-A10, BA0-BA10 Row Addresses A0-A7, BA0-BA7 Column Addresses A10, BA10 Automatic-Precharge Select | DQML1,2 DQMU1,2 | Data/Input Mask Enables |
| A11,BA11 | Bank Select | RAS $\bar{1}$,RAS $\bar{2}$ | Row-Address Strobe |
| $\bar{C}AS\bar{1}$, $\bar{C}AS\bar{2}$ | Column-Address Strobe | VCC | Power Supply |
| CKE1,CKE2 | Clock Enable | VCCQ | Power Supply for Output Drivers |
| CLK1,CLK2 | System Clock | VSS | Ground |
| $\bar{C}S\bar{1}$, $\bar{C}S\bar{2}$ | Chip Select | VSSQ | Ground for Output Drivers |
| DQ0-DQ95 | SDRAM Data Input/Output | WE $\bar{1}$,WE $\bar{2}$ | Write Enable |

ACT-D1M96S CQFP Pinouts – "F20"

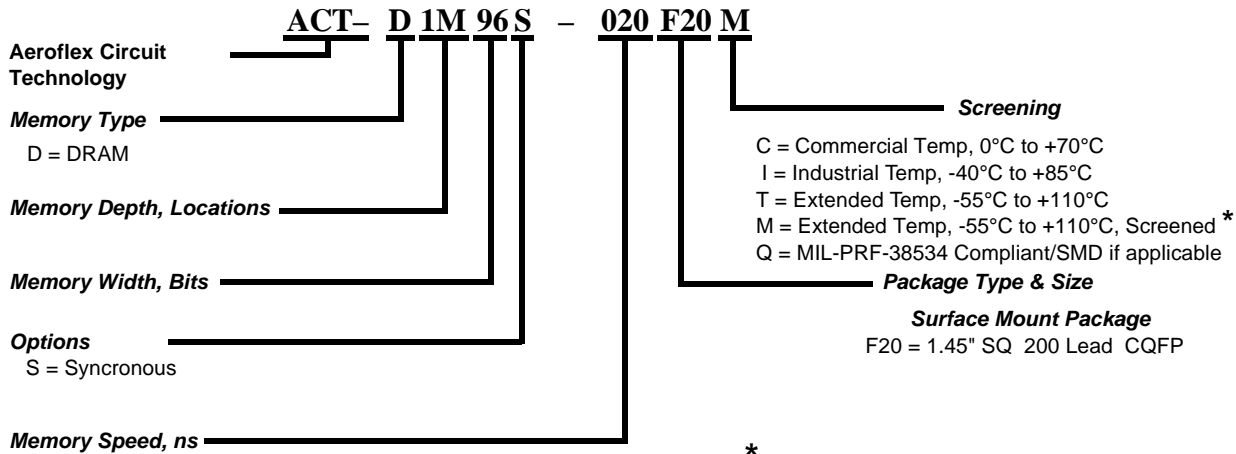
| PIN # | FUNCTION | PIN # | FUNCTION | PIN # | FUNCTION | PIN # | FUNCTION | PIN # | FUNCTION |
|--------------|-------------------|--------------|-----------------|--------------|-------------------|--------------|-----------------|--------------|-----------------|
| 1 | DQ2 | 41 | DQ91 | 81 | DQ67 | 121 | VSSQ | 161 | DQ30 |
| 2 | DQ3 | 42 | VSSQ | 82 | DQ66 | 122 | BA1 | 162 | VSSQ |
| 3 | VSSQ | 43 | DQ92 | 83 | VSS | 123 | BA2 | 163 | DQ29 |
| 4 | DQ4 | 44 | DQ93 | 84 | DQ65 | 124 | VCCQ | 164 | DQ28 |
| 5 | DQ5 | 45 | VCCQ | 85 | DQ64 | 125 | BA3 | 165 | VCC |
| 6 | VCCQ | 46 | DQ94 | 86 | VCC | 126 | A4 | 166 | DQ27 |
| 7 | DQ6 | 47 | DQ95 | 87 | DQ63 | 127 | VCCQ | 167 | DQ26 |
| 8 | DQ7 | 48 | VSSQ | 88 | DQ62 | 128 | A5 | 168 | VSS |
| 9 | VSSQ | 49 | DQ87 | 89 | VSSQ | 129 | A6 | 169 | DQ25 |
| 10 | DQML1 | 50 | DQ86 | 90 | DQ61 | 130 | VSSQ | 170 | DQ24 |
| 11 | $\overline{WE1}$ | 51 | DQ85 | 91 | DQ60 | 131 | A7 | 171 | VSSQ |
| 12 | VSSQ | 52 | DQ84 | 92 | VSSQ | 132 | A8 | 172 | CLK1 |
| 13 | $\overline{CAS1}$ | 53 | VSSQ | 93 | DQ59 | 133 | VSS | 173 | CKE1 |
| 14 | $\overline{RAS1}$ | 54 | DQ83 | 94 | DQ58 | 134 | A9 | 174 | VCCQ |
| 15 | VCC | 55 | DQ82 | 95 | VCCQ | 135 | DQMU1 | 175 | DQ23 |
| 16 | $\overline{CS1}$ | 56 | VCCQ | 96 | DQ57 | 136 | VCC | 176 | DQ22 |
| 17 | A11 | 57 | DQ81 | 97 | DQ56 | 137 | DQ40 | 177 | VCCQ |
| 18 | VSS | 58 | DQ80 | 98 | VSSQ | 138 | DQ41 | 178 | DQ21 |
| 19 | A10 | 59 | VSSQ | 99 | DQ48 | 139 | VSSQ | 179 | DQ20 |
| 20 | A0 | 60 | DQ79 | 100 | DQ49 | 140 | DQ42 | 180 | VSSQ |
| 21 | VSSQ | 61 | DQ78 | 101 | DQ50 | 141 | DQ43 | 181 | DQ19 |
| 22 | A1 | 62 | VSSQ | 102 | DQ51 | 142 | VSSQ | 182 | DQ18 |
| 23 | A2 | 63 | DQ77 | 103 | VSSQ | 143 | DQ44 | 183 | VSS |
| 24 | VCCQ | 64 | DQ76 | 104 | DQ52 | 144 | DQ45 | 184 | DQ17 |
| 25 | A3 | 65 | VCC | 105 | DQ53 | 145 | VCCQ | 185 | DQ16 |
| 26 | BA4 | 66 | DQ75 | 106 | VCCQ | 146 | DQ46 | 186 | VCC |
| 27 | VCCQ | 67 | DQ74 | 107 | DQ54 | 147 | DQ47 | 187 | DQ15 |
| 28 | BA5 | 68 | VSS | 108 | DQ55 | 148 | VSSQ | 188 | DQ14 |
| 29 | BA6 | 69 | DQ73 | 109 | VSSQ | 149 | DQ39 | 189 | VSSQ |
| 30 | VSSQ | 70 | DQ72 | 110 | DQML2 | 150 | DQ38 | 190 | DQ13 |
| 31 | BA7 | 71 | VSSQ | 111 | $\overline{WE2}$ | 151 | DQ37 | 191 | DQ12 |
| 32 | BA8 | 72 | CLK2 | 112 | VSSQ | 152 | DQ36 | 192 | VSSQ |
| 33 | VSS | 73 | CKE2 | 113 | $\overline{CAS2}$ | 153 | VSSQ | 193 | DQ11 |
| 34 | BA9 | 74 | VCCQ | 114 | $\overline{RAS2}$ | 154 | DQ35 | 194 | DQ10 |
| 35 | DQMU2 | 75 | DQ71 | 115 | VCC | 155 | DQ34 | 195 | VCCQ |
| 36 | VCC | 76 | DQ70 | 116 | $\overline{CS2}$ | 156 | VCCQ | 196 | DQ9 |
| 37 | DQ88 | 77 | VCCQ | 117 | BA11 | 157 | DQ33 | 197 | DQ8 |
| 38 | DQ89 | 78 | DQ69 | 118 | VSS | 158 | DQ32 | 198 | VSSQ |
| 39 | VSSQ | 79 | DQ68 | 119 | BA10 | 159 | VSSQ | 199 | DQ0 |
| 40 | DQ90 | 80 | VSSQ | 120 | BA0 | 160 | DQ31 | 200 | DQ1 |



Sample Ordering Information

| Part Number | Screening | Speed | Package |
|--------------------|--------------------------------|-------|---------------|
| ACT-D1M96S-020F20C | Commercial Temperature | 20 ns | 200 Lead CQFP |
| ACT-D1M96S-020F20T | Extended Temperature | 20 ns | 200 Lead CQFP |
| ACT-D1M96S-020F20M | Extended Temperature Screening | 20 ns | 200 Lead CQFP |

Part Number Breakdown



* Screened to the individual test methods of MIL-STD-883

Specifications subject to change without notice.

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|---|---|
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