PRELIMINARY PRODUCT SUMMARY

SKY77413 Front-End Module for WCDMA (824-849 MHz)

Applications

- Digital cellular (WCMDA) handsets

Features

- HSDPA (High Speed Downlink Packet Access)
- Low quiescent current
  - 20 mA
- Low current consumption
  - 450 mA
- Integrated Power Detector
- 22-pin package
- Small profile
  - 5 mm x 8 mm x 1.5 mm
- Low voltage
  - 3.2 V to 4.2 V
- Digital enable pin
- Highly integrated, user friendly solution
- InGaP HBT
- Integrated interstage filter and duplexer
- Requires few external components

NEW

Skyworks offers lead (Pb)-free "environmentally friendly" packaging that is RoHS compliant (European Parliament for the Restriction of Hazardous Substances).

Description

The SKY77413 Front-End Module (FEM) is a fully matched, 22-pin surface mount module developed for WCDMA applications. Small and efficient, this WCDMA FEM integrates the interstage filter, the input matching, the power amplifier, the output matching, the power detection, and the duplexer into a single 5 mm x 8 mm x 1.5 mm package.

The SKY77413 meets the stringent spectral requirements of HSDPA (High Speed Downlink Packet Access) up to 23.9 dBm output power. The FEM incorporates an InGaP HBT PA and contains circuitry to optimize power detector performance. Different control pins are available to enhance the performance of the FEM at different power levels.

Integration of the RF front-end greatly simplifies the design of the handset radio as all critical matching between the interstage filter, PA, power detection, and duplexer is optimized within the module. By optimizing the efficiency of the InGaP HBT PA MMIC and reducing the RF loss between the integrated components, this FEM achieves current as low as 450 mA at maximum output power (24.8 dBm) that significantly improves the talk time of the WCDMA handset. This small package uses Skyworks' low cost, multi-laminate substrate technology and is approximately half the size of individually-packaged component solutions. The SKY77413 front-end module can save handset designers significant board space and design-cycle time.

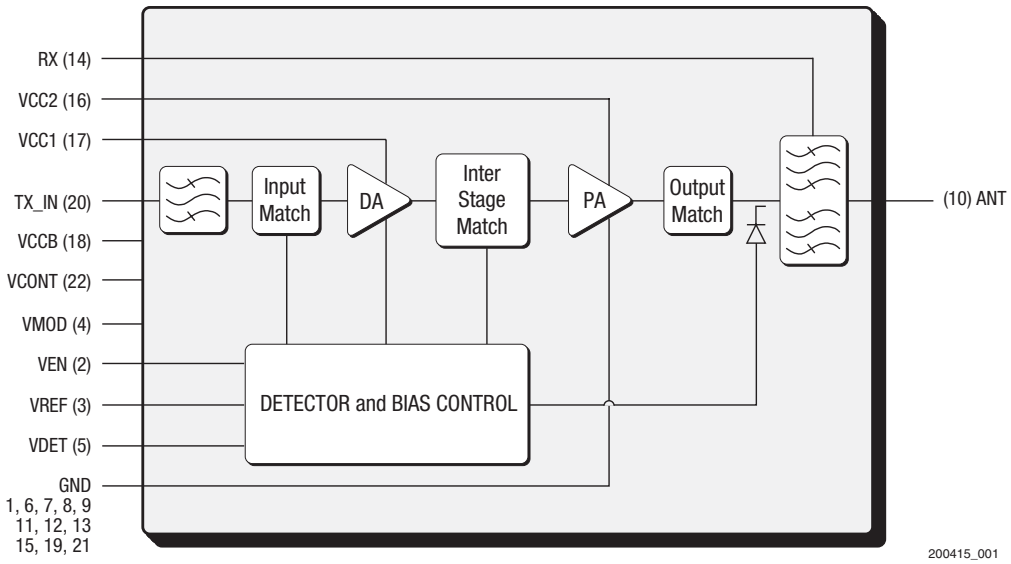


Figure 1. Functional Block Diagram

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