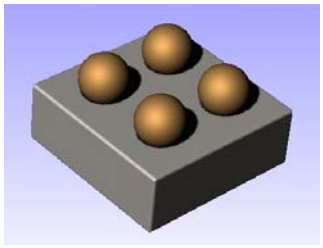
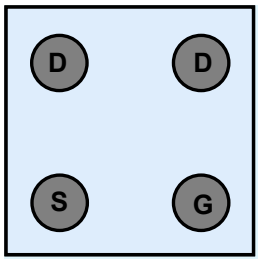
TSM8405P

Single P-Channel 1.8V Specified MicroSURF™ MOSFET



Patent Pending



Bump Side View

Lateral Power™ for
Load Switching and PA Switch

V_{DS} = - 12V
$R_{DS\ (on)}$, Vgs @ - 4.5V, Ids @ - 4.9A = 50mΩ
$R_{DS\ (on)}$, Vgs @ - 2.5V, Ids @ - 4.4A = 70mΩ
$R_{DS\ (on)}$, Vgs @ - 1.8V, Ids @ - 4.0A = 90mΩ

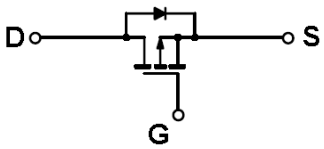
Description

TSM8405P is new low cost, state of the art MicroSURF™ lateral MOSFET process technology in chip scale bondwireless packaging minimizes PCB space and Rds(on) plus provides an ultra low Qg x Rds(on) figure of merit.

Features

- ✧ Low profile package: less than 0.8mm height when mounted on PCB
- ✧ Occupies only 2.25mm^2 of PCB area
- ✧ Less than 25% of the area of a SSOT-6
- ✧ Excellent thermal and electrical capabilities
- ✧ Lead free solder bumps available

Block Diagram



Ordering Information

Part No.	Packing	Q'ty
TSM8405P	Tape & Reel	3kpcs / 7"

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 12V	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	I_D	- 4.9	A
Pulsed Drain Current	I_{DM}	- 10	A
Maximum Power Dissipation (Steady State)	P_D	1. 5	W
Operating Junction Temperature	T_J	+150	°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

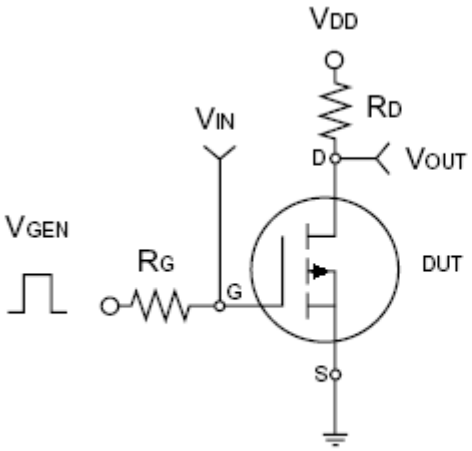
Parameter	Symbol	Limit	Unit
Junction to Ambient Thermal Resistance	Rθja	85	°C/W
Junction to Balls Thermal Resistance	$R\theta_{jR}$	12	°C/W

Electrical Characteristics

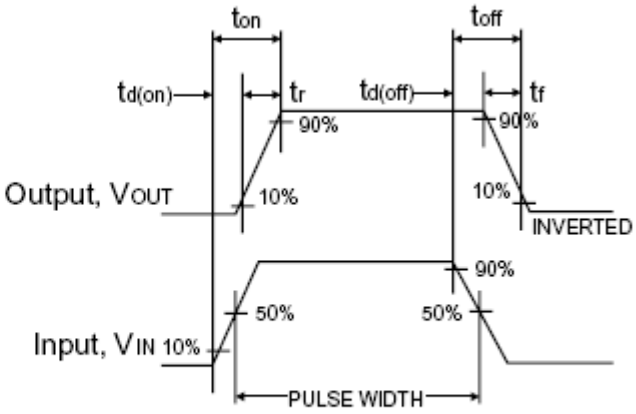
Ta = 25 °C, unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = - 250uA	BV_{DSS}	- -	--	-12	V
Drain-Source On-State Resistance	V_{GS} = - 4.5V, I_D = -1.0A	$R_{DS(ON)}$	--	--	50	mΩ
	V_{GS} = - 2.5V, I_D = -1.0A		--	--	70	
	V_{GS} = - 1.8V, I_D = -1.0A		--	--	90	
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = - 250uA	$V_{GS(TH)}$	--	- 0.7	--	V
Zero Gate Voltage Drain Current	V_{DS} =-12V, Ta=25 °C	I_{DSS}	--	--	- 1.0	uA
	V_{GS} = 0V, Ta=70 °C		--	--	- 5.0	
Gate Body Leakage	V_{GS} = ± 8V, V_{DS} = 0V	I_{GSS}	--	--	± 100	nA
Dynamic						
Total Gate Charge	V_{DS} = - 6V, I_D = - 1.0A, V_{GS} = - 4.5V	Q_g	--	9.0	--	nC
Input Capacitance	V_{DS} = - 12V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	800	--	pF
Output Capacitance		C_{oss}	--	250	--	
Reverse Transfer Capacitance		C_{rss}	--	100	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	- 1.0	A
Diode Forward Voltage	I_S = - 1.0A, V_{GS} = 0V	V_{SD}	--	- 0.7.1	- 1.2	V
Source-Drain Reverse Recovery Time	I_S = - 1.0A, V_{GS} = 0V, di / dt = 100A / uS	Trr	--	40	--	nS

Note : pulse test: pulse width <=300uS, duty cycle <=2%



Switching Test Circuit

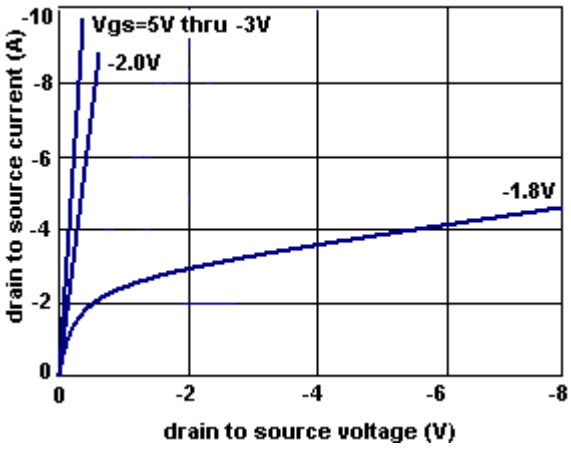


Switchin Waveforms

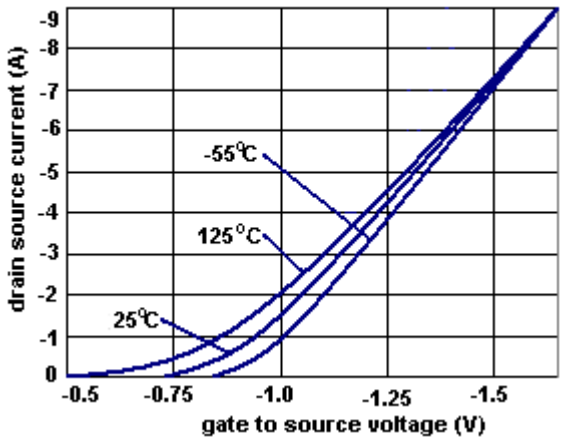
TSC

Typical Characteristics Curve (Ta = 25 °C unless otherwise noted)

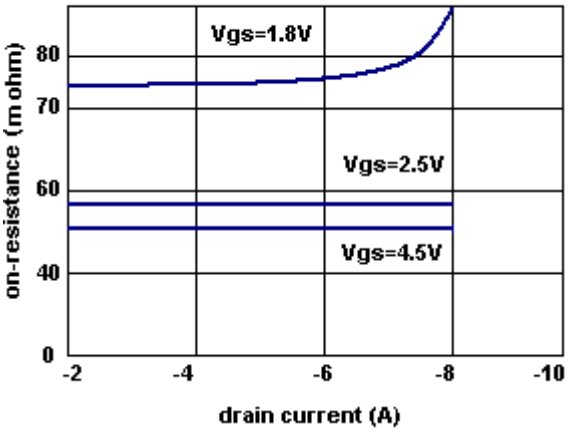
Output Characteristic



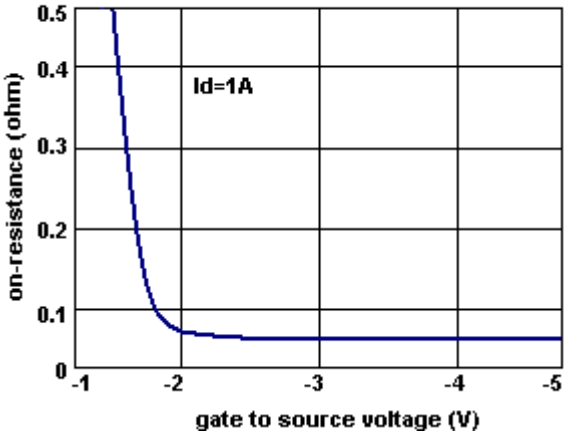
Transfer Characteristic



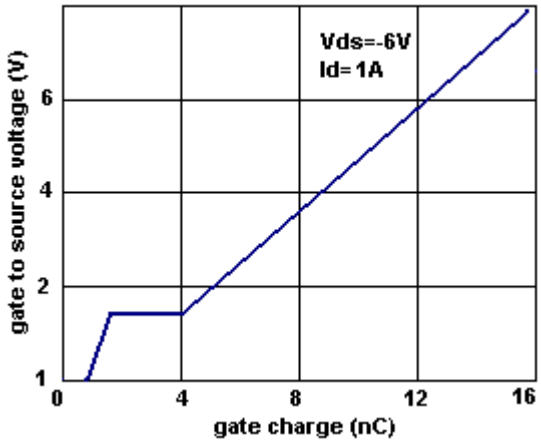
On Resistance vs Drain Current



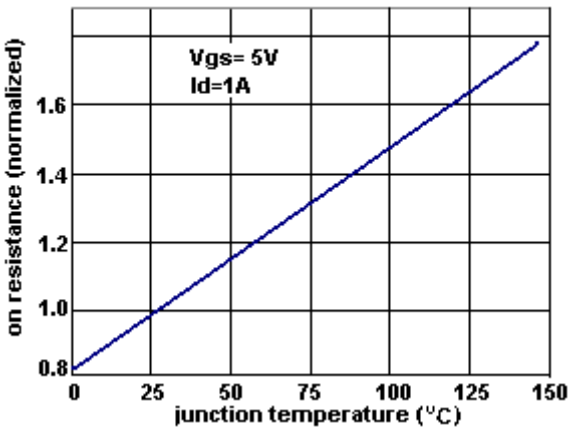
On Resistance vs Gate-Source



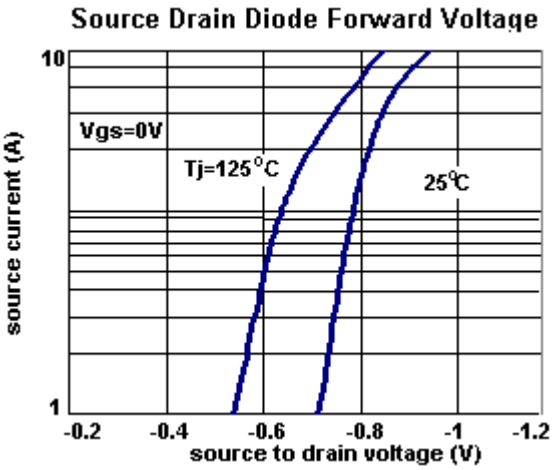
Gate Charge

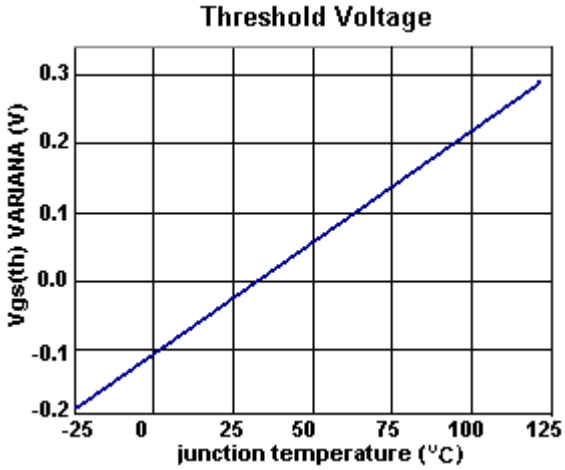


On Resistance vs Junction temp.

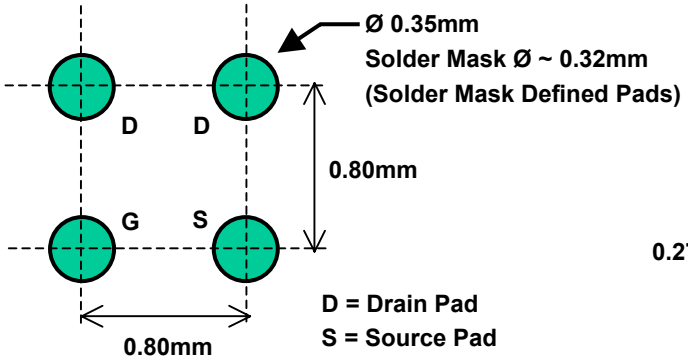


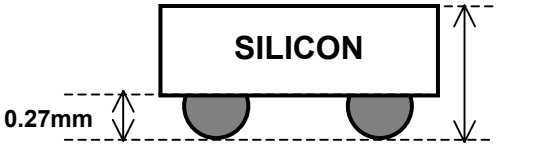
Typical Characteristics Curve (Ta = 25 °C unless otherwise noted)



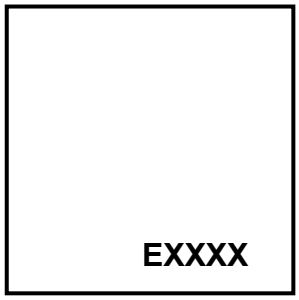


Dimensional Outline and Pad Layout

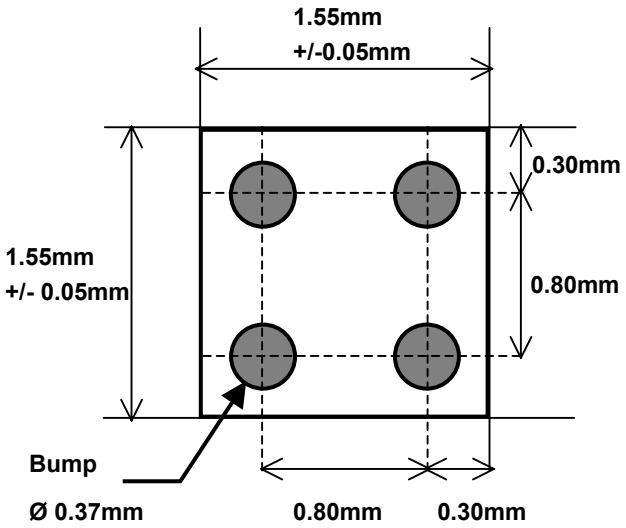




LAND PATTERN RECOMMENDATION



BACKSIDE VIEW (No Bump Side View)
Mark on backside of die
E = 8405P Product Code
XXXX = Lot Traceability Code
Mark is located in lower right quadrant on top of Drain pad. Gate pad is located in lower left quadrant.



Bumps are Lead Free solder 96.8 Sn / 2.6 Ag / 0.6 Cu

Patents are pending on the product described in the data sheet.

Lateral Power™ and MicroSURF™ are trademarks of Great Wall Semiconductor Corporation.

BGA FET Tape and reel Specification

1. Tape and Reel

1.1. Reel Size: 7 inch diameter.

1.2. Qty / Reel: 3,000pcs

1.3. Peel Strength:

1.3.1. Peel strength must be between 20 to 80 grams.

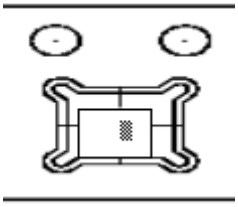
1.3.2. Minimum peel back length is 150 mm.

1.3.3. Peel back speed must be between 300 +/-5 mm per minute.

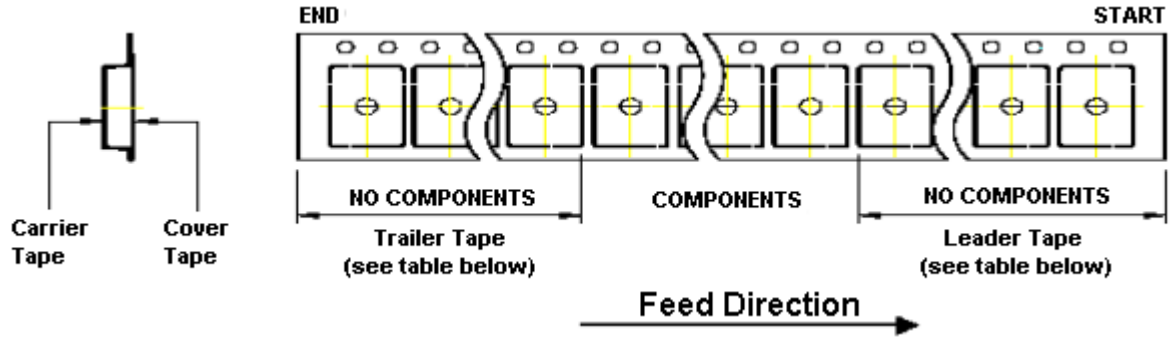
1.3.4. Peel back angle must be between 165 to 185 degrees with respect to the component carrier along the longitudinal axis of the carrier tape.

1.3.5 Peel strength test must be performed at the trailer.

1.4. Part Orientation: Marking in upper right quadrant

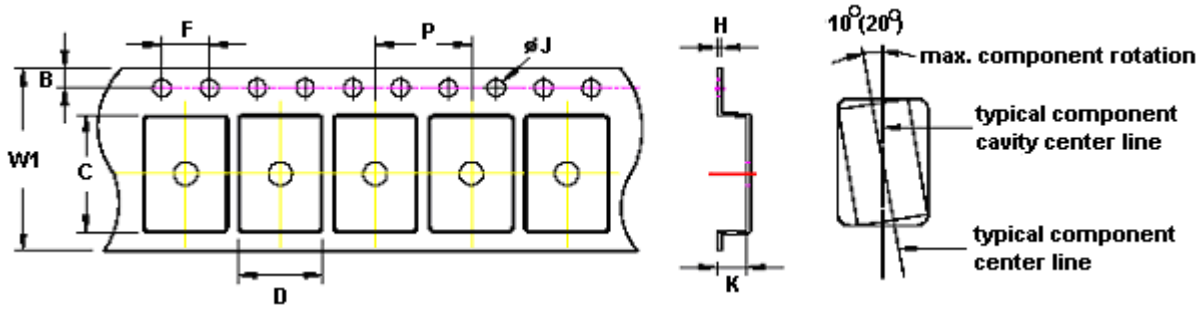


2. Tape Leader and Trailer



Die Size	Leader	Trailer
1.5 mm x 1.5 mm	500 mm	160 mm

3. Tape Dimension



Die Size	Tape size	W1	C	D	K	H	P	F	B
1.5 x 1.5 x 0.8	8	8.0+0.3 - 0.1	1.73±0.05	1.73±0.05	1,19±0.10	0.254±0.02	4.0	4.0	1.75±0.1