8-Bit Octal, 2-Quadrant Multiplying, CMOS TrimDAC

DAC-8841

FEATURES

Replaces 8 Potentiometers
Operates From Single +5 V Supply
1 MHz 2-Quadrant Multiplying Bandwidth
No Signal Inversion
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
+3 Volt Output Swing
Midscale Preset
Low 95 mW Power Dissipation

APPLICATIONS

Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation
Programmable Gain Amplifiers

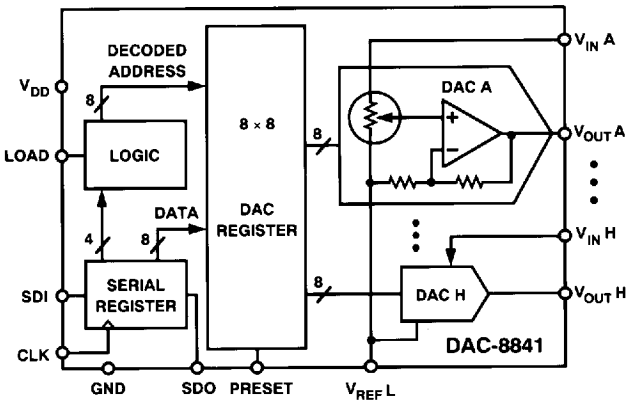
GENERAL DESCRIPTION

The DAC-8841 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability replaces the mechanical trimmer function in new designs. It is ideal for ac or dc gain control of up to 1 MHz bandwidth signals.

Internally the DAC-8841 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



The DAC-8841 consumes only 95 mW from a +5 V power supply. For dual polarity applications see the DAC-8840 which provides full 4-quadrant-multiplying ±3 V signal capability while operating from ±5 V power supplies.

The DAC-8841 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages. For MIL-STD/883 applications, contact ADI sales for the DAC-8841BW/883 data sheet which specifies operation over −55°C to +125°C.

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

DAC-8841—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0V, T_A = −40°C to +85°C apply for DAC-8841F, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL	Note 1		±1/2	±1.5	LSB
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1			±1	LSB
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475	1.500	1.525	V
Zero-Scale Output Voltage	V_{ZS}	Digital Code = 00_H		20	100	mV
Output Voltage Drift	TCV_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H		10		μV/°C
SIGNAL INPUTS		Applies to All Inputs $V_{IN}X$ or $V_{REF}L$				
Input Voltage Range	IVR		0		1.5	V
Input Resistance	R_{IN}	D = 55_H; Code Dependent	4	10		kΩ
Input Capacitance	C_{IN}	Code Dependent		19	30	pF
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	0.75		kΩ
REF Low Capacitance	$C_{REF}L$	Code Dependent		190	250	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	0		3	V
Output Current	I_{OUT}	ΔV_{OUT} < 25 mV, $V_{IN}X$ = 1.375V, $\overline{PR}$ = 0 V	±5	7		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p-p + 1.0 V dc	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
	+SR	$\Delta V_{OUT}X$ = +3 V	1.3	4.0		V/μs
	−SR	$\Delta V_{OUT}X$ = −3 V	1.3	2.5		V/μs
Total Harmonic Distortion	THD	$V_{IN}X$ = 1 V p-p + 1.0 V dc, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		μV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, 8_{10} to 255_{10}		3.5	6	μs
Channel to Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	70		dB
Digital Feedthrough	Q	$V_{REF}L$ = +1.5 V, D = 0 to FF_H		6		nVs
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			95	130	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V			0.01	%/%
Power Supply Range	PSR	V_{DD}	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	μA
Input Capacitance	C_{IL}				8	pF
Input Coding				Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = −0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS						
Input Clock Pulse Width	t_{CH}, t_{CL}		80			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				120	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTE

[1]INL and DNL tests do not include operation at codes 0 thru 7 due to zero-scale output voltage. For bias voltages above 100 mV on $V_{REF}L$, INL and DNL are maintained over all codes.

Specifications subject to change without notice.

WAFER TEST LIMITS: V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0 V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	DAC-8841GBC Limits	Units
Integral Nonlinearity	INL	Note 1	±1.5	LSB max
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1	±1	LSB max
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475/1.525	V min/max
Input Resistance ($V_{IN}X$)	R_{IN}	D = 55_H; Code Dependent	4	kΩ min
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	kΩ min
DAC Output Voltage Range	OVR	R_L = 10 kΩ	3	V min
DAC Output Current	I_{OUT}	ΔV_{OUT} < 25 mV	±5	mA min
Slew Rate		Measured 10% to 90%		
Positive	SR+	$\Delta V_{OUT}X$ = +3 V	1.3	V/μs min
Negative	SR−	$\Delta V_{OUT}X$ = −3 V	1.3	V/μs min
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V	26	mA max
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%	0.01	%/% max
Logic Input High	V_{IH}		2.4	V min
Logic Input Low	V_{IL}		0.8	V max
Logic Input Current	I_L		±10	μA max
Logic Output High	V_{OH}	I_{OH} = −0.4 mA	3.5	V min
Logic Output Low	V_{OL}	I_{OL} = 1.6 mA	0.4	V max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

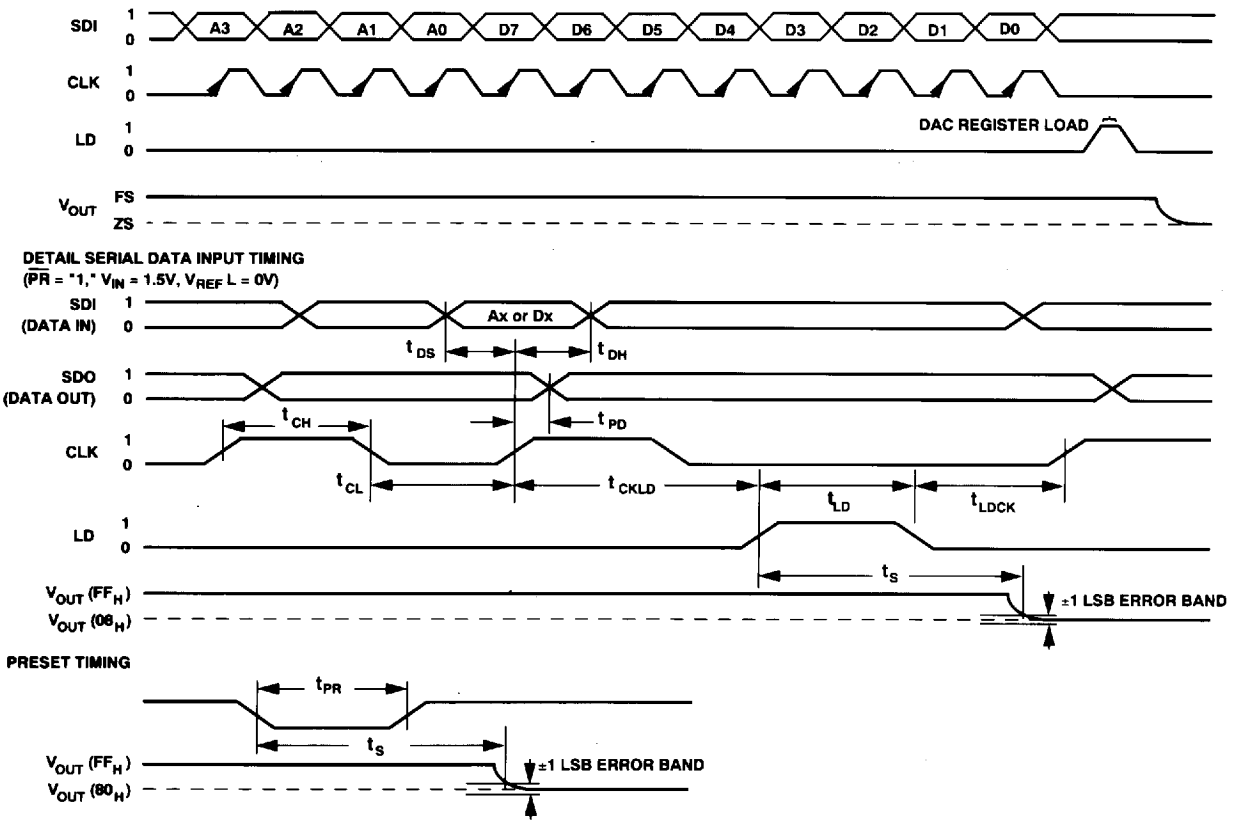


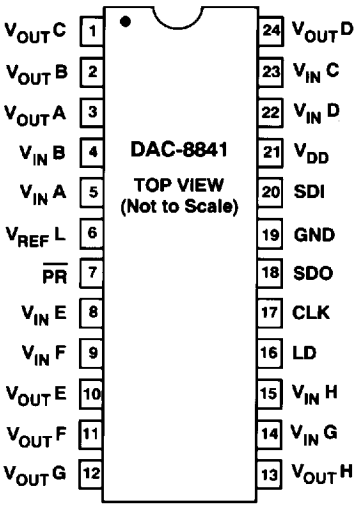
Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... −0.3 V, +7 V
V_{IN}X to GND ..... V_{DD}
V_{REF}L to GND ..... V_{DD}
V_{OUT}X to GND ..... V_{DD}
Short Circuit I_{OUT}X to GND ..... Continuous
Digital Input & Output Voltage to GND ..... V_{DD}
Operating Temperature Range
Extended Industrial: DAC-8841F ..... −40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J Max − T_A)/θ_{JA}
Thermal Resistance θ_{JA}
Cerdip ..... 64°C/W
P-DIP ..... 57°C/W
SOIC-24 ..... 70°C/W

PIN CONFIGURATIONS

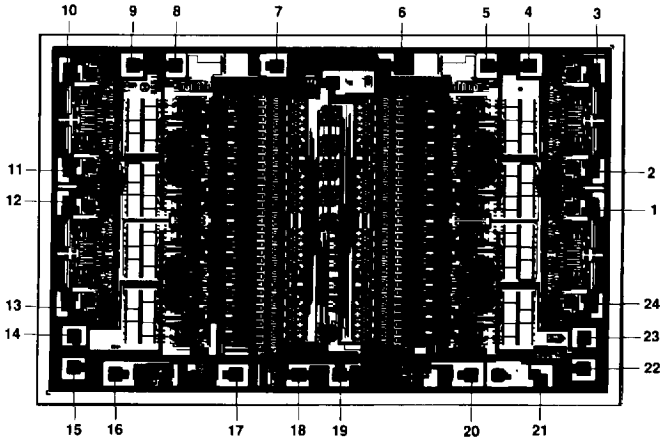


DAC-8841 PIN DESCRIPTION

Pin	Mnemonic	Description
1	V_{OUT}C	DAC C Output
2	V_{OUT}B	DAC B Output
3	V_{OUT}A	DAC A Output
4	V_{IN}B	DAC B Reference Input
5	V_{IN}A	DAC A Reference Input
6	V_{REF}L	DAC Input Reference Low
7	$\overline{PR}$	Preset Input, Active Low, All DAC Registers = 80_H
8	V_{IN}E	DAC E Reference Input
9	V_{IN}F	DAC F Reference Input
10	V_{OUT}E	DAC E Output
11	V_{OUT}F	DAC F Output
12	V_{OUT}G	DAC G Output
13	V_{OUT}H	DAC H Output
14	V_{IN}G	DAC G Reference Input
15	V_{IN}H	DAC H Reference Input
16	LD	Load DAC Register Strobe, Active High Input that Transfers the Data Bits from the Serial Input Register into the Decoded DAC Register. See Table I
17	CLK	Serial Clock Input, Positive Edge Triggered
18	SDO	Serial Data Output, Active Totem Pole Output
19	GND	Ground
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	V_{IN}D	DAC D Reference Input
23	V_{IN}C	DAC C Reference Input
24	V_{OUT}D	DAC D Output

DICE CHARACTERISTICS

DIE SIZE 0.117 × 0.185 inch, 21,645 sq. mils
(2.9718 × 4.699 mm, 13.964 sq. mm)
The die backside is electrically common to V_{DD}.



1. V_{OUT}C	13. V_{OUT}H
2. V_{OUT}B	14. V_{IN}G
3. V_{OUT}A	15. V_{IN}H
4. V_{IN}B	16. LD
5. V_{IN}A	17. CLK
6. V_{REF}L	18. SDO
7. PR	19. GND
8. V_{IN}E	20. SDI
9. V_{IN}F	21. V_{DD}
10. V_{OUT}E	22. V_{IN}D
11. V_{OUT}F	23. V_{IN}C
12. V_{OUT}G	24. V_{OUT}D

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

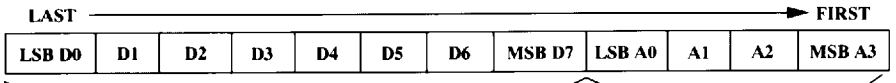


ORDERING GUIDE

Model	Temperature Range	Package Option
DAC8841FP	−40°C to +85°C	Plastic DIP
DAC8841FW	−40°C to +85°C	Cerdip
DAC8841FS	−40°C to +85°C	SOIC
DAC8841GBC	−25°C	Dice

For devices processed in total compliance to MIL-STD 883, contact your local sales office for the DAC8841BW/883 data sheet.

Table I. Serial Input Decode Table



MSB A3	A2	A1	LSB A0	DAC Updated
0	0	0	0	No Operation
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC C
0	1	0	0	DAC D
0	1	0	1	DAC E
0	1	1	0	DAC F
0	1	1	1	DAC G
1	0	0	0	DAC H
1	0	0	1	No Operation
⋮				⋮
1	1	1	1	No Operation

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	DAC Output Voltage VOUT = D/128 (VIN – VREFL) + VREFL
0	0	0	0	0	0	0	0	VREFL
0	0	0	0	0	0	0	1	1/128 (VIN – VREFL) + VREFL
				⋮				⋮
0	1	1	1	1	1	1	1	127/128 (VIN – VREFL) + VREFL
1	0	0	0	0	0	0	0	VIN (Preset Value)
1	0	0	0	0	0	0	1	129/128 (VIN – VREFL) + VREFL
				⋮				⋮
1	1	1	1	1	1	1	0	254/128 (VIN – VREFL) + VREFL
1	1	1	1	1	1	1	1	255/128 (VIN – VREFL) + VREFL

Table II. Logic Control Input Truth Table

SDI	CLK	LD	$\overline{PR}$	Input Shift Register Operation
X	L	L	H	No Operation
X		L	H	Shift One Bit In from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	X	L	L	All DAC Registers = 80_H
X	L	H	H	Load Serial Register Data into DAC(X) Register

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

DAC-8841—Typical Performance Characteristics

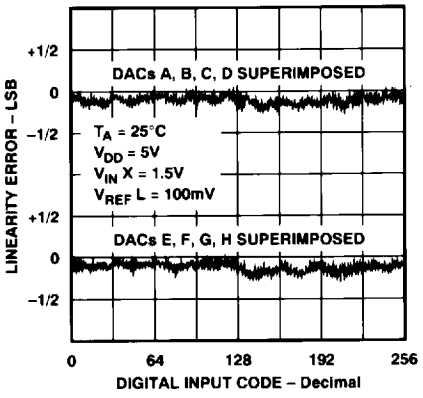


Figure 2. Linearity Error vs. Digital Input Code

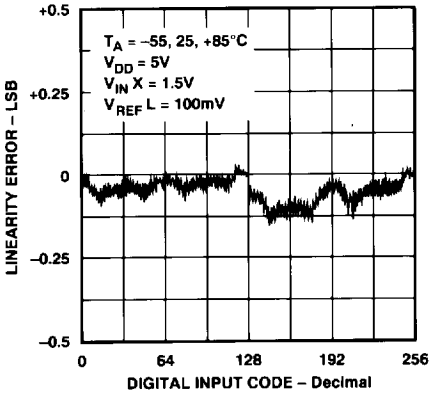


Figure 3. Linearity Error vs. Digital Code vs. Temperature

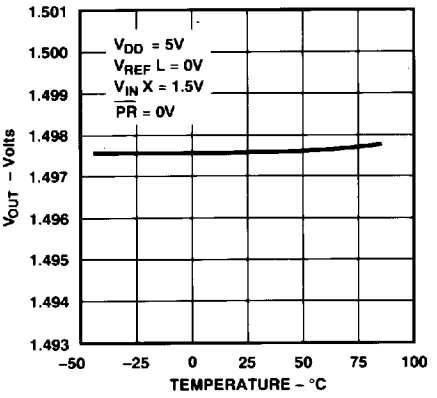


Figure 4. Half Scale vs. Temperature

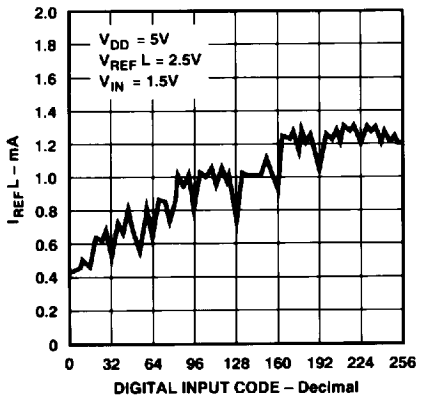


Figure 5. I_{REF}L Input Current vs. Digital Code

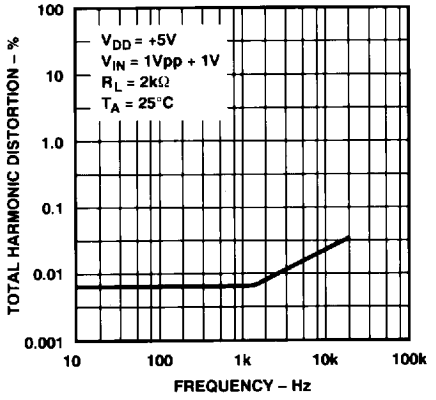


Figure 6. Total Harmonic Distortion vs. Frequency

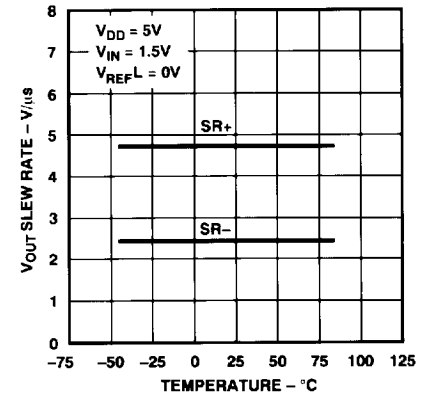


Figure 7. V_{OUT} Slew Rate vs. Temperature

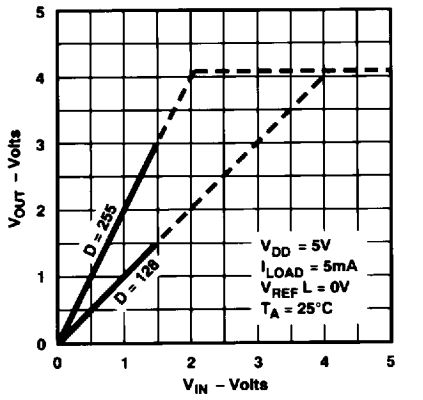


Figure 8. Full-Scale Output to Positive Saturation

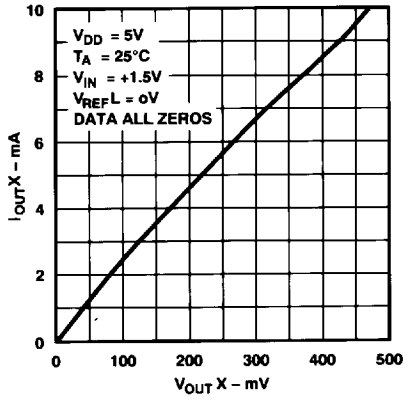


Figure 9. Zero-Scale Output Detail

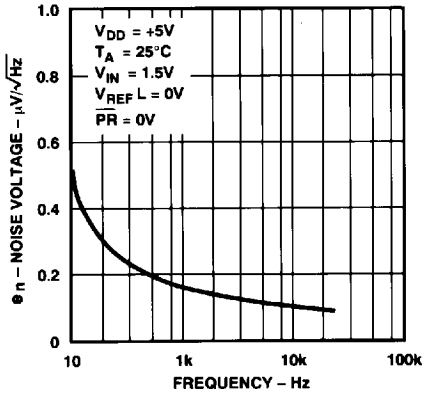


Figure 10. Voltage Noise Density vs. Frequency

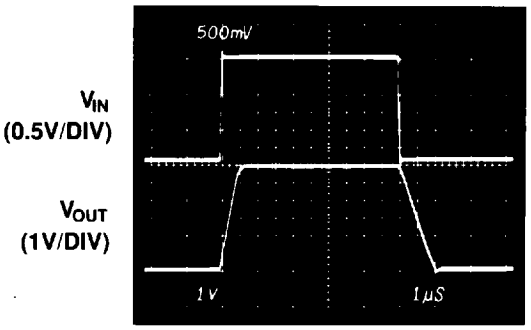


Figure 11. Pulse Response

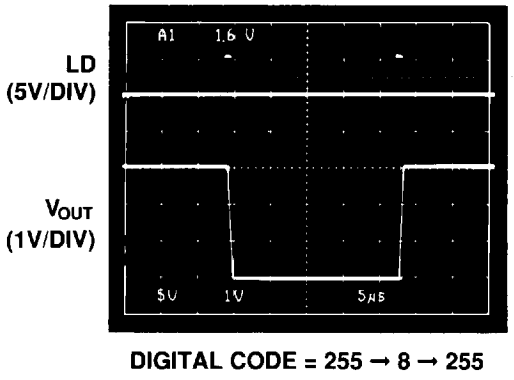


Figure 12. Settling Time

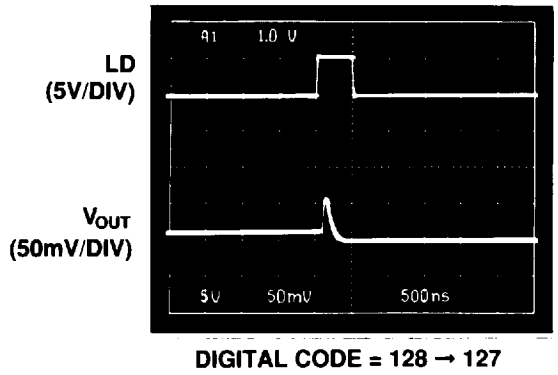


Figure 13. Worst Case 1 LSB Digital Step Change

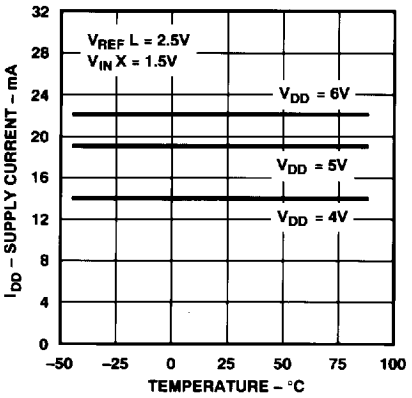


Figure 14. Supply Current vs. Temperature

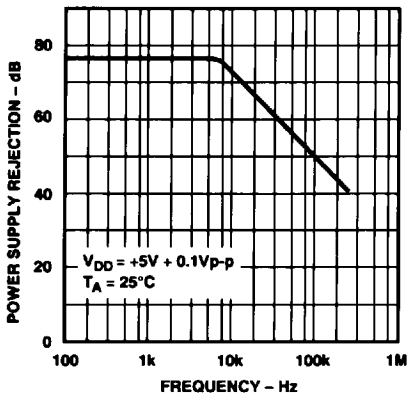


Figure 15. PSRR vs. Frequency

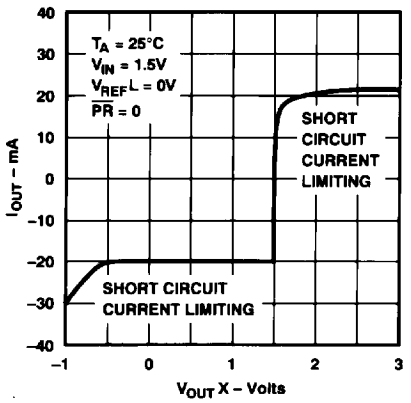


Figure 16. DAC Output Current vs. $V_{OUT}X$

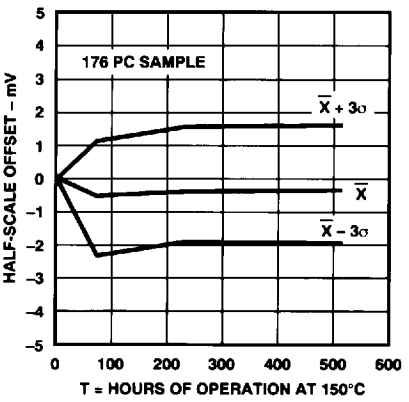


Figure 17. Output Drift Delta Accelerated by Burn-In

CIRCUIT OPERATION

The DAC-8841 is a general purpose multiple-channel ac or dc signal level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 5 mA of drive current to drive external loads. The DAC and amplifier combination shown in Figure 18 produces two-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition the DAC-8841 provides a 1 MHz gain-bandwidth product in the two-quadrant multiplying channel. Operating from a 5 V power supply, analog inputs to +1.5 V which generate outputs to +3 V are easily accommodated.

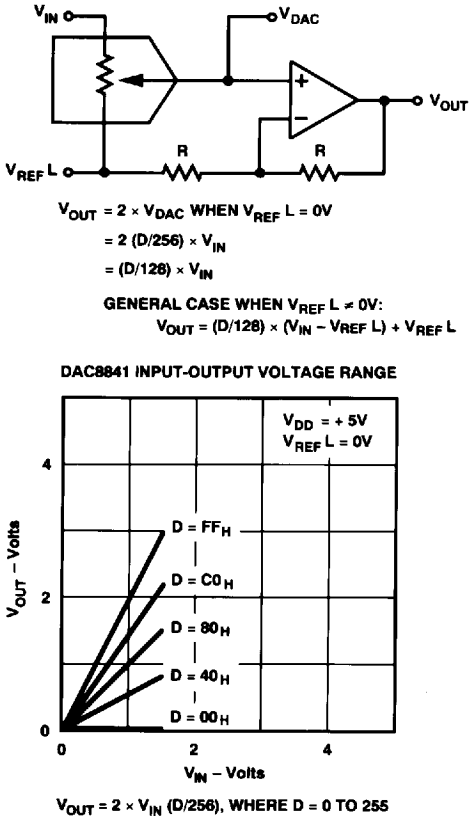


Figure 18. DAC Plus Amplifier Combine to Produce Two-Quadrant Multiplication

In order to be easy to use with a controlling microprocessor, a simple layout-efficient three-wire serial data interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pin make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8-bits of data. Using this combination, any DAC register can be changed without disturbing the other devices. A serial data output (SDO) pin simplifies cascading multiple DAC-8841s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to equal half-scale. The transfer equation (1) shows that in the preset condition (80_H) that V_{OUT} will equal V_{IN}. The asynchronous $\overline{PR}$ input pin can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start for general purpose adjustment applications.

ADJUSTING AC OR DC SIGNAL LEVELS

The two-quadrant multiplication operation of the DAC-8841 is shown in Figure 18. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128) \times (V_{IN} - V_{REF}L) + V_{REF}L \qquad (1)$$

where D is a decimal number between 0 and 255.

The actual output voltages generated with a fixed 1.5 V dc input on V_{IN} and $V_{REF}L$ = 0 V are summarized in this table.

Decimal Input (D)	$V_{OUT}(D)$	Comments (V_{IN} = 1.5 V, $V_{REF}L$ = 0 V)
0	0.000 V*	Zero Scale
1	0.012*	
2	0.024*	
127	1.488	
128	1.500	Half Scale = V_{IN}
129	1.512	
254	2.976	
255	2.988	Full Scale (FS) ≈ 2 × V_{IN}

*See "Operation Near Ground."

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal two times the input voltage. This is a result of the R-2R ladder DAC chosen. When the DAC register is loaded with 0, the output is $V_{REF}L$. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the DAC-8841. The actual voltage error would be ±0.012 V.

Operation Near ground – The input stage of the internal buffer amplifier functions down to ground, but the output stage cannot pull lower than the internal ground voltage. When a DAC output tries to output a voltage at or below the internal ground potential, it saturates and appears like a 50 Ω resistor to ground. The typical saturation voltage appearing at the output is 20 mV, see Figure 9. The 100 mV worst case zero-scale voltage specification reflects this saturation effect, including the worst case anticipated variation of the internal ground resistances, quiescent currents and buffer sinking current. Linearity is measured between code 8_{10} and code 255_{10} to avoid this saturation effect. In summary, the transfer function of each DAC will be a straight line from code 8 to code 255 when $V_{REF}L$ = 0 V. For input codes 0 to 7, some DAC outputs will be saturated in the zero-scale output voltage region; therefore, changing digital code 0 to 1 may not change the output voltage when $V_{REF}L$ = 0 V.

SIGNAL INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a code dependent input resistance whose worst case minimum value is specified in the electrical characteristics table. Use a suitable amplifier capable of driving this input resistance in parallel with the specified input capacitance. These reference inputs are designed to receive not only dc, but ac input voltages. This results from the incorporation of a true bilateral analog switch in the DAC design, see Figure 19. The DAC switch operation has been designed to operate in the break-before-make format to minimize transient loading of the inputs. The reference input voltage range can operate from ground (GND) to 1.5 V. That is, the operating input voltage range, when $V_{REF}L$ = 0 V, is:

$$0\ V < V_{IN}X < 1.5\ V \quad (2)$$

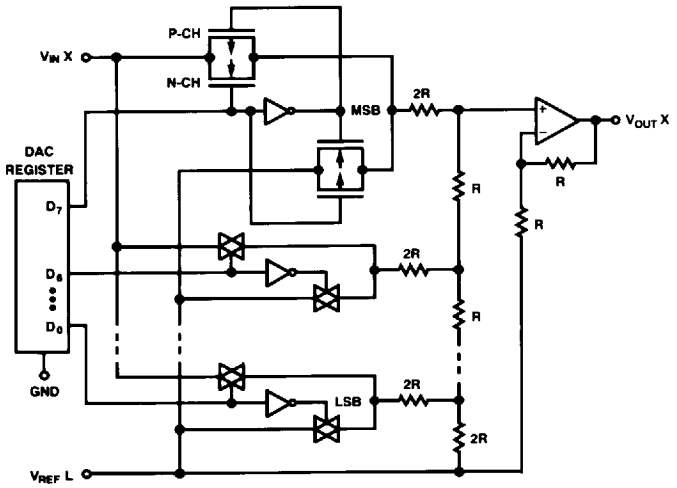


Figure 19. DAC-8841 TrimDAC Equivalent Circuit (One Channel)

The reference inputs can withstand input voltages up to V_{DD}; however due to the internal amplifier's gain of two configuration, the output voltage of the circuit reaches its maximum specified value of 3 V when the input voltage equals 1.5 V and $V_{REF}L$ = 0 V; see Figure 18.

The reference low input $V_{REF}L$ is the bottom end of the DAC (see Figure 18). This input is normally tied to ground; however it can be biased above ground. When $V_{REF}L$ is biased above ground, its value and that of $V_{IN}X$ should be chosen in agreement with Equation 3.

$$V_{OUT} \leq V_{DD} - 2\ V \quad (3)$$

Also for the general case the headroom restriction to V_{DD} for $V_{IN}X$ and $V_{REF}L$ is given by Equation 4.

$$V_{IN}X,\ V_{REF}L \leq V_{DD} - 2\ V \quad (4)$$

According to the above equations, the DAC-8841 can only be operated under certain combinations of $V_{IN}X$ and $V_{REF}L$. The shaded area in Figure 20 defines the theoretical allowable ranges of operation. Note that $V_{REF}L$ can be biased higher than $V_{IN}X$. Linearity will vary with the reference voltages and supply conditions. If a symmetrical output ac signal is desired, then the symmetrical ac input on $V_{IN}X$ should be offset to $V_{REF}L$. The output signal will then be with respect to $V_{REF}L$.

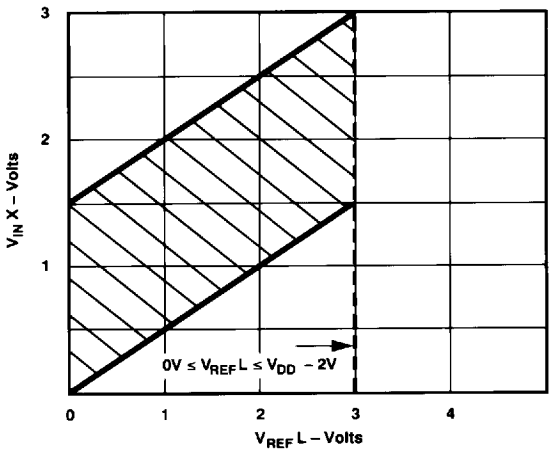


Figure 20. DAC-8841 Input Voltage Operating Boundaries

For example, biasing $V_{REF}L$ equal to one volt would accept a 1 V p–p ac input signal on V_{IN}. This input signal could then be attenuated or given a gain-of-two depending on the DAC data setting.

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the DAC-8841s internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 200 pF. However in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation. See Figure 16 "DAC output current versus V_{OUT}X" graph.

The amplifier output is guaranteed to operate to within 2 V of V_{DD} under all load conditions and temperature. Figure 8 shows typical operation to positive output saturation with a 5 mA load.

The low output impedance of the buffers minimizes crosstalk between analog input channels. At 100 kHz 70 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 μF ceramic in parallel with a 1–10 μF tantulum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, $\overline{PR}$) of the DAC-8841 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several DAC-8841s.

The Logic Control Input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive edge-sensitive input. If mechanical switches are used for breadboard, product evaluation they should be debounced by a flipflop or other suitable means.

The required address plus data input format is defined in the Serial Input Decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the DAC-8841 when the active high load strobe LD is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. It takes 12 clocks on the CLK

pin to fully load the serial input shift register. Data on the SDI input pin is subject to the timing diagram (Figure 1) data setup and data hold time requirements. After the twelfth clock pulse, the processor needs to activate the LD strobe to have the DAC-8841 decode the serial register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are in the electrical characteristic table and in the Figure 1 timing diagram. After twelve clock edges data initially loaded into the shift register at SDI appears at the shift register output SDO.

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels.

Figure 21 shows a three-wire interface for a single DAC-8841 that easily cascades for multiple packages.

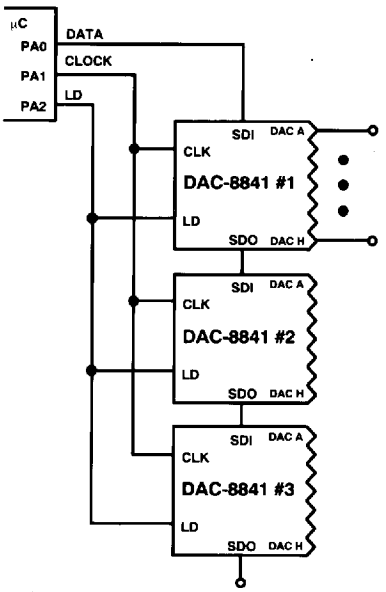


Figure 21. Three-Wire Interface

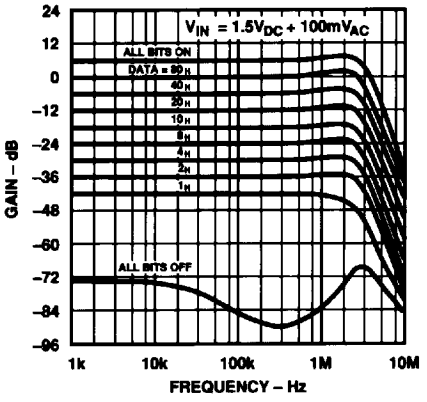


Figure 22. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency