TEXAS INSTRUMENTS

AMC1300B-Q1

SBASA40 – APRIL 2020

AMC1300B-Q1 Precision, ±250-mV Input, Reinforced Isolated Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C, T_A
- ±250-mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift:
  - ±0.2 mV (max), ±3 µV/°C (max)
- Fixed gain: 8.2
- Very low gain error and drift:
  - ±0.3% (max), ±50 ppm/°C (max)
- Low nonlinearity and drift: 0.03%, 1 ppm/°C (typ)
- 3.3-V operation on high-side
- System-level diagnostic features
- Safety-related certifications:
  - 7071-V_{PK} reinforced isolation per DIN VDE V 0884-11: 2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL1577
- High CMTI: 140 kV/µs (typ)

2 Applications

- Shunt-resistor-based current sensing in:
  - HEV/EV on-board chargers (OBC)
  - HEV/EV DC/DC converters
  - HEV/EV traction inverters

3 Description

The AMC1300B-Q1 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the AMC1300B-Q1 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings and, especially in traction inverters, accurate torque control. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1300B-Q1 simplify system-level design and diagnostics.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1300B-Q1	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

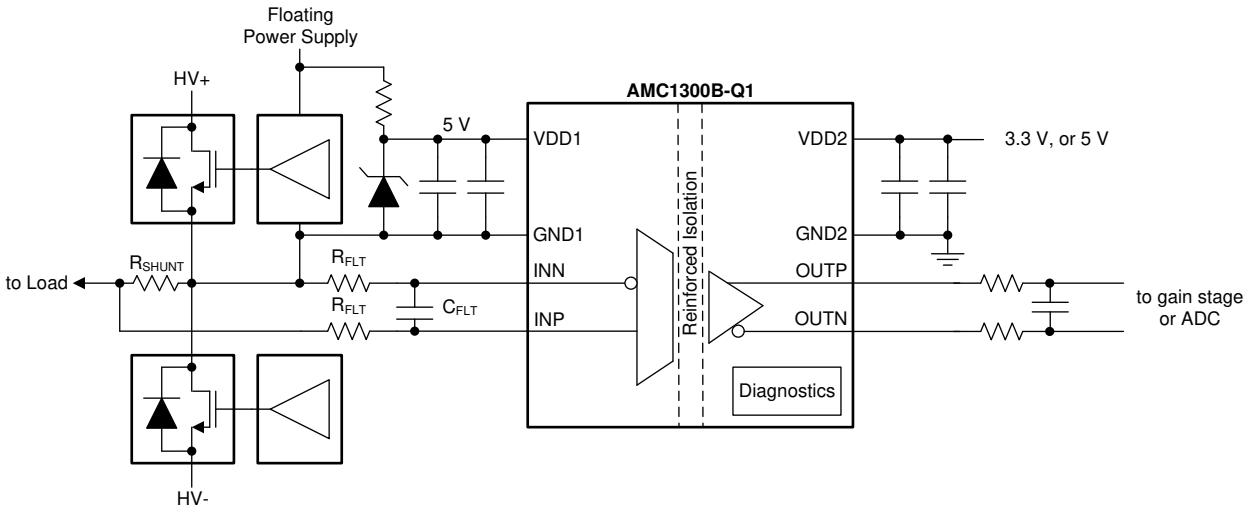


Table of Contents

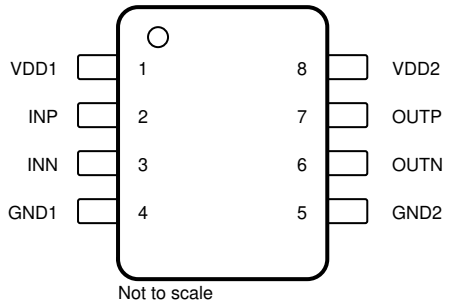
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2020	*	Initial release.

5 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	—	High-side power supply, 3.0 V to 5.5 V, relative to GND1. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
2	INP	I	Noninverting analog input
3	INN	I	Inverting analog input
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	OUTN	O	Inverting analog output
7	OUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	High-side power supply	VDD1 to GND1	3.0	5	5.5	V
	Low-side power supply	VDD2 to GND2	3.0	3.3	5.5	V
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
	Absolute common-mode input voltage(1)	$(V_{INP} + V_{INN}) / 2$ to GND1	–2		VDD1	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	–0.16		VDD1 – 2.1	V
T_A	Specified ambient temperature		–40		125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in *Absolute Maximum Ratings*.

6.4 Thermal Information

THERMAL METRIC(1)		AMC1300B-Q1 DWV (SOIC) 8 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
R_{qJB}	Junction-to-board thermal resistance	43.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	4.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (P_{D1} + P_{D2})	VDD1 = VDD2 = 5.5 V		65.5	98.45	mW
		VDD1 = VDD2 = 3.6 V		40.17	56.52	
P_{D1}	Maximum power dissipation (high-side) VDD1 = 5.5 V	VDD1 = 5.5 V		36	53.9	mW
		VDD1 = 3.6 V		22.68	30.6	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V		29.5	44.55	mW
		VDD2 = 3.6 V		17.49	25.92	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); see Figure 4	1500	V_{RMS}
		At DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8485	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7071 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	Certificate number: E181974

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	R_{qJA} = 85.4°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 2			266	mA
		R_{qJA} = 85.4°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 2			406	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C, see Figure 3			1463	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level	(V_{INP} + V_{INN}) / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			95		mV
V_{OS}	Input offset voltage(1)	Initial, at T_A = 25°C, INP = INN = GND1	–0.2	±0.01	0.2	mV
TCV_{OS}	Input offset drift(1)		–3	±1	3	uV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–98		
C_{IN}	Single-ended input capacitance(2)	INN = GND1, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance(2)	f_{IN} = 275 kHz		1		pF
R_{IN}	Single-ended input resistance(2)	INN = GND1		19		kΩ
R_{IND}	Differential input resistance(2)			22		kΩ
I_{IB}	Input bias current	INP = INN = GND1; I_{IB} = (I_{IBP} + I_{IBN}) / 2	–41	–30	–24	uA
TCI_{IB}	Input bias current drift			±1		nA/°C
I_{IO}	Input offset current	I_{IO} = I_{IBP} – I_{IBN}		±5		nA

(1) The typical value includes one sigma statistical variation.
(2) Also see the Analog Input section for more details.

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Nominal gain			8.2		
E_G	Gain error(1)	Initial, at T_A = 25°C	–0.3	0.05	0.3	%
TCE_G	Gain error drift(1)		-50	±15	50	ppm/°C
	Nonlinearity(1)		–0.03	±0.01	0.03	%
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	f_{IN} = 10 kHz		–85		dB
	Output noise	INP = INN = GND1, f_{IN} = 0 Hz, BW = 100 kHz brickwall filter		230		μV_{RMS}
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	80	85		dB
		f_{IN} = 10 kHz, BW = 100 kHz		72		
PSRR	Power-supply rejection ratio(3)	PSRR vs VDD1, at DC		–103		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–96		
		PSRR vs VDD2, at DC		–106		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–86		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{Failsafe}$	Failsafe differential output voltage	$V_{CM} \geq V_{CMov}$, or VDD1 missing		–2.6	–2.5	V
BW_{OUT}	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN		±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV	75	140		kV/µs
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	1.75	2.53	2.7	V
IDD1	High-side supply current	3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

(3) This parameter is input referred.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	See Figure 1		1.3		µs
t_f	Output signal fall time	See Figure 1		1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output, see Figure 1		1	1.5	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output, see Figure 1		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output, see Figure 1		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to VOUTP, VOUTN valid, 0.1% settling		500		µs

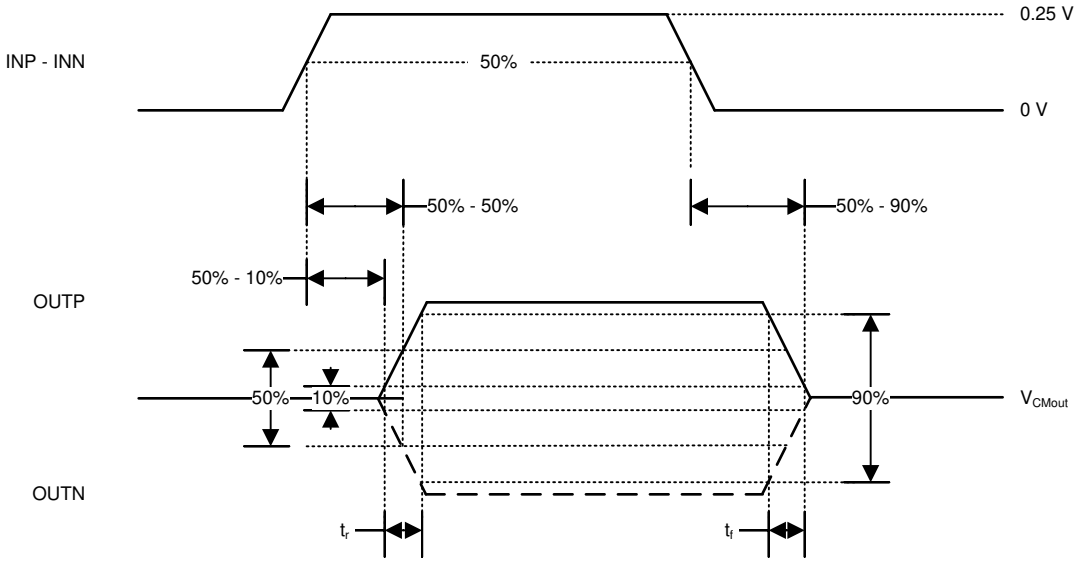


Figure 1. Rise, Fall, and Delay Time Waveforms

6.11 Insulation Characteristics Curves

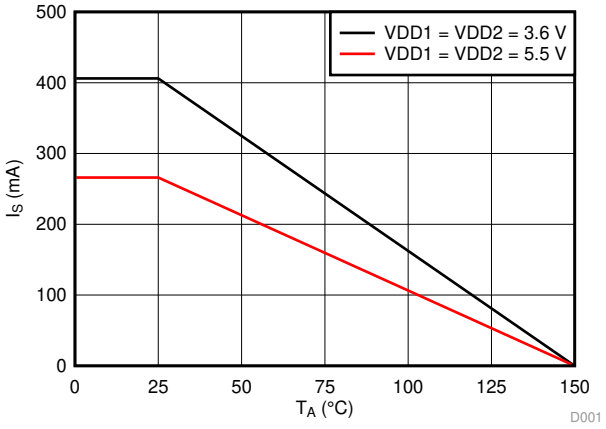


Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE

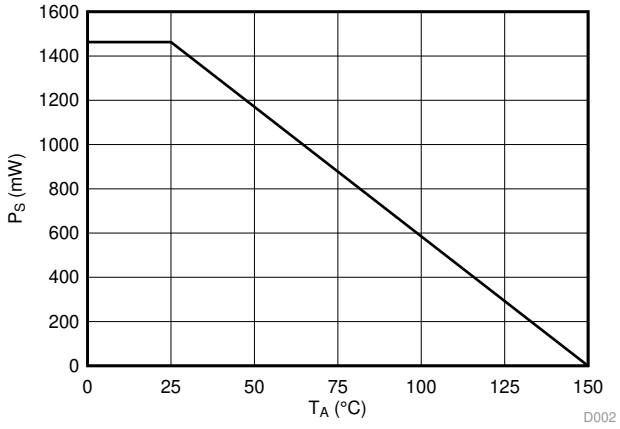
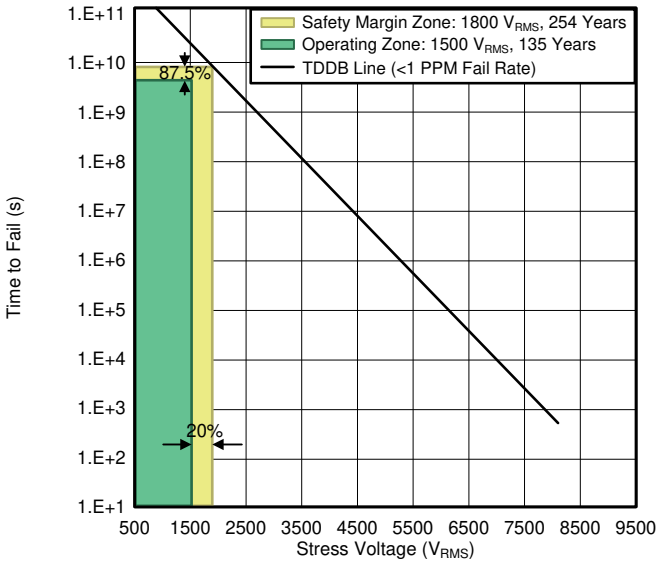


Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 year

Figure 4. Reinforced Isolation Capacitor Lifetime Projection

6.12 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

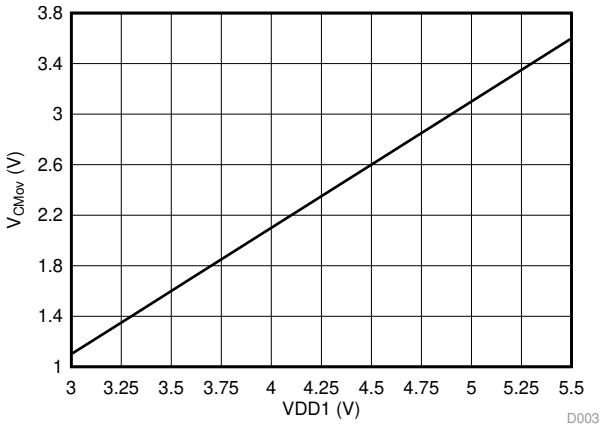


Figure 5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

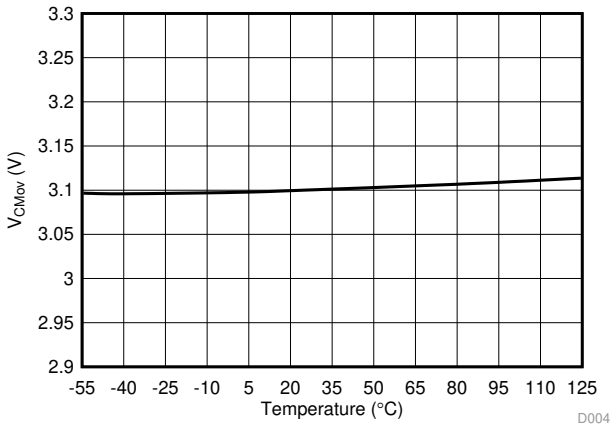


Figure 6. Common-Mode Overvoltage Detection Level vs Temperature

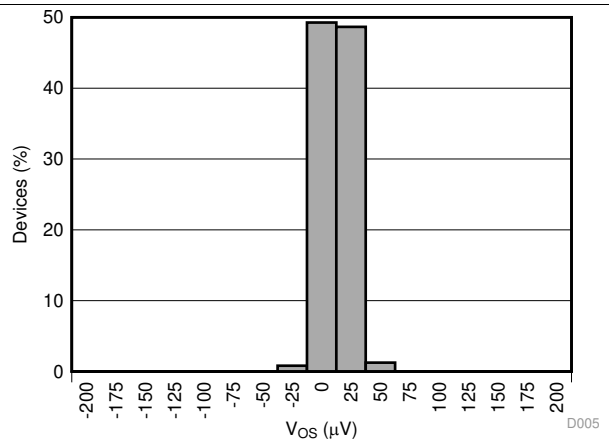


Figure 7. Input Offset Voltage Histogram

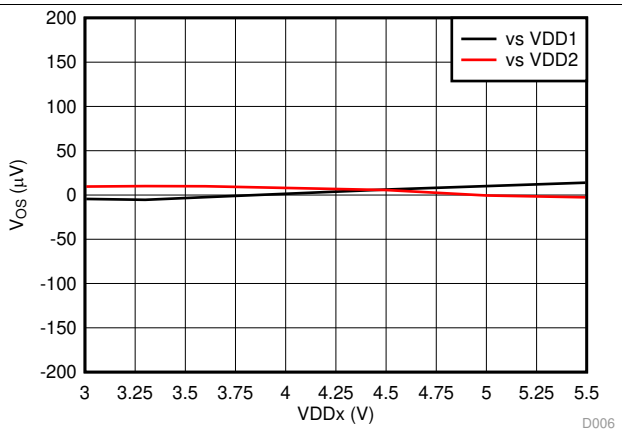


Figure 8. Input Offset Voltage vs Supply Voltage

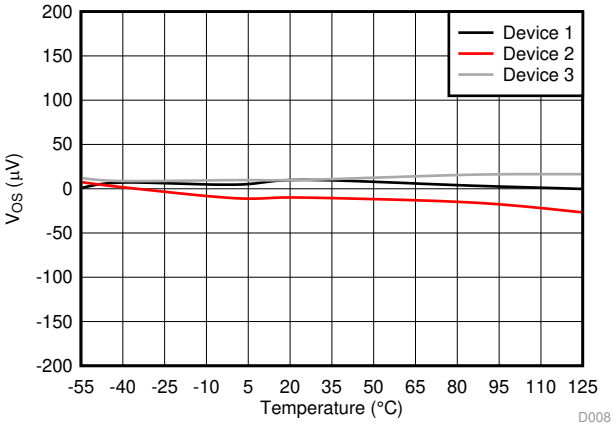


Figure 9. Input Offset Voltage vs Temperature

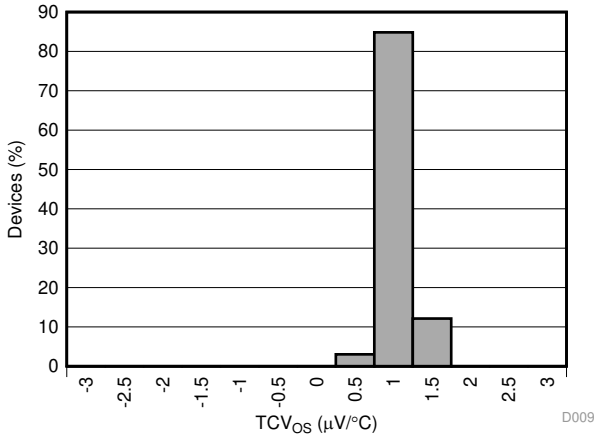


Figure 10. Input Offset Drift Histogram

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

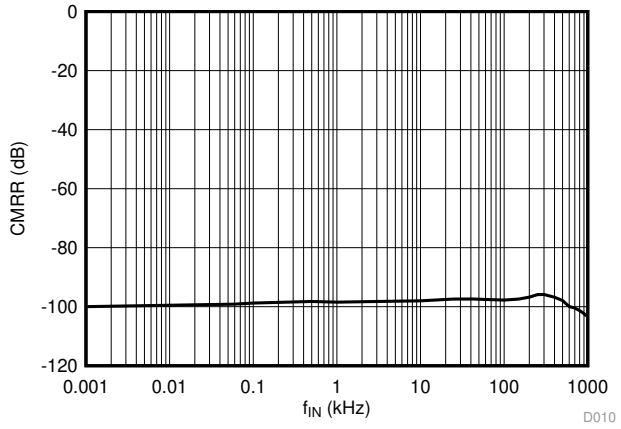


Figure 11. Common-Mode Rejection Ratio vs Input Frequency

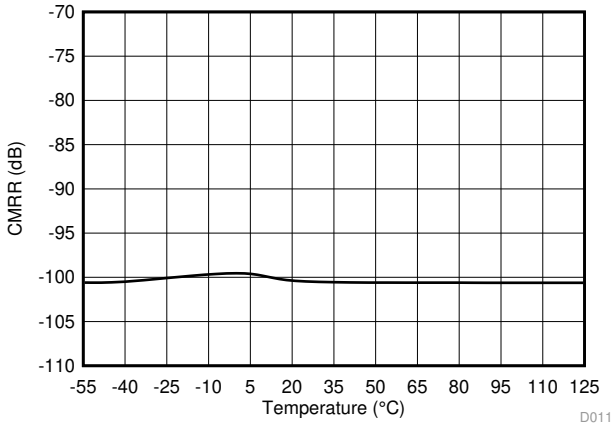


Figure 12. Common-Mode Rejection Ratio vs Temperature

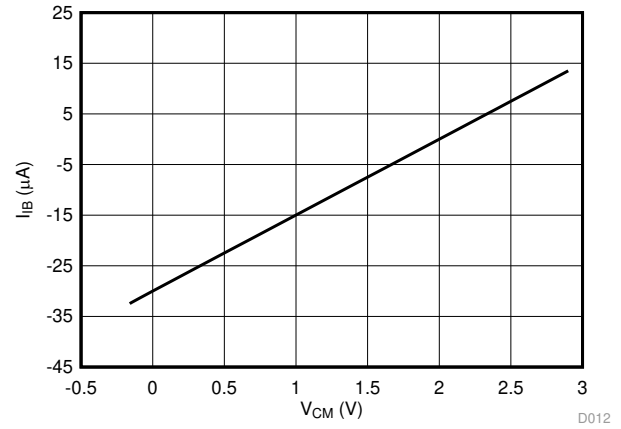


Figure 13. Input Bias Current vs Common-Mode Input Voltage

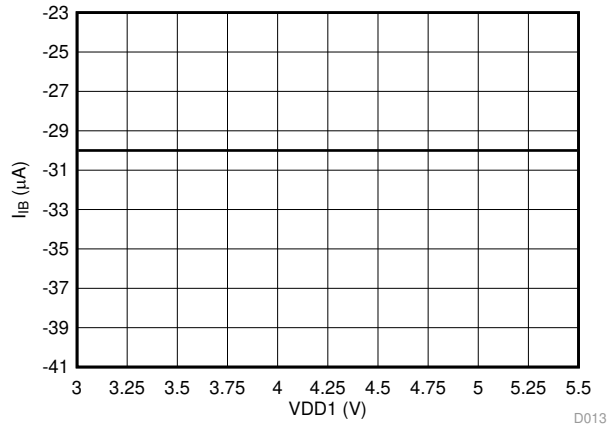


Figure 14. Input Bias Current vs High-Side Supply Voltage

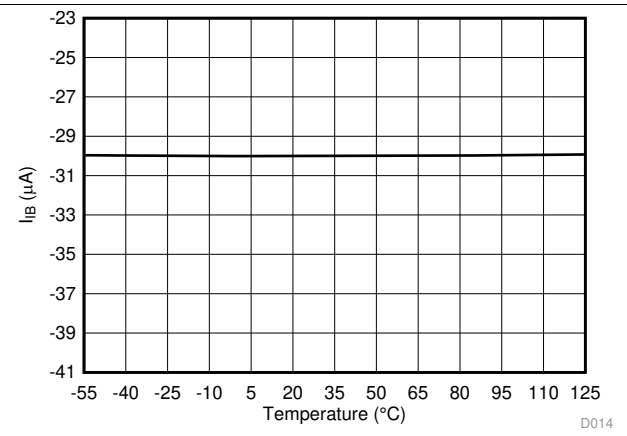


Figure 15. Input Bias Current vs Temperature

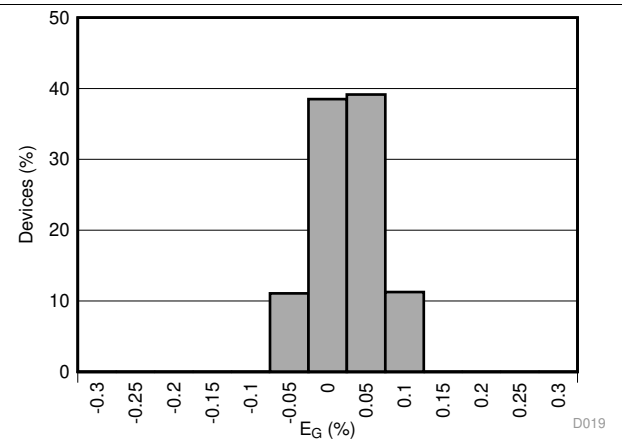


Figure 16. Gain Error Histogram

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

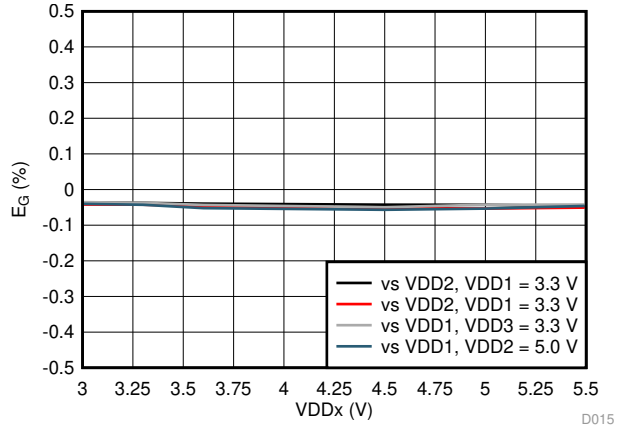


Figure 17. Gain Error vs Supply Voltage

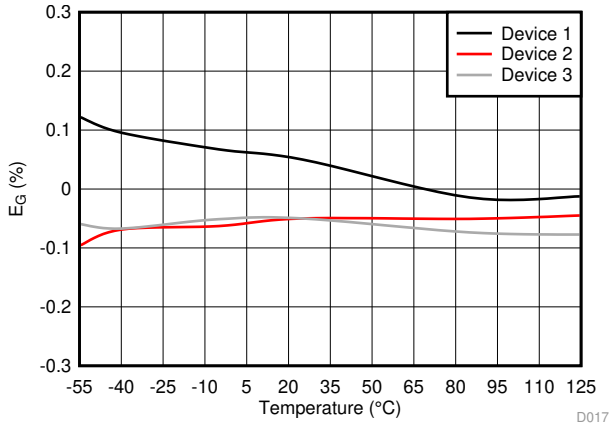


Figure 18. Gain Error vs Temperature

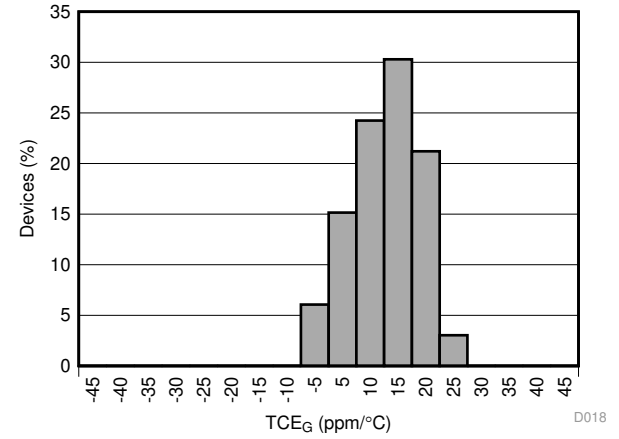


Figure 19. Gain Error Drift Histogram

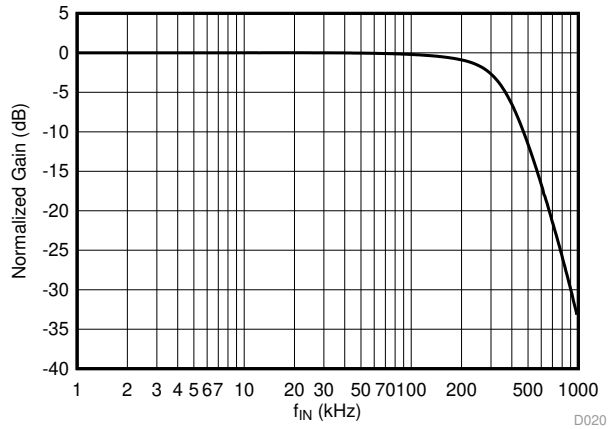


Figure 20. Normalized Gain vs Input Frequency

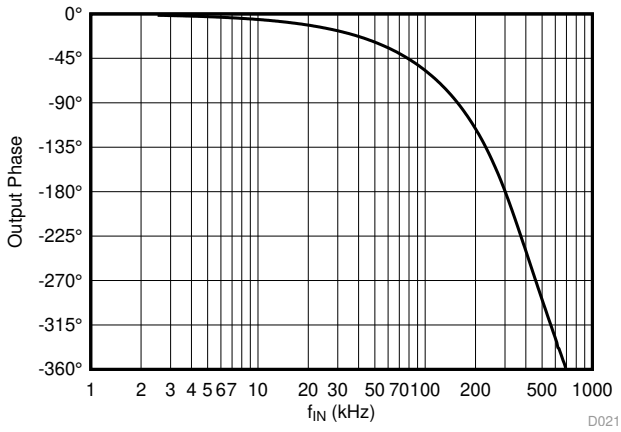


Figure 21. Output Phase vs Input Frequency

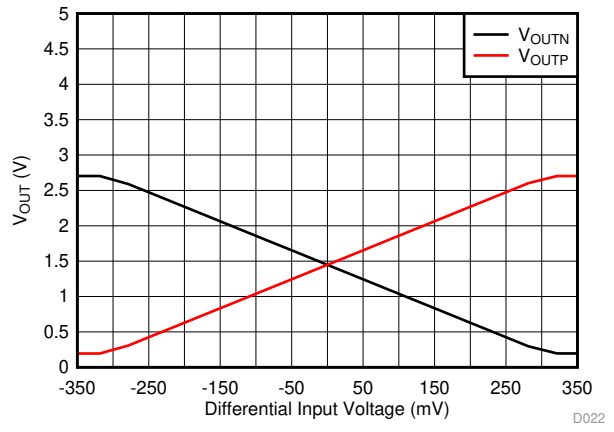


Figure 22. Output Voltage vs Input Voltage

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

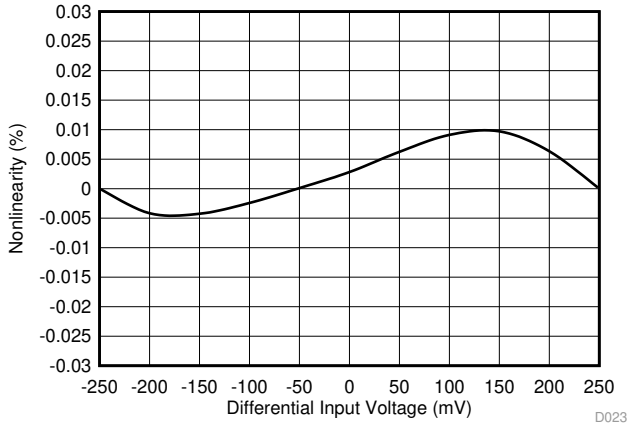


Figure 23. Nonlinearity vs Input Voltage

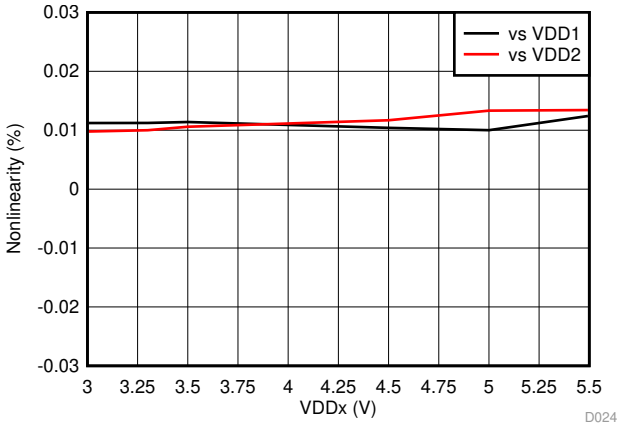


Figure 24. Nonlinearity vs Supply Voltage

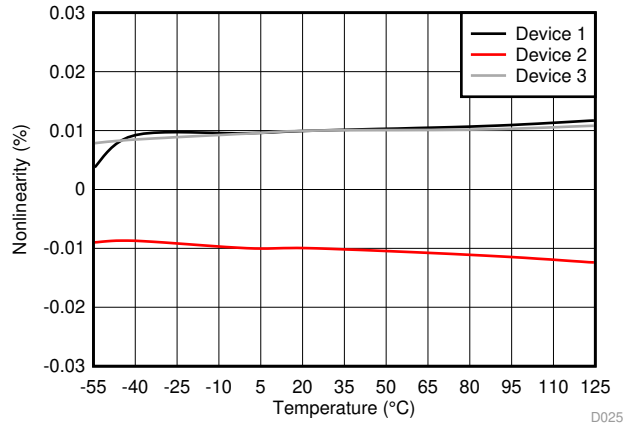


Figure 25. Nonlinearity vs Temperature

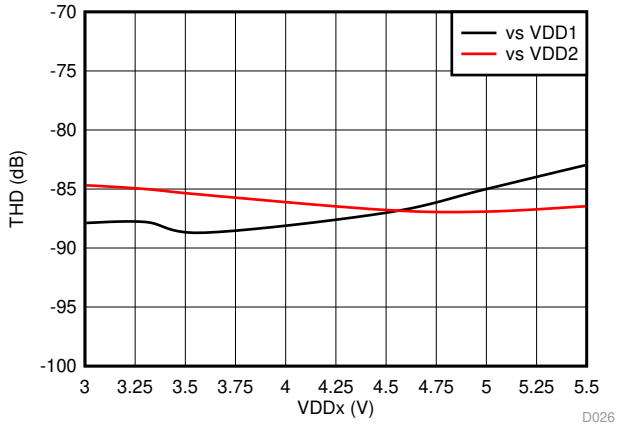


Figure 26. Total Harmonic Distortion vs Supply Voltage

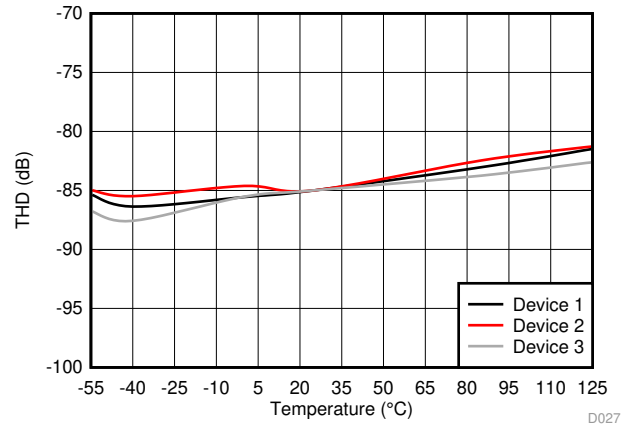


Figure 27. Total Harmonic Distortion vs Temperature

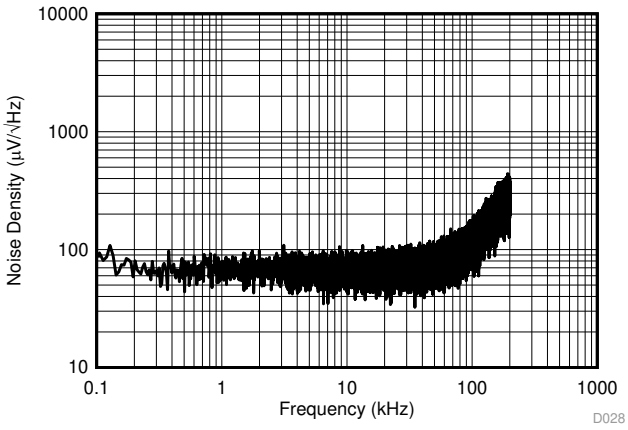


Figure 28. Input-Referred Noise Density vs Frequency

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

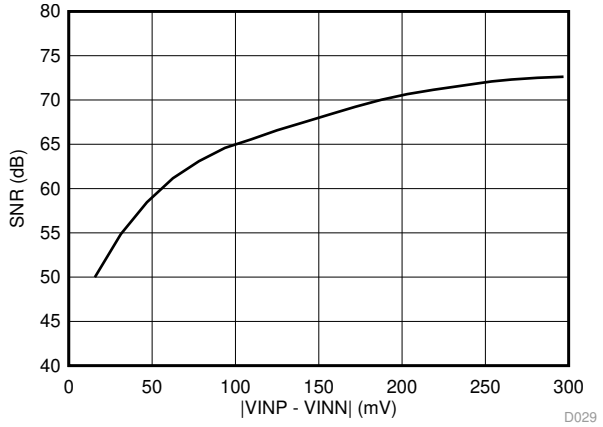


Figure 29. Signal-to-Noise Ratio vs Input Voltage

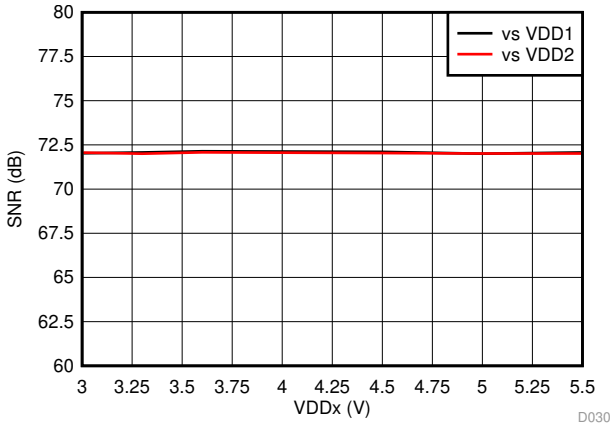


Figure 30. Signal-to-Noise Ratio vs Supply Voltage

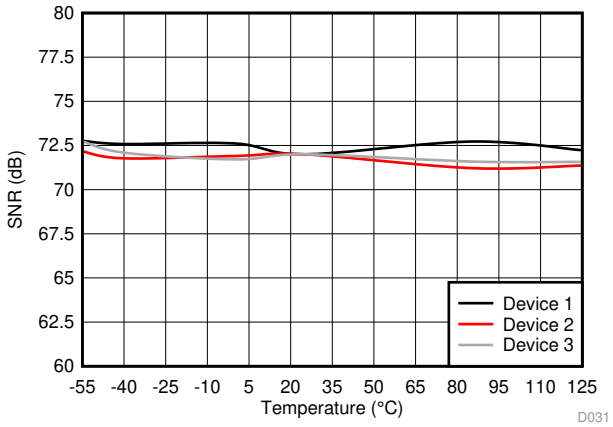


Figure 31. Signal-to-Noise Ratio vs Temperature

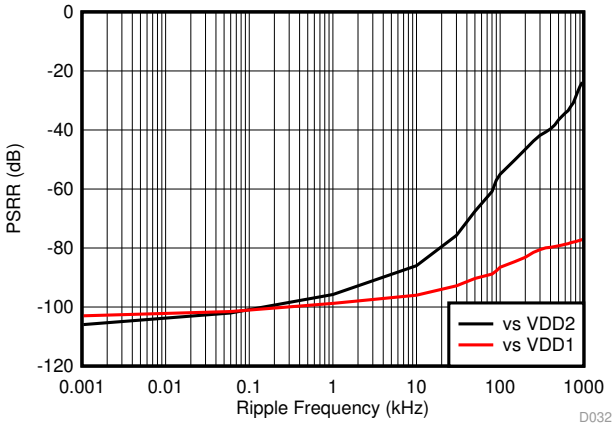


Figure 32. Power-Supply Rejection Ratio vs Ripple Frequency

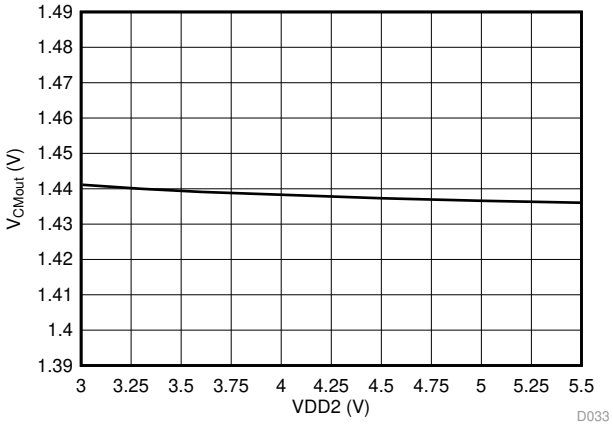


Figure 33. Output Common-Mode Voltage vs Low-Side Supply Voltage

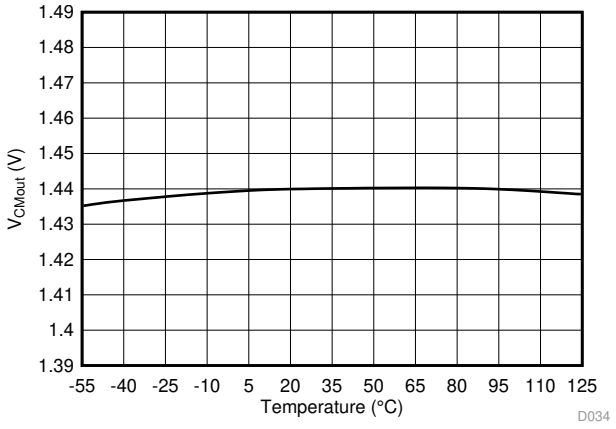


Figure 34. Output Common-Mode Voltage vs Temperature

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

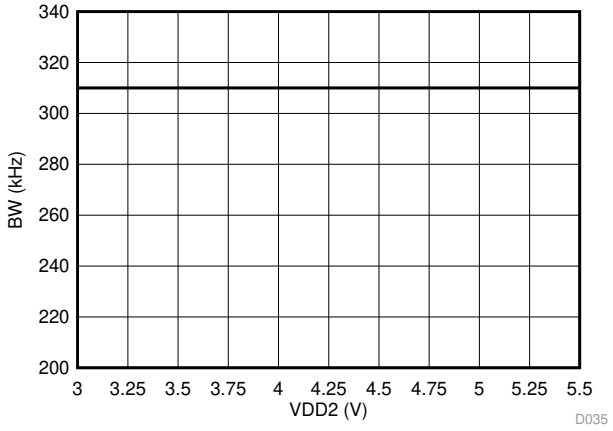


Figure 35. Output Bandwidth vs Low-Side Supply Voltage

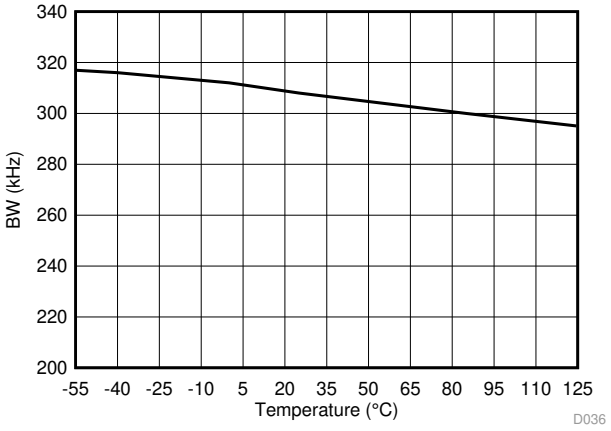


Figure 36. Output Bandwidth vs Temperature

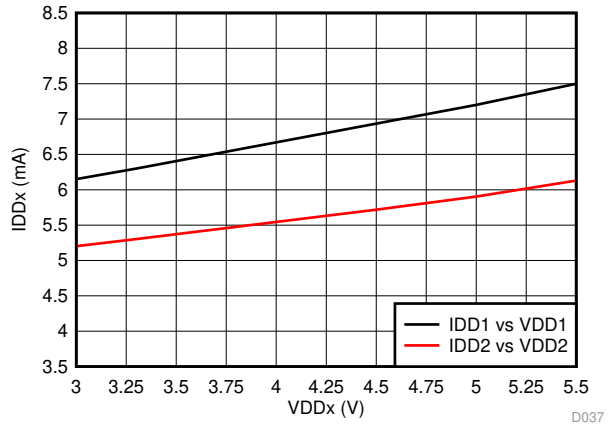


Figure 37. Supply Current vs Supply Voltage

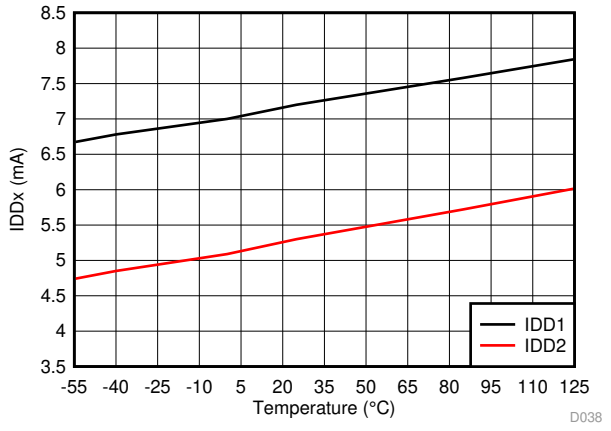


Figure 38. Supply Current vs Temperature

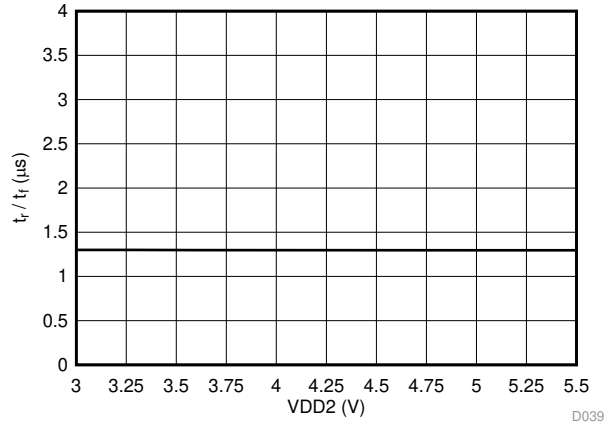


Figure 39. Output Rise and Fall Time vs Low-Side Supply

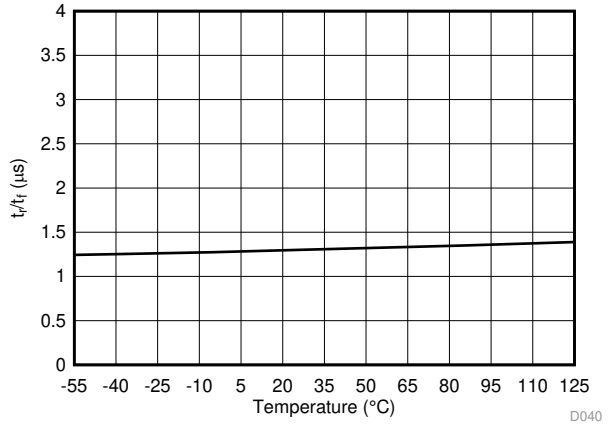


Figure 40. Output Rise and Fall Time vs Temperature

Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

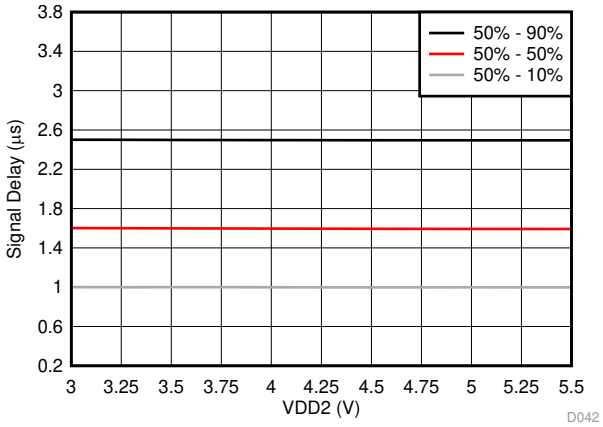


Figure 41. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

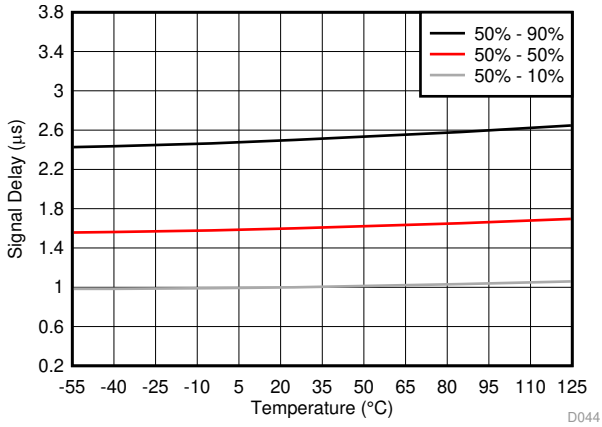


Figure 42. V_{IN} to V_{OUT} Signal Delay vs Temperature

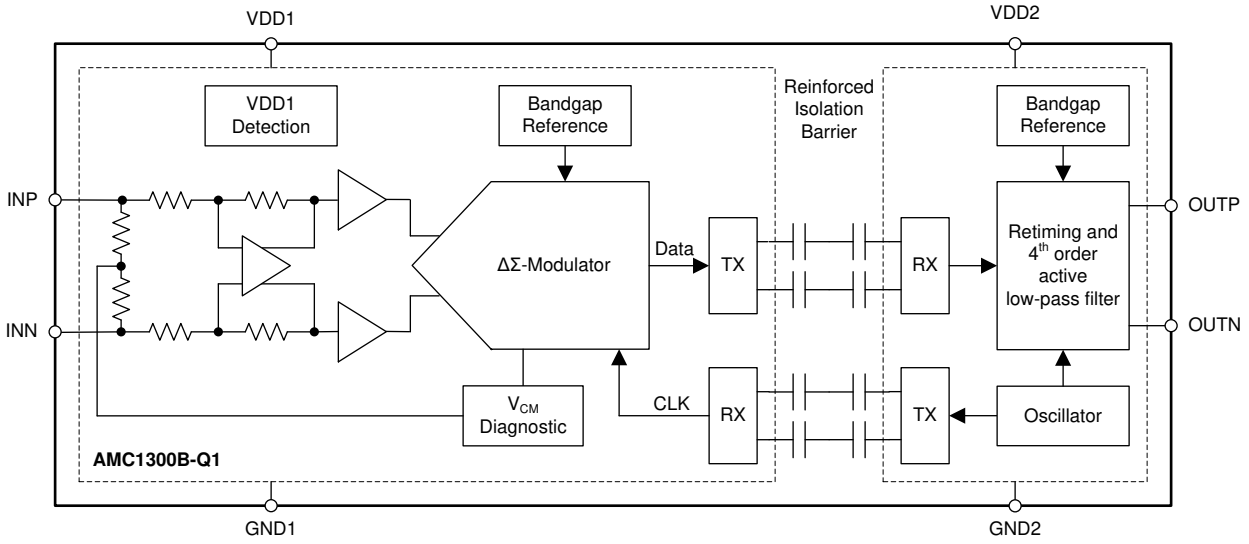
7 Detailed Description

7.1 Overview

The AMC1300B-Q1 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed, as shown in the *Functional Block Diagram*, by a fourth-order analog filter on the low-side and presented as a differential output of the device.

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the AMC1300B-Q1 and the isolation barrier characteristics result in high reliability and common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC1300B-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 kΩ. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (V_{INP} and V_{INN}). First, if the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

Feature Description (continued)

7.3.2 Isolation Channel Signal Transmission

The AMC1300B-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. As shown in Figure 43, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC1300B-Q1 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC1300B-Q1 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

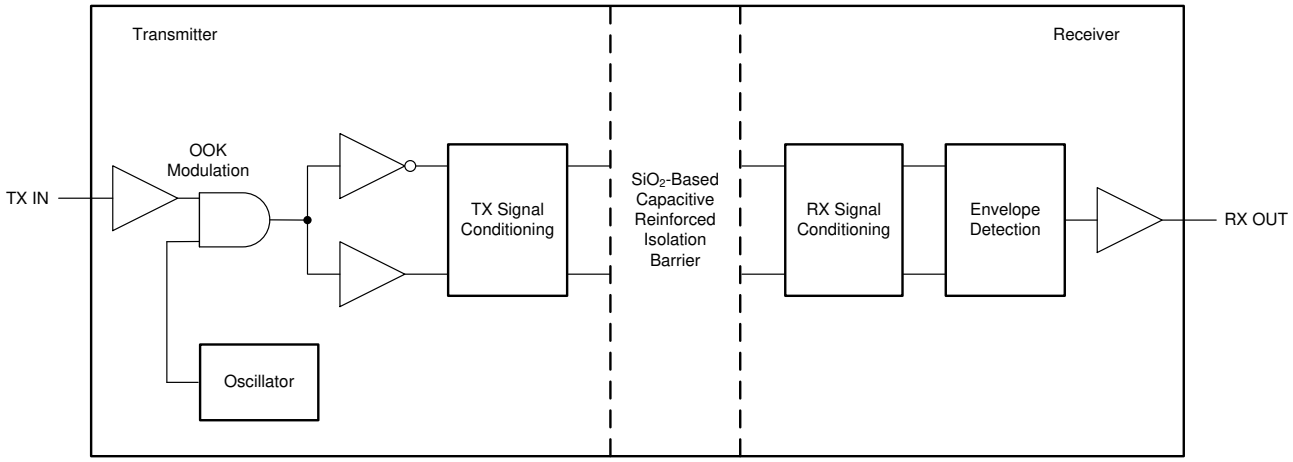


Figure 43. Block Diagram of an Isolation Channel

Figure 44 shows the concept of the OOK scheme.

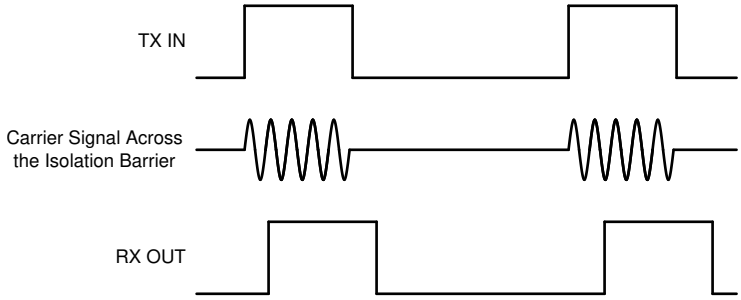


Figure 44. OOK-Based Modulation Scheme

Feature Description (continued)

7.3.3 Fail-Safe Output

The AMC1300B-Q1 offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the AMC1300B-Q1 is missing, or
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN}) / 2$, exceeds the minimum common-mode overvoltage detection level V_{CMov} of VDD1 – 2 V.

Figure 45 and Figure 46 show the fail-safe output of the AMC1300B-Q1 as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on a system level.

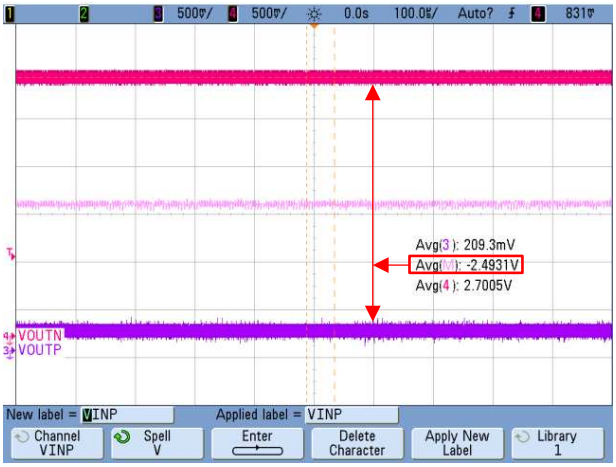


Figure 45. Typical Negative Clipping Output of the AMC1300B-Q1

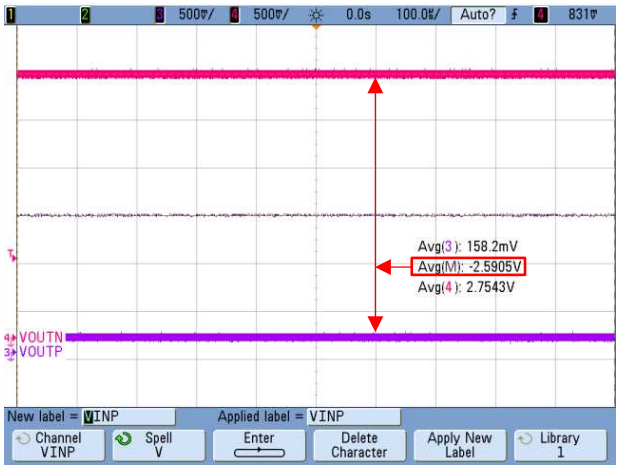


Figure 46. Typical Fail-Safe Output of the AMC1300B-Q1

7.4 Device Functional Modes

The AMC1300B-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table in the *Specifications* section.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC1300B-Q1 a high-performance solution for automotive applications where shunt-based current sensing with high common-mode voltage levels is required.

8.2 Typical Application

Isolated amplifiers are widely used in on-board chargers (OBC), DC/DC converters, and traction inverters. The input structure of the AMC1300B-Q1 is optimized for use with low-value shunt resistors in current sensing applications.

Figure 47 depicts a typical operation of the AMC1300B-Q1 for current sensing in a traction inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the AMC1300B-Q1 ensure reliable and accurate operation even in high-noise environments such as a traction inverter. The high-impedance input and wide input voltage range make the AMC1311-Q1 suitable for DC bus voltage sensing.

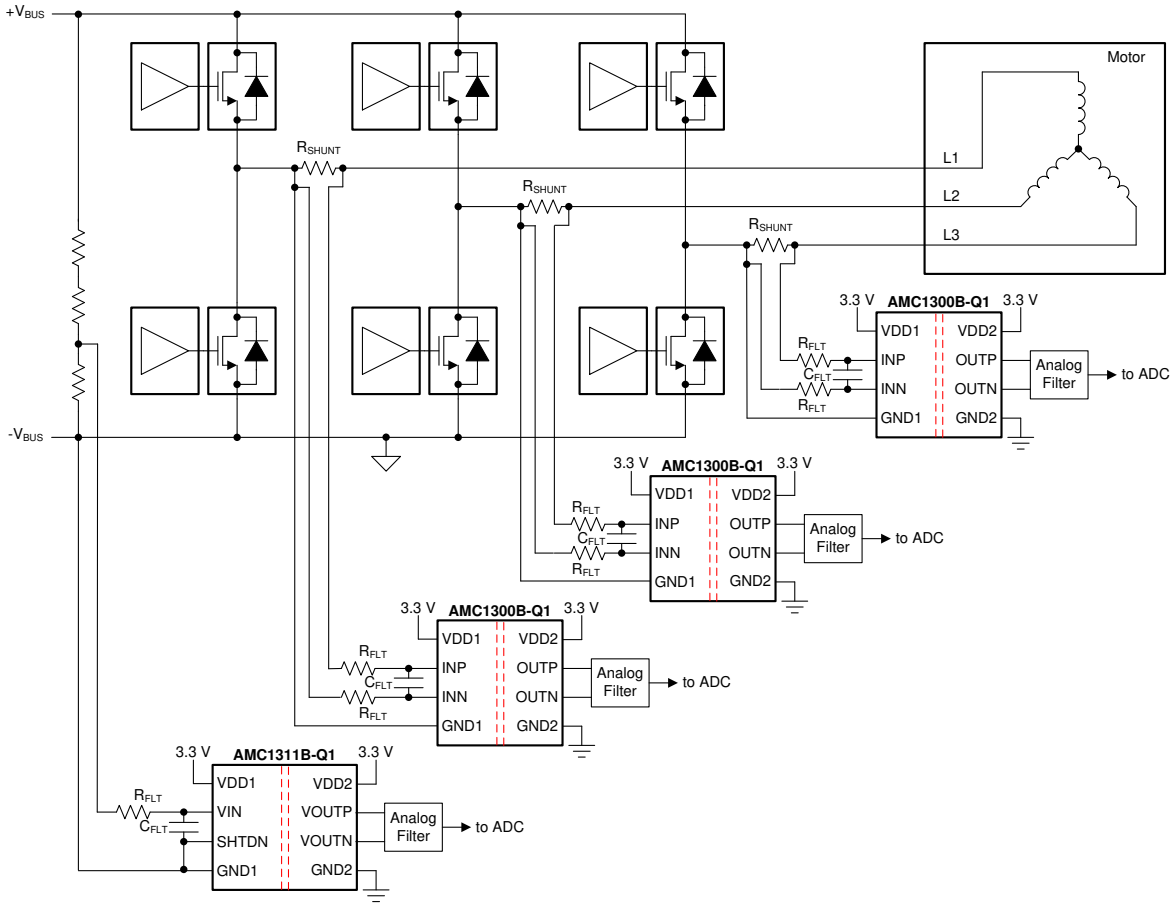


Figure 47. Using the AMC1300B-Q1 for Current Sensing in Traction Inverters

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

Table 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	± 250 mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	3 µs (maximum)

8.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the AMC1300B-Q1 is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1300B-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC1300B-Q1 device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For systems using single-ended input ADCs, Figure 48 shows an example of a TLV313-Q1-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

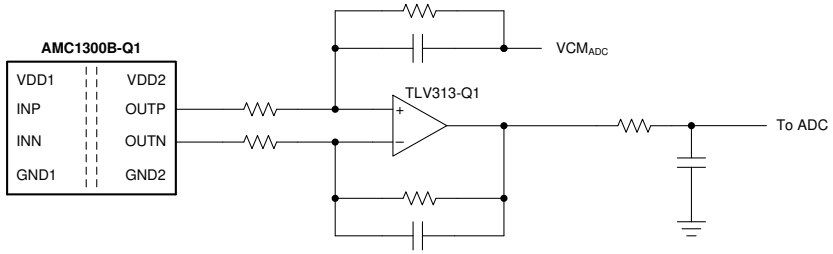


Figure 48. Connecting the AMC1300B-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curves

In traction inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. Figure 49 shows the typical full-scale step response of the AMC1300B-Q1. Consider the delay of the required window comparator and the micro contol unit (MCU) to calculate the overall response time of the system.

Figure 49. Step Response of the AMC1300B-Q1

The high linearity and low temperature drift of offset and gain errors of the AMC1300B-Q1, as shown in Figure 50, allow design of high-efficiency OBC systems with a high-performance power factor correction (PFC) stage.

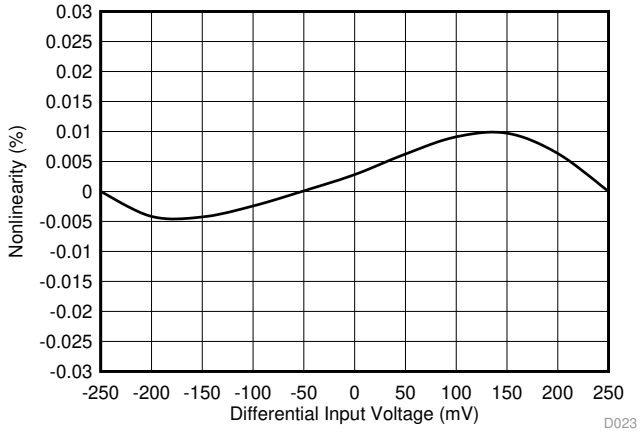


Figure 50. Typical Nonlinearity of the AMC1300B-Q1

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC1300B-Q1 unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 2 V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and the output functions as described in the *Fail-Safe Output* section, which may lead to an undesired reaction on the system level.

9 Power Supply Recommendations

In a typical traction inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5 V or 3.3 V± 10%. Alternatively, a low-cost low-dropout (LDO) regulator (for example, the LP2951-xx-Q1) may be used to minimize noise on the power supply. TI recommends a low-ESR decoupling capacitor of 0.1 µF to filter this power-supply path. Place this capacitor (C2 in Figure 51) as close as possible to the VDD1 pin of the AMC1300B-Q1 for best performance. If better filtering is required, an additional 2.2-µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt.

To decouple the low-side power supply on the controller side, use a 0.1-µF capacitor placed as close to the VDD2 pin of the AMC1300B-Q1 as possible, followed by an additional capacitor from 1 µF to 10 µF.

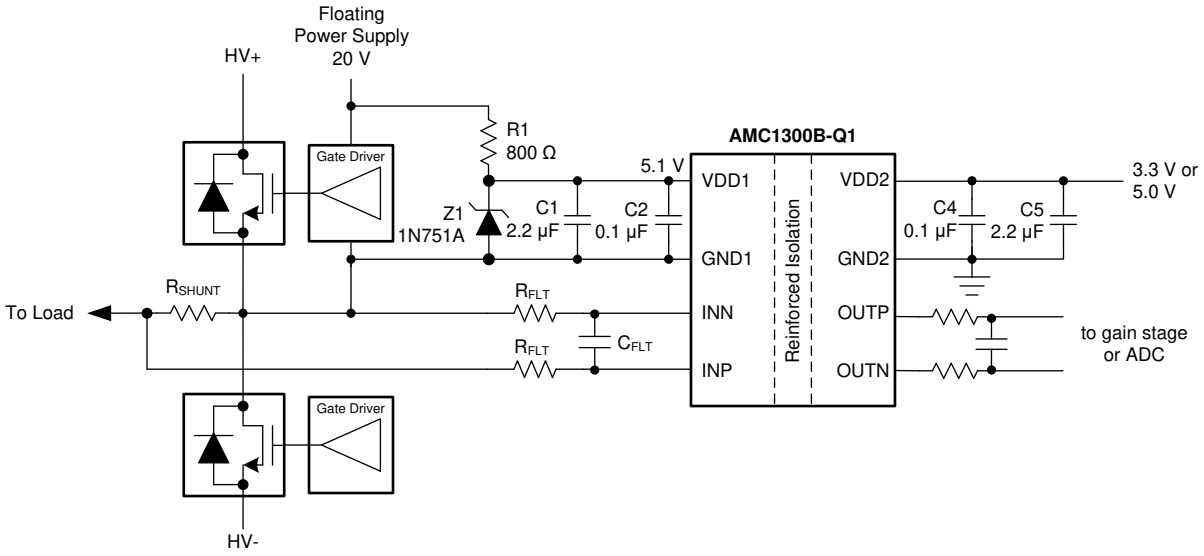


Figure 51. Zener-Diode-Based, High-Side Power Supply

10 Layout

10.1 Layout Guidelines

Figure 52 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300B-Q1 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300B-Q1 and keep the layout of both connections symmetrical.

10.2 Layout Example

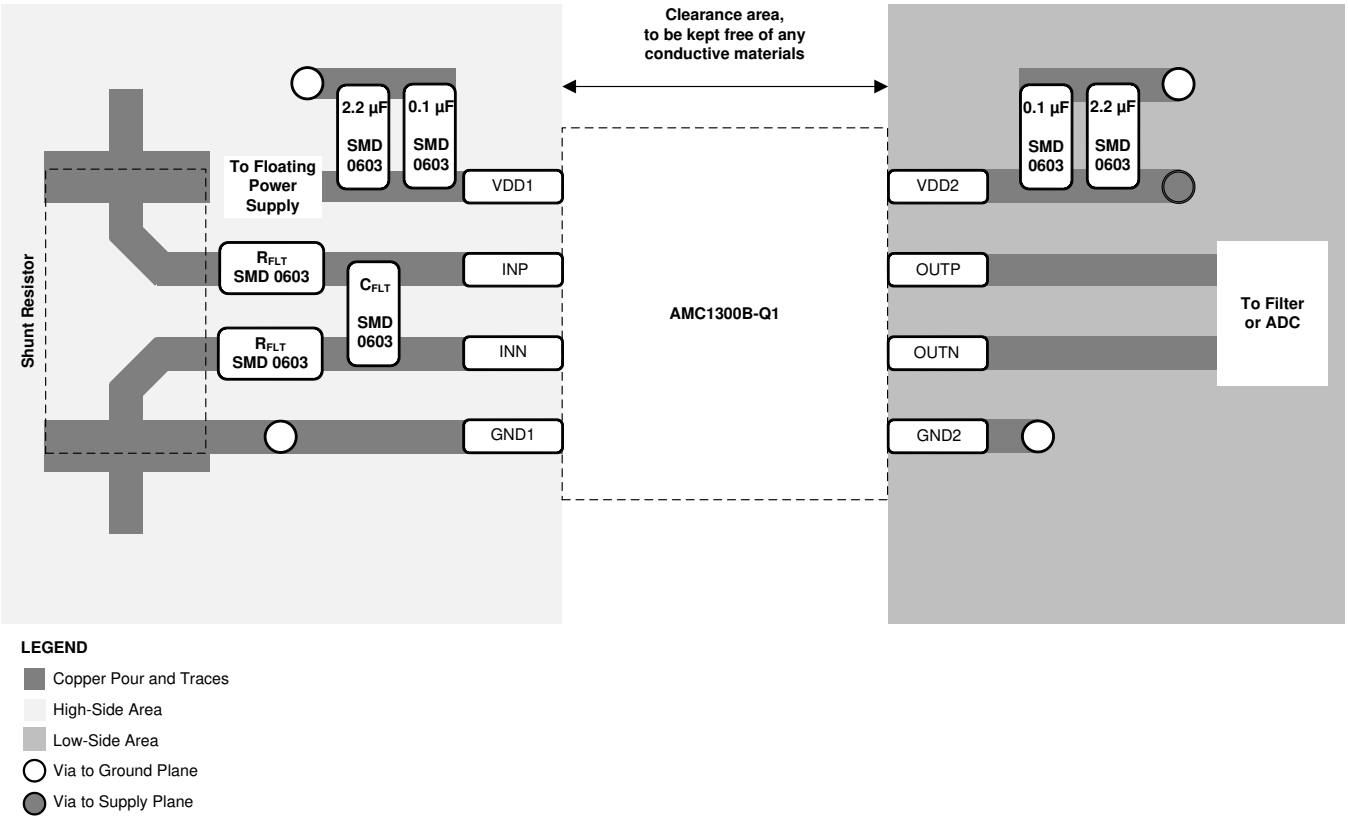


Figure 52. Recommended Layout of the AMC1300B-Q1

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *AMC1311x-Q1 High-Impedance, 2-V Input, Reinforced Isolated Amplifier* data sheet
- Texas Instruments, *TLV313-Q1 Low-Power, Rail-to-Rail In/Out, 750-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *AMC1311EVM* user guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *HEV/EV traction inverter power stage with 3 types of IGBT/SiC bias-supply solutions reference design*
- Texas Instruments, *Automotive High-Voltage and Isolation Leakage Measurements Reference Design*
- Texas Instruments, *Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1300BQDWVRQ1	PREVIEW	SOIC	DWV	8	1000	TBD	Call TI	Call TI	-40 to 125		
PAMC1300BQDWVRQ1	ACTIVE	SOIC	DWV	8	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

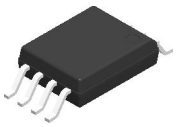
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

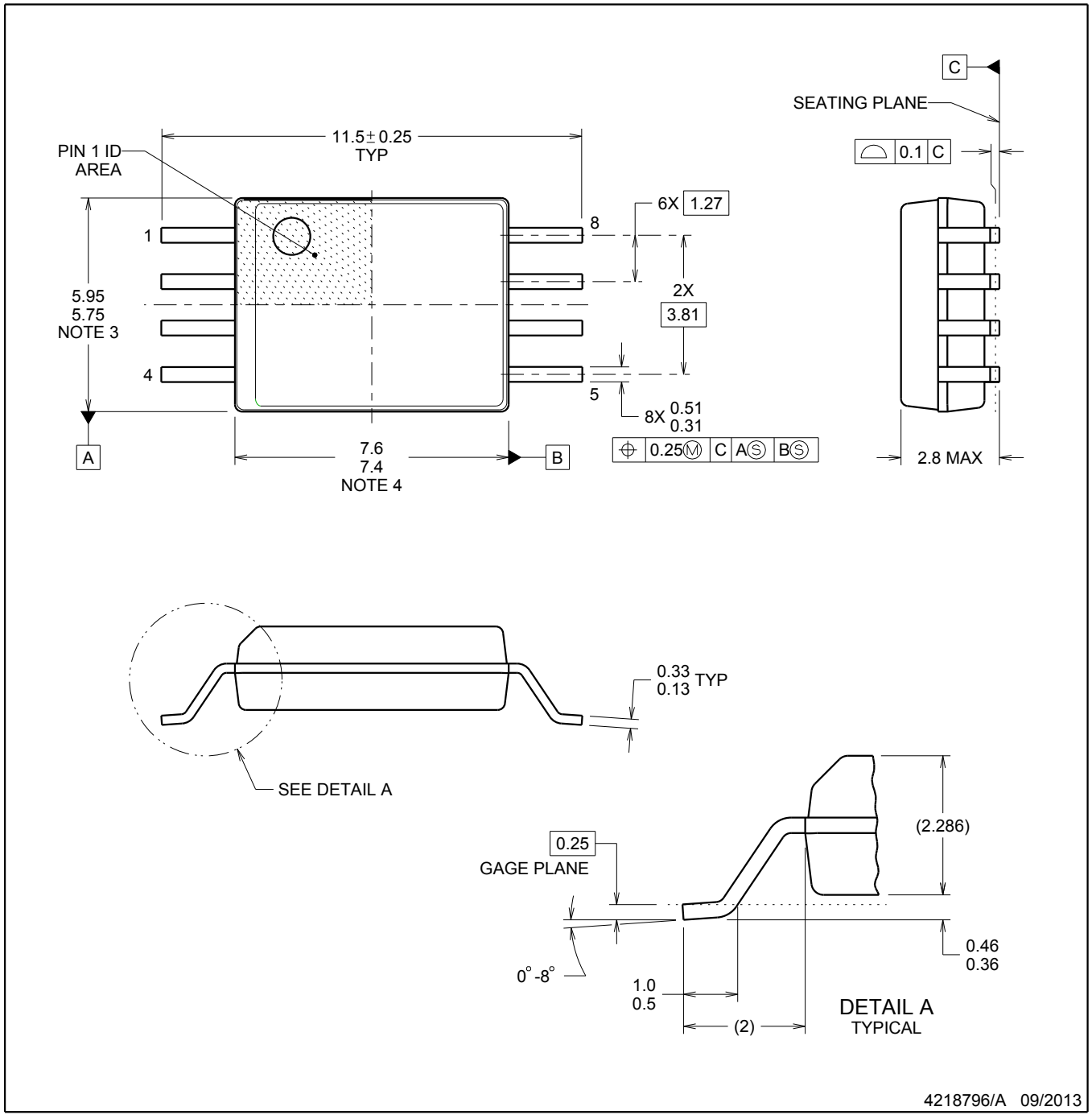
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



DWV0008A

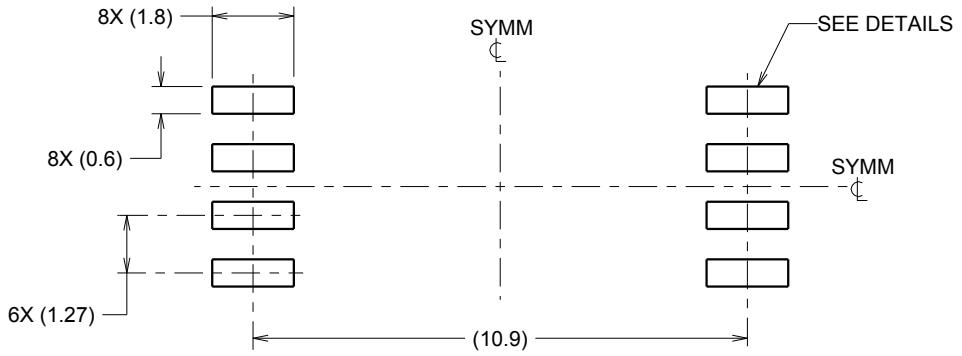
SOIC - 2.8 mm max height

SOIC

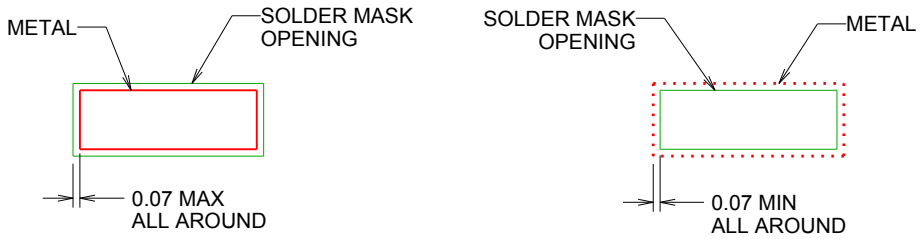


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

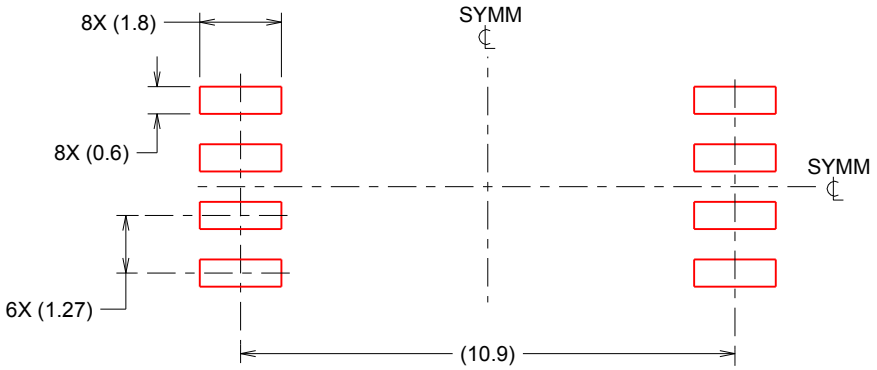
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265