Terminal Voltage ±5V, 100 Taps, Log Taper

Description

The Intersil X9C303 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a three-wire interface.

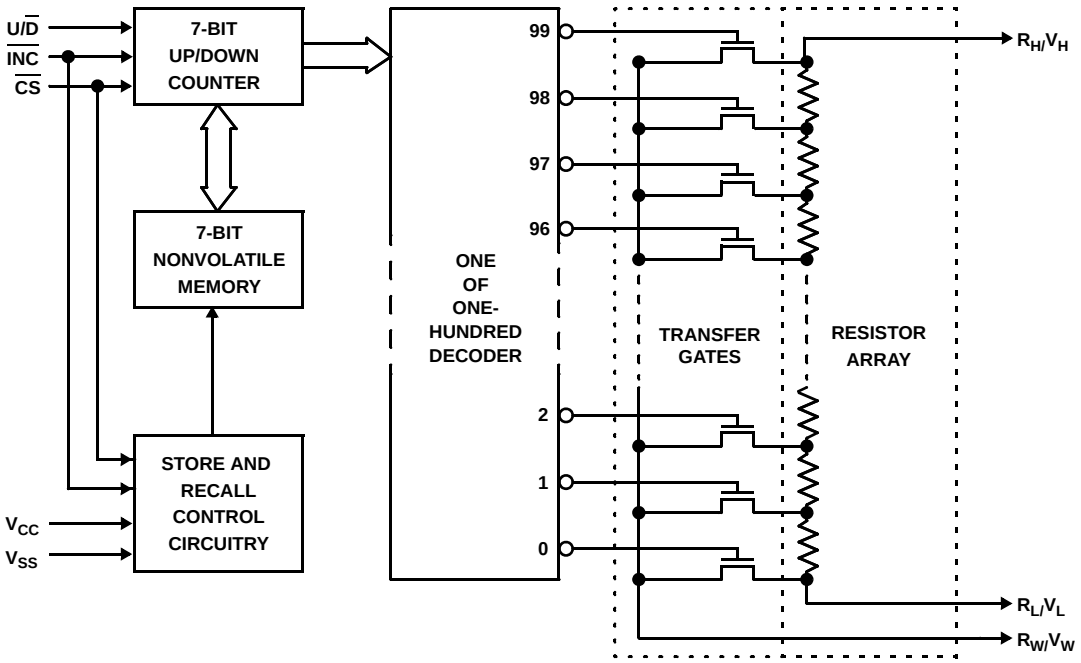
The resistor array is composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications ranging from control, to signal processing, to parameter adjustment. Digitally-controlled potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the use of nonvolatile memory for potentiometer settings retention.

Features

- Solid-state potentiometer
- Three-wire serial interface
- 100 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 99 resistive elements, log taper
  - Temperature compensated
  - End-to-end resistance, 32kΩ ±15%
  - Terminal voltages, ±5V
- Low power CMOS
  - V_{CC} = 5V
  - Active current, 3mA max.
  - Standby current, 750µA max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- Packages
  - 8 Ld TSSOP
  - 8 Ld SOIC
  - 8 Ld PDIP
- Pb-free available (RoHS compliant)

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
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Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X9C303P	X9C303P	0 to +70	8 Ld PDIP	MDP0031
X9C303PI	X9C303P I	-40 to +85	8 Ld PDIP	MDP0031
X9C303PIZ (Notes 1, 2)	X9C303P ZI	-40 to +85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X9C303PZ (Notes 1, 2)	X9C303P Z	0 to +70	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X9C303S8*, **	X9C303S	0 to +70	8 Ld SOIC (150 mil)	MDP0027
X9C303S8I*	X9C303S I	-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X9C303S8IZ* (Note 1)	X9C303S ZI	-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X9C303S8Z* (Note 1)	X9C303S Z	0 to +70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X9C303V8*, **	9C303	0 to +70	8 Ld TSSOP (4.4mm)	M8.173
X9C303V8I*	C303 I	-40 to +85	8 Ld TSSOP (4.4mm)	M8.173
X9C303V8IZ* (Note 1)	C303 IZ	-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X9C303V8Z* (Note 1)	9C303 Z	0 to +70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X9C303S8I-2.7	X9C303S G	-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X9C303S8IZ-2.7 (Note 1)	X9C303S ZG	-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027

*Add “T1” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

**Add “T2” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pin Descriptions

V_H and V_L

The high (V_H) and low (V_L) terminals of the device are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is –5V and the maximum is +5V. It should be noted that the terminology of V_L and V_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

V_W

V_W is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

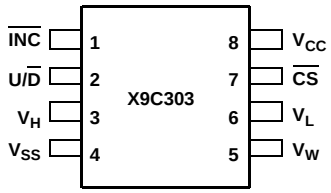
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

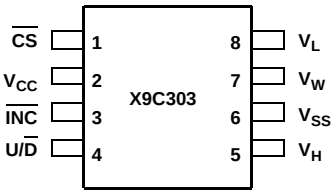
The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete, the device will be placed in the low power standby mode until the device is selected once again.

Pinouts

X9C303
(8 LD SOIC, 8 LD PDIP)
TOP VIEW



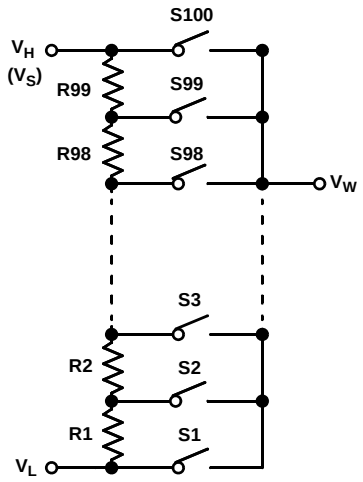
X9C303
(8 LD TSSOP)
TOP VIEW



Pin Names

SYMBOL	DESCRIPTION
V_H	High Terminal (Potentiometer)
V_W	Wiper Terminal (Potentiometer)
V_L	Low Terminal (Potentiometer)
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Control Input
$\overline{INC}$	Increment Control Input
$\overline{CS}$	Chip Select Control Input
NC	No Connection

Potentiometer Relationships



$$G_i = 20Log\frac{R_1 + R_2 + \ldots + R_i}{R_{TOTAL}} = \frac{V_W}{V_S}(V_L = 0V)$$

$$R_1 + R_2 + \ldots + R_{99} = R_{TOTAL}$$

(REFER TEST CIRCUIT 1)

Principles of Operation

There are three sections of the X9C303: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven-bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9C303, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as previously described ; once the new position is reached, the system would the keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position would be maintained until changed by the system or until a power-down/up cycle recalled the previously stored data.

This would allow the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference: system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

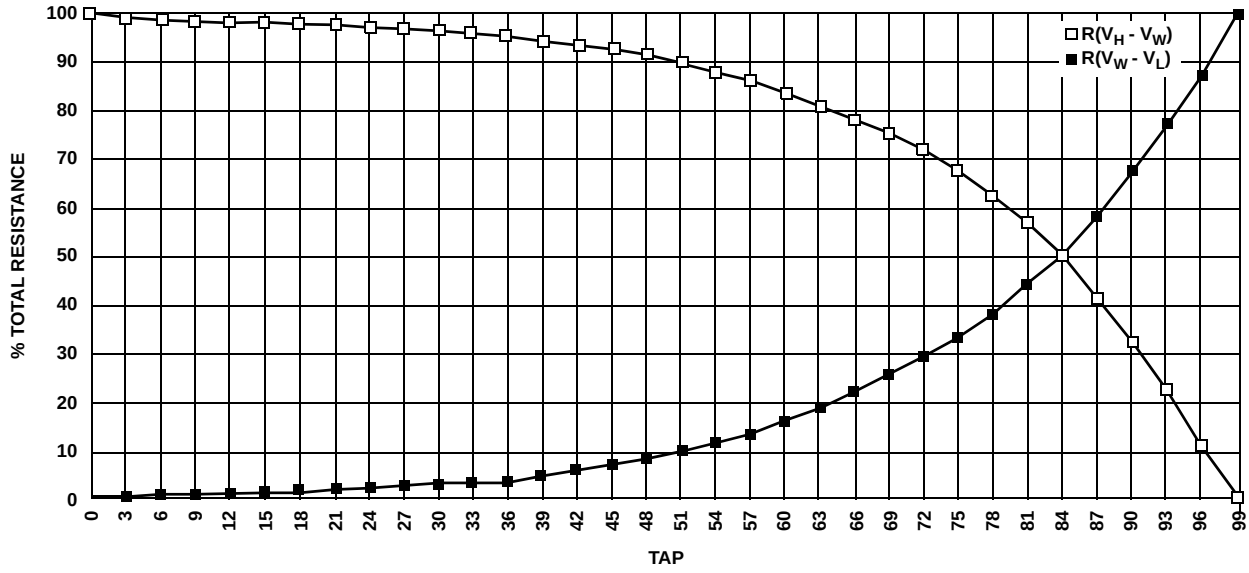
Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position
H	X	X	Standby Current
↗	L	X	No Store, Return to Standby
↘	L	H	Wiper Up (not recommended)
↘	L	L	Wiper Down (not recommended)

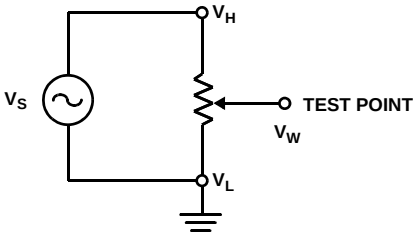
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

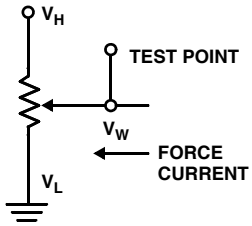
Typical Electrical Taper



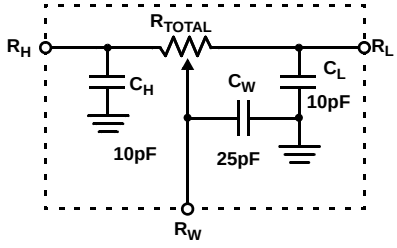
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



Absolute Maximum Ratings

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC} with Respect to V_{SS} . -1V to +7V
Voltage on V_H and V_L Referenced to V_{SS} . . . . . -8V to +8V
$\Delta V = |V_H - V_L|$ X9C303 . . . . . .10V
Wiper Current. . . . . ±1mA

Thermal Information

Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Recommended Operating Conditions

Commercial Temperature Range. . . . . 0°C to +70°C
Industrial Temperature Range . . . . . .-40°C to +85°C
Military Temperature Range. . . . . .-55°C to +125°C
Supply Voltage Range . . . . . 5V ±10%
Power Rating at +25°C X9C303 . . . . . .10mW
Physical Characteristics
Marking Includes
Manufacturer's Trademark
Resistance Value or Code
Date Code

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Analog Specifications

Over recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (Note 3)	MAX	
R_{TOTAL}	End-to-End Resistance			32		kΩ
	End-to-End Resistance Tolerance		-15		+15	%
V_H	V_H Terminal Voltage		-5		+5	V
V_L	V_L Terminal Voltage		-5		+5	V
R_W	Wiper Resistance	Max Wiper Current ±1mA		40	100	Ω
	Tap Position Relative Step Size Error	Error = log (Vw(n)) - log (Vw(n - 1)) for tap n = 2 - 99, V_H-V_L = 10V	0.005		0.115	dB
	Resistor Noise	At 1kHz		23		nV(RMS)/$\sqrt{Hz}$
	Charge Pump Noise	At 850kHz		20		mV(RMS)
	End-to-End Resistance Temperature Coefficient	T = -40°C to +85°C		±400		ppm/°C
	Ratiometric Temperature Coefficient	Tap position 84		±20		ppm/°C
$C_H/C_L/C_W$ (Note 5)	Potentiometer Capacitance	See "Circuit #3 SPICE Macro Model" on page 4		10/10/25		pF

DC Electrical Specifications

Over recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (Note 3)	MAX	
I_{CC}	V_{CC} Active Current	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V to 2.4V @ Max t_{CYC}		1	3	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V		200	750	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}	-10		+10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Voltage		2			V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW voltage				0.8	V
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz		10		pF
EEPROM SPECS						
	EEPROM Endurance	Wiper storage operations over recommended operation conditions	100,000			Cycles
	EEPROM Retention	At +55°C		100		Years

NOTES:

3. Typical values are for T_A = +25°C and nominal supply voltage.

Standard Parts

PART NUMBER	MAXIMUM RESISTANCE	WIPER INCREMENTS	MINIMUM RESISTANCE
X9C303	32kΩ	Log Taper	40Ω Typical

AC Conditions of Test

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

AC Electrical Specifications

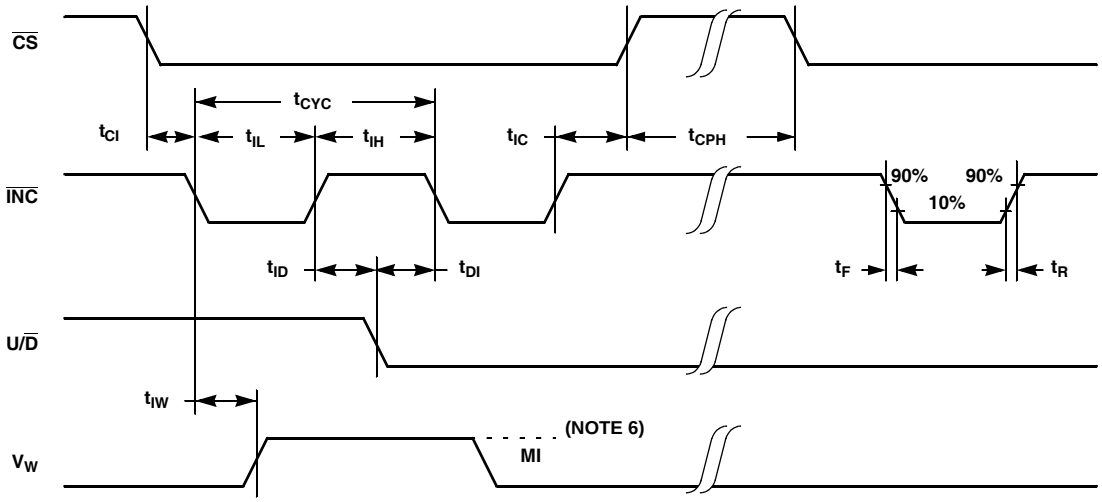
Over recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP (Note 4)	MAX	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Set-up	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Set-up	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW} (Note 5)	$\overline{INC}$ to V_W Change		100		µs
t_{CYC}	$\overline{INC}$ Cycle Time	2			µs

AC Electrical Specifications Over recommended operating conditions, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP (Note 4)	MAX	
t_R, t_F (Note 5)	$\overline{INC}$ Input Rise and Fall Time			500	ns
t_{PU} (Note 5)	Power-up to Wiper Stable		500		µs
t_R V_{CC} (Note 5)	V_{CC} Power-up Rate	0.2		50	mV/µs

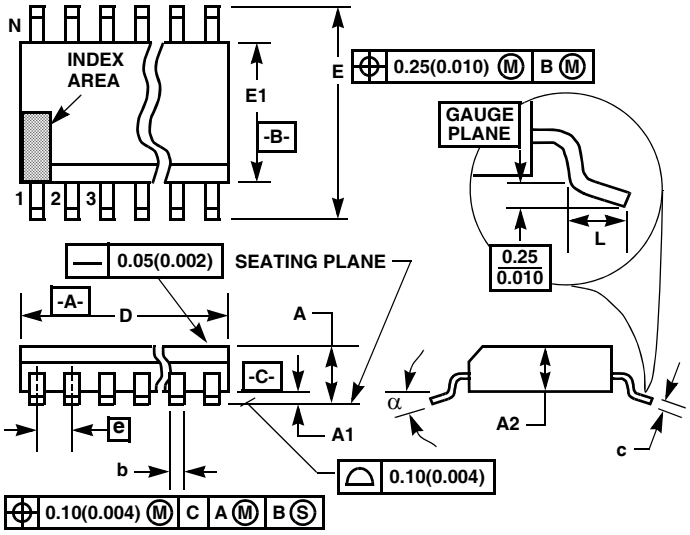
AC Timing Diagram



NOTES:

4. Typical values are for T_A = +25°C and nominal supply voltage.
5. This parameter is not 100% tested.
6. MI in the “AC Timing Diagram” refers to the minimum incremental change in the V_W output due to a change in the wiper position.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

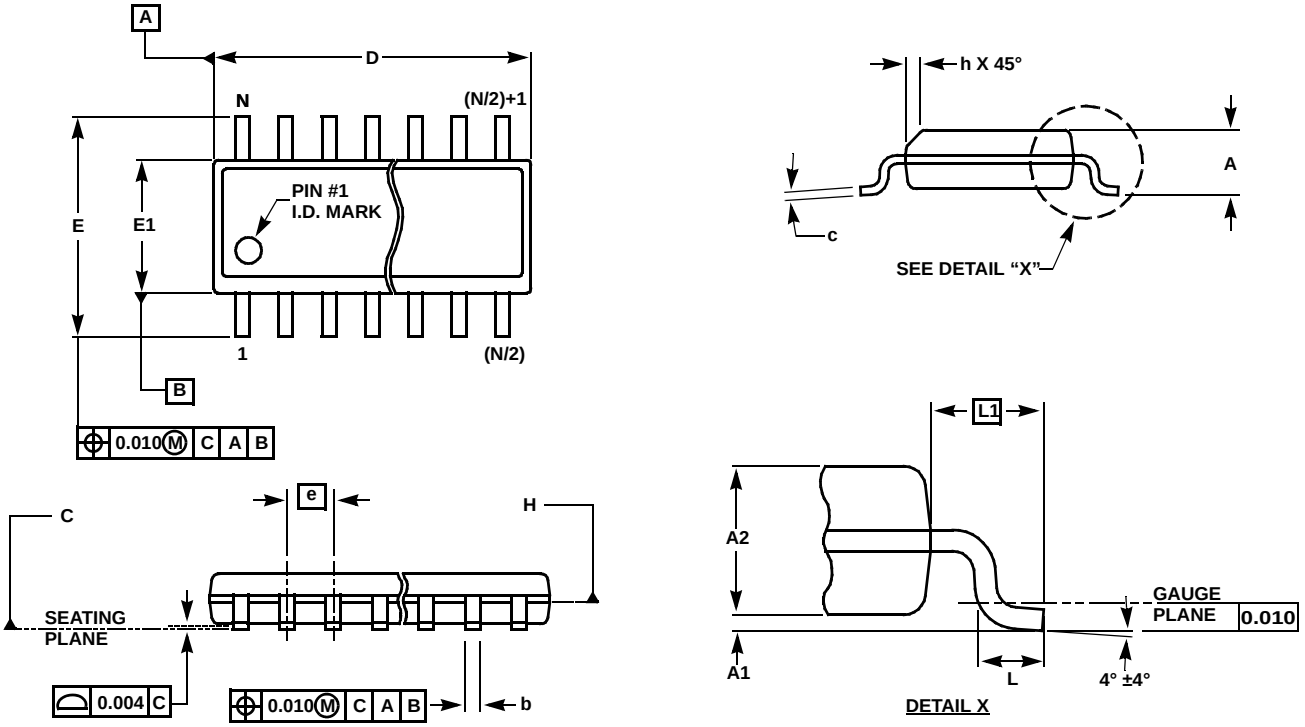
M8.173

8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0º	8º	0º	8º	-

Rev. 1 12/00

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

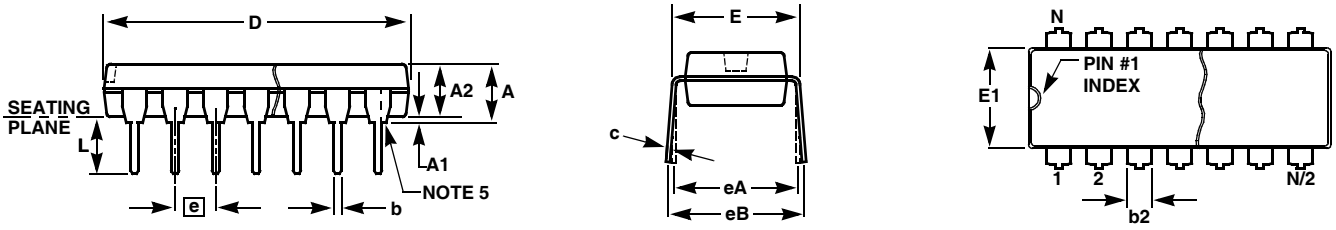
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

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NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
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