SPICE Device Model Si9407BDY

Vishay Siliconix

P-Channel 60-V (D-S) MOSFET

CHARACTERISTICS

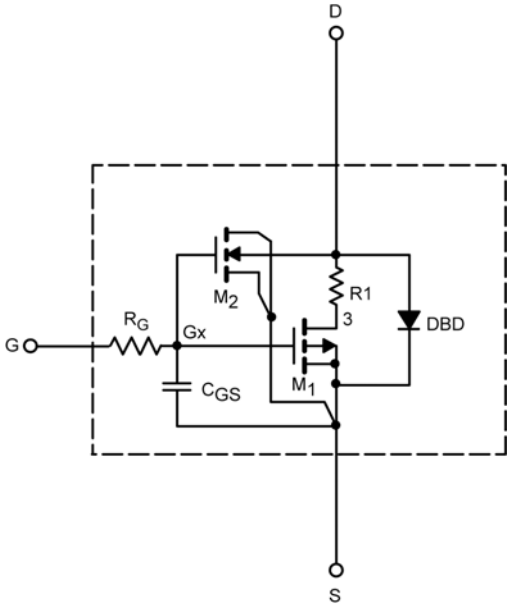
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the P-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

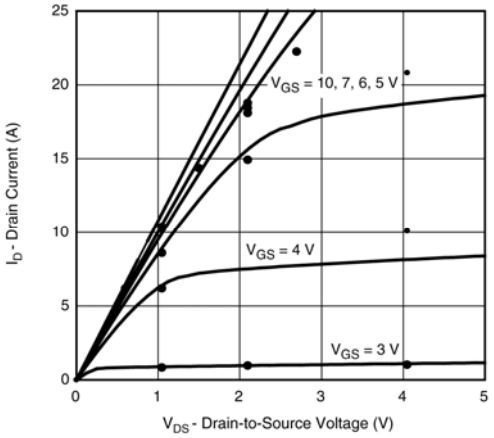


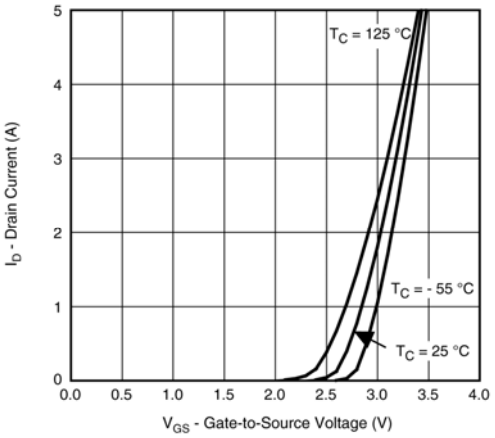
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

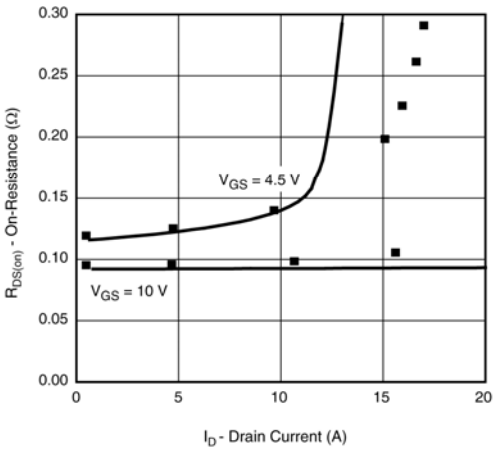
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	2.1		V
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -3.2$ A	0.092	0.100	Ω
		$V_{GS} = -4.5$ V, $I_D = -2.9$ A	0.119	0.126	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -10$ V, $I_D = -3.2$ A	7.1	8.5	S
Diode Forward Voltage	V_{SD}	$I_F = -2$ A	- 0.76	- 0.80	V
Dynamic[b]					
Input Capacitance	C_{iss}	$V_{DS} = -30$ V, $V_{GS} = 0$ V, f = 1 MHz	608	600	pF
Output Capacitance	C_{oss}		71	70	
Reverse Transfer Capacitance	C_{rss}		39	50	
Total Gate Charge	Q_g	$V_{DS} = -30$ V, $V_{GS} = -10$ V, $I_D = -3.2$ A	12	14.5	nC
		$V_{DS} = -30$ V, $V_{GS} = -4.5$ V, $I_D = -3.2$ A	6.4	8	
Gate-Source Charge	Q_{gs}		2.2	2.2	
Gate-Drain Charge	Q_{gd}		3.7	3.7	

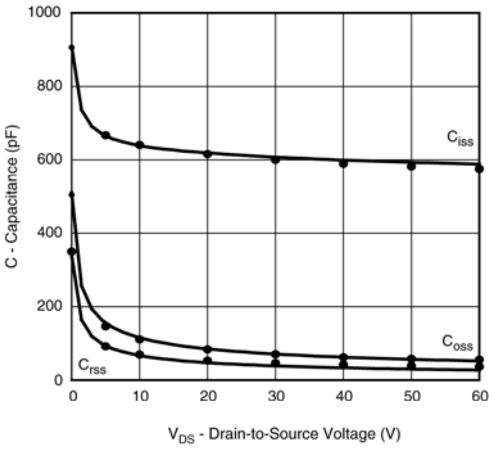
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

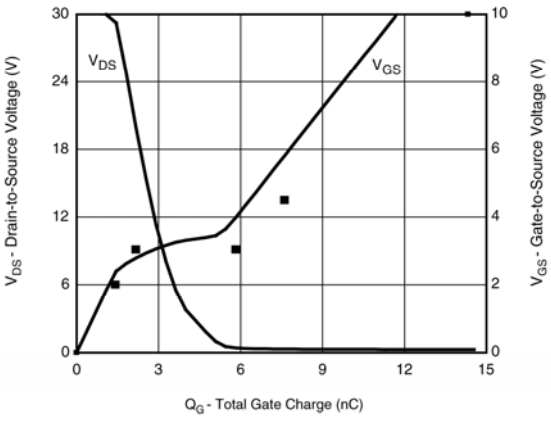
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C UNLESS OTHERWISE NOTED)

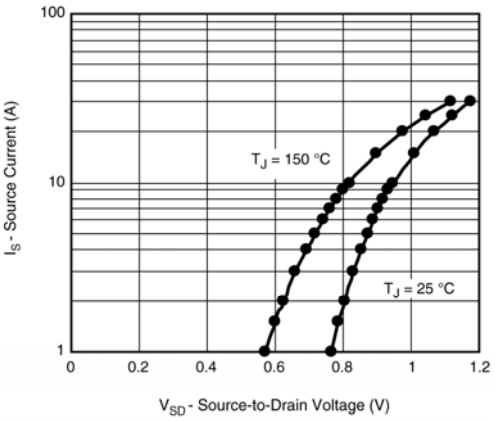












Note: Dots and squares represent measured data.

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