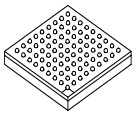
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Data Sheet: Technical Data

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MCF5251



Package Information
MAPBGA–225

MCF5251 ColdFire® Microprocessor Data Sheet

Ordering Information: See Table 1 on page 2

1 Introduction

This document provides an overview of the MCF5251 ColdFire processor and general descriptions of the MCF5251 features and modules. Also provided are electrical specifications, pin assignments, and package diagrams for MCF5251 ColdFire® processor. For functional characteristics, refer to the *MCF5251 Reference Manual* (MCF5251RM).

The MCF5251 is a system controller/decoder for compressed audio music players addressing both portable and automotive solutions supporting CD, HDD and USB based systems. The 32-bit ColdFire core with enhanced multiply and accumulate (eMAC) unit provides optimum performance and code density for the combination of control code and signal processing required for compressed audio decode, file management, and system control.

The MCF5251 is a general purpose system controller with over 125 Dhrystone 2.1 MIPS @ 140 MHz performance. The integrated peripherals and EMAC allow the MCF5251 to replace both the microcontroller

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and the DSP in certain applications. Most peripheral pins can also be remapped as general purpose I/O pins.

Low power features include flexible PLL (with power-down mode) with dynamic clock switching, a hardwired CD ROM decoder, advanced 0.13 µm CMOS process technology, 1.2 V core power supply, and on-chip 128K-byte SRAM.

MP3 decode requires less than 20 MHz CPU bandwidth and runs from on-chip SRAM.

For additional information regarding software drivers and applications, refer to http://www.freescale.com/coldfire.

1.1 Orderable Part Numbers

Table 1 lists the orderable part numbers for the MCF5251 processor.

Table 1. Orderable Part Numbers

Orderable Part Number	Maximum Clock Frequency	Package Type	Operating Temperature Range	MP3 Royalty	Part Status
MCF5251VM140	140 MHz	225 MAPBGA	-20 to +70°C	N/A	Lead free
MCF5251CVM140			-40 to +85°C	N/A	

1.2 Block Diagram

Figure 1 illustrates the functional block diagram of the MCF5251 processor.

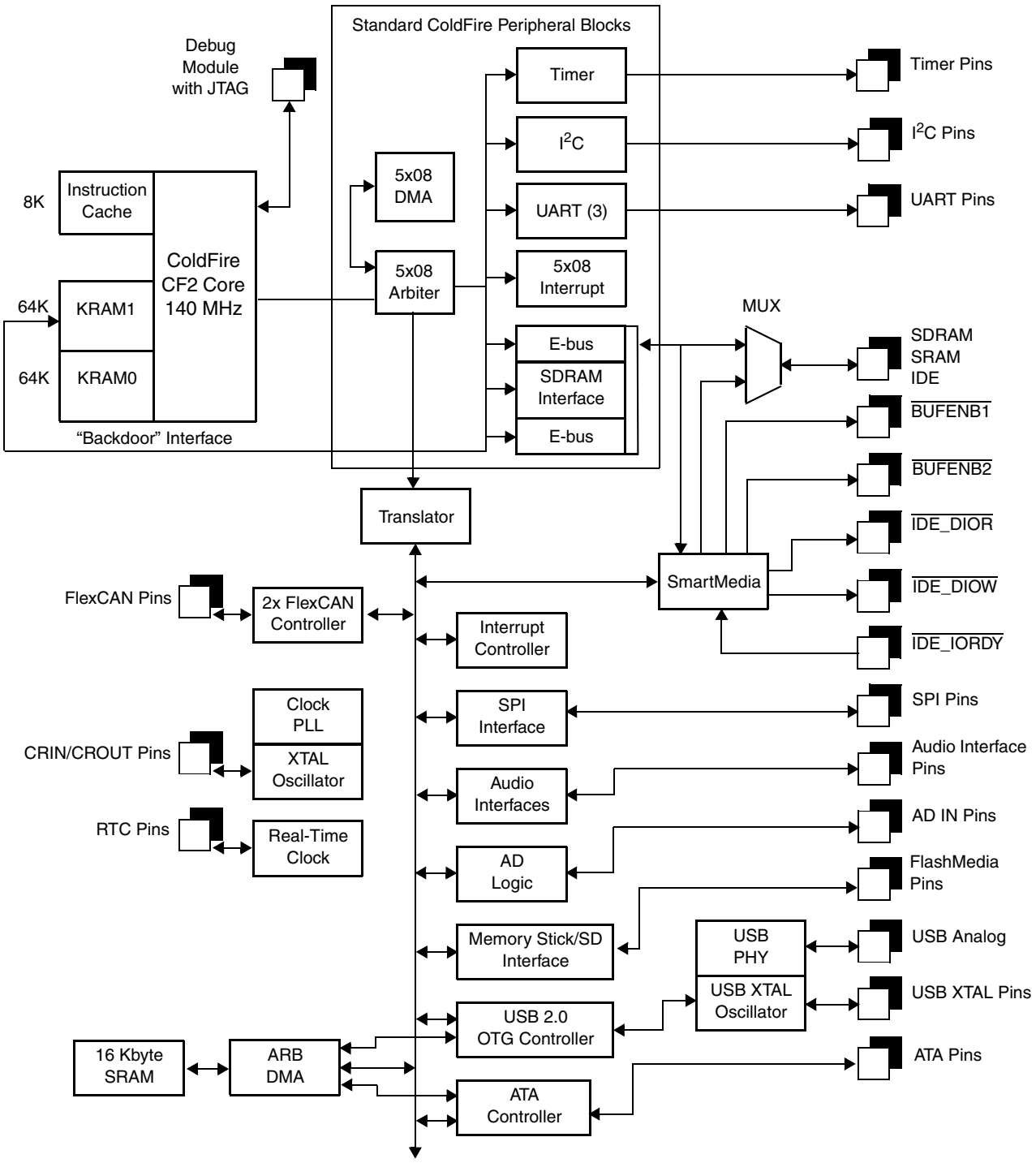


Figure 1. MCF5251 Block Diagram

2 Functional Description

2.1 Version 2 ColdFire Core

The Version 2 ColdFire (CF2) core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size. The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function.

2.2 Module Inventory

Table 2 shows an alphabetical listing of the modules in the processor.

Table 2. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description
ATA	Advanced Technology Attachment Controller	Connectivity Peripheral	The ATA block is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives.
ADC	Battery Level/Keypad Analog/Digital Converter	Analog Input	The six-channel ADC is based on the Sigma-Delta concept with 12-bit resolution. Both the analog comparator and digital sections are integrated in the MCF5251.
AB	Audio Bus	Audio Interface	The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission.
AIM	Audio Interface	Audio Interface	The audio interface module provides the necessary input and output features to receive and transmit digital audio signals over serial audio interfaces (IIS/EIAJ) and over digital audio interfaces (IEC958).
BROM	Bootloader	Boot ROM	The MCF5251 incorporates a ROM Bootloader, which enables booting from UART, I2C, SPI, or IDE devices.
FlexCAN	Twin Controller Area Network 2.0B Communication Unit	Connectivity Peripheral	The FlexCan module is a full implementation of the Bosch CAN protocol specification 2.0B, which supports both standard and extended message frames.
CSM	Chip Select Module	Connectivity Peripheral	Three programmable chip-select outputs ($\overline{CS0}$/$\overline{CS4}$, $\overline{CS1}$, and $\overline{CS2}$) provide signals that enable glueless connection to external memory and peripheral circuits.
DMAC	Direct Memory Access Controller Module	Connectivity Peripheral	There are four fully programmable DMA channels for quick data transfer.
eMAC	enhanced Multiply Accumulate Module	Core	The integrated eMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture.
MBUS	Memory Bus Interface	Bus Operation	The bus interface controller transfers data between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus.
MMC/SD	Multimedia Card/Secure Digital Interface	Flash Memory Card Interface	The interface is Sony® Memory Stick®, SecureDigital, and Multi-Media card compatible. **Note:** The Sony Memory Interface does not support Sony MagicGate™.

Table 2. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
GPIO	General Purpose I/O Interface	System integration	GPIO signals are multiplexed with various other signals.
GPT	General Timer Module	Timer peripheral	The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer.
IDE	Integrated Drive Electronics	Connectivity peripheral	The IDE hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses from propagating to the IDE bus.
INC	Instruction Cache	Core	The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock cycle.
I^2C	Inter IC Communication Module	Connectivity peripheral	The two-wire I^2C bus interfaces, compliant with the Philips I^2C bus standard, are bidirectional serial buses that exchange data between devices.
SRAM	Internal 128-KB SRAM	Internal memory	The 128-Kbyte on-chip SRAM is split over two banks, SRAM0 (64K) and SRAM1 (64K). It provides single clock-cycle access for the ColdFire core.
LIN	Internal Voltage Regulator	Linear regulator	An internal 1.2 V regulator is used to supply the CPU and PLL sections of the MCF5251, reducing the number of external components required and allowing operation from a single supply rail, typically 3.3 volts.
JTAG	Joint Test Action Group	Test and debug	To help with system diagnostics and manufacturing testing, the MCF5251 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG.
QSPI	Queued Serial Peripheral Interface	Connectivity Interface	The QSPI module provides a serial peripheral interface with queued transfer capability.
RTC	Real-Time Clock	Timer Peripheral	The RTC is a clock that keeps track of the current time even if the clock is turned off.
BDM	Background Debug Interface	Test and debug	A background-debug mode (BDM) interface provides system debug.
SDRAMC	Synchronous DRAM Memory Controller	Peripheral Interface	The SDRAM controller provides a glueless interface for one bank of SDRAM, and can address up to 32MB. The controller supports a 16-bit data bus. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMs.
SIM	System Integration Module	System Integration	The SIM provides overall control of the internal and external buses and serves as the interface between the ColdFire core and the internal peripherals or external devices. The SIM is responsible for the two interrupt controllers (setting priorities and levels). And it also configures the GPIO ports.
PLL	System Oscillator and Phase Lock Loop	System Clocking	The oscillator operates from an external crystal connected across CRIN and CROUT. The circuit can also operate from an external clock connected to CRIN. The on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5–35 MHz).

Table 2. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description
UART	Universal Asynchronous Receiver /Transmitter Module	Connectivity Peripheral	Three UARTs handle asynchronous serial communication.
USBOTG	USB 2.0 High-Speed On-The-Go	Connectivity Peripheral	The USB module is used for communication to a PC or communication to slave devices; for example, to download data from a hard disc player to a flash player, and to other devices.

3 Signal Description

This chapter describes the MCF5251 input and output signals. The signal descriptions as shown in Table 3 are grouped according to relevant functionality. For additional signal information, see "Chapter 2, Signal Description" in the MCF5251 reference manual.

Table 3. MCF5251 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[24:1] A[23]/GPO54	24 address lines—address 23 is multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only).	Out	X
Read-write control	RW	Bus write enable—indicates if read or write cycle in progress.	Out	H
Output enable	$\overline{OE}$	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	$\overline{SDRAS}$/GPIO59	Row address strobe for external SDRAM	Out	negated
Synchronous column address strobe	$\overline{SDCAS}$/GPIO39	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	$\overline{SDWE}$/GPIO38	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	$\overline{SDUDQM}$/GPO53	Upper byte enable—indicates during write cycle if high byte is written.	Out	–
SDRAM lower byte enable	$\overline{SDLDQM}$/GPO52	Lower byte enable—indicates during write cycle if low byte is written.	Out	–
SDRAM chip selects	$\overline{SD_CS0}$/GPIO60	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE/GPIO63	SDRAM clock enable	Out	–
System clock	BCLK/GPIO40	SDRAM clock output	In/Out	–

Table 3. MCF5251 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
ISA bus read strobe	IDE_DIOR/GPIO31 (CS2)	1 ISA bus read strobe and 1 ISA bus write strobe—allow connection of an independent ISA bus peripheral, such as an IDE slave device.	In/Out	–
ISA bus write strobe	IDE_DIOW/GPIO32 (CS2)		In/Out	–
ISA bus wait signal	IDE_IORDY/GPIO33	ISA bus wait line available for both busses	In/Out	–
Chip Selects[2:0]	CS0/CS4 CS1/QSPICS3/GPIO28	Chip selects bits 2 through 0—enable peripherals at programmed addresses. CS0 provides boot ROM selection.	Out In/Out	negated
Buffer enable 1	BUFENB1/GPIO29	Two programmable buffer enables—allow seamless steering of external buffers to split data and address bus in sections.	In/Out	–
Buffer enable 2	BUFENB2/GPIO30		In/Out	–
Transfer acknowledge	TA/GPIO12	Transfer Acknowledge signal.	In/Out	–
Wake Up	WAKEUP/GPIO21	Wake-up signal input	In	–
Serial Clock Line	SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10	Clock signal for Dual I^2C module operation	In/Out	–
Serial Data Line	SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44	Serial data port for second I^2C module operation	In/Out	–
Receive Data	SDA1/RXD1/GPIO44 RXD0/GPIO46 EF/RXD2/GPIO6	Receive serial data input for UART	In	–
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45 XTRIM/TXD2/GPIO0	Transmit serial data output for UART	Out	–
Request-To-Send	DDATA3/RTS0/GPIO4 DDATA1/RTS1/SDATA2_BS2/GPIO2	Signals sent from UART0/1 that it is ready to receive data	Out	–
Clear-To-Send	DDATA2/CTS0/GPIO3 DDATA0/CTS1/SDATA0_SDIO1/GPIO1	Signals sent to UART0/1 that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capability of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLKOUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPICS0/EBUIN4/GPIO15	Audio interfaces to IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPICS1/EBUOUT2/GPIO16	Audio interfaces to IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	Audio interfaces to serial data inputs	In	–

Table 3. MCF5251 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	Audio interfaces to serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/AUDIOCLOCK/GPIO43	Audio interfaces to serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	Audio interfaces to serial bit clocks	In/Out	–
Serial input	EF/RXD2/GPIO6	Error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPIDIN/QSPIDOUT/ GPIO26	Audio interfaces to subcode clock	In/Out	–
Subcode sync	QSPIDOUT/SFSY/GPIO27	Audio interfaces to subcode sync	In/Out	–
Subcode data	QSPICLK/SUBR/GPIO25	Audio interfaces to subcode data	In/Out	–
Clock frequency trim	XTRIM/TXD2/GPIO0	Clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPICS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/AUDIOCLOCK/GPIO43	Optional audio clock input		–
MemoryStick/ SecureDigital interface	EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command lane—MemoryStick interface 2 data I/O	In/Out	–
	EBUIN2/SCLKOUT/GPIO13	Clock out for both MemoryStick interfaces and for Secure Digital	In/Out	–
	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	SecureDigital serial data bit 0—MemoryStick interface 1 data I/O	In/Out	–
	SCL0/SDATA1_BS1/GPIO41	SecureDigital serial data bit 1—MemoryStick interface 1 strobe	In/Out	–
	DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	SecureDigital serial data bit 2—MemoryStick interface 2 strobe Reset output signal	In/Out	–
	SDA0/SDATA3/GPIO42	SecureDigital serial data bit 3	In/Out	–

Table 3. MCF5251 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
AT attachment interface (IDE interface)	ATA_DIOW	ATA write strobe signal	Out	–
	ATA_DIOR	ATA read strobe signal	Out	–
	ATA_IORDY	ATA I/O ready input	In	–
	ATA_DMARQ	ATA DMA request	In	–
	ATA_DMACK	ATA DMA acknowledge	Out	–
	ATA_INTRQ	ATA interrupt request	In	–
	ATA_CS0	ATA chip select 0	Out	–
	ATA_CS1	ATA chip select 1	Out	–
	ATA_A[2:0]	3-bit ATA address bus	Out	–
	ATA_D[15:0]	16-bit ATA data bus	In/Out	–
CAN interface	CAN0_TX	CAN 0 transmit	Out	–
	CAN0_RX	CAN 0 receive	In	–
	CAN1_TX	CAN 1 transmit	Out	–
	CAN1_RX	CAN 1 receive	In	–
USB PHY interface	USBVBUS	USB Vbus input	In	–
	USBID	USB ID input	In	–
	USBRES	USB current programming resistor pin	Analog	–
	USBDN	USB DM signalling line	In/Out	–
	USBDP	USB DP signalling line	In/Out	–
USB oscillator	USB_CRIN USB_CROUT	Connections for USB oscillator crystal (24 MHz)	In Out	–
RTC oscillator	RTC_CRIN RTCCROUT	Connections for real-time clock crystal (32.768 kHz)	In Out	–
AD IN	ADIN0/GPI52 ADIN1/GPI53 ADIN2/GPI54 ADIN3/GPI55 ADIN4/GPI56 ADIN5/GPI57	Analog-to-Digital Converter input signals	In	–
AD OUT	ADREF ADOUT/SCLK4/GPIO58	Analog-to-Digital Converter output signal—connects to ADREF via integrator network.	In/Out	–
QSPI clock	QSPICLK/SUBR/GPIO25	QSPI clock signal	In/Out	–
QSPI data in	RCK/QSPIDIN/QSPIDOUT/GPIO26	QSPI data input	In/Out	–

Table 3. MCF5251 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
QSPI data out	RCK/QSPIDIN/QSPIDOUT/GPIO26 QSPIDOUT/SFSY/GPIO27	QSPI data out	In/Out	–
QSPI chip selects	QSPICS0/EBUIN4/GPIO15 QSPICS1/EBUOUT2/GPIO16 QSPICS2/MCLK2/GPIO24 $\overline{CS1}$/QSPICS3/GPIO28	QSPI chip selects	In/Out	–
System oscillator in	CRIN	System input	In	–
System oscillator out	CROUT	System output	Out	–
Reset In	$\overline{RSTI}$	Processor reset input	In	–
Freescale Test Mode	TEST[2:0]	TEST pins.	In	–
Linear regulator output	LINOUT	Output of 1.2 V to supply core	Out	–
Linear regulator input	LININ	Input, typically I/O supply (3.3V)	In	–
Linear regulator ground	LINGND			–
High Impedance	$\overline{HI_Z}$	Assertion tri-states output signal pins	In	
Debug Data	DDATA0/$\overline{CTS1}$/SDATA0_SDIO1/GPIO1 DDATA1/$\overline{RTS1}$/SDATA2_BS2/GPIO2 DDATA2/$\overline{CTS0}$/GPIO3 DDATA3/$\overline{RTS0}$/GPIO4	Display of captured processor data and break-point statuses	In/Out	Hi-Z
Processor Status	PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47	Indication of internal processor status.	In/Out	Hi-Z
Processor clock	PSTCLK/GPIO51	Processor clock output	Out	–
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG	In	–
Test Reset/ Development Serial Clock	DSCLK/$\overline{TRST}$	Multiplexed signal that is asynchronous reset for JTAG controller. Also, clock input for debug module.	In	–
Test Mode Select/Break Point	TMS/$\overline{BKPT}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode	In	–
Test Data Input/ Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	–
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module	Out	–

4 Electrical Specifications

Table 4 through Table 9 provide the electrical characteristics for the MCF5251 processor. The remaining figures and tables in this section provide the timing diagrams and the timing parameters for the MCF5251 processor.

Table 4 provides the maximum rating parameters for the MCF5251 processor.

Table 4. Maximum Ratings

Rating	Symbol	Value	Units
Supply Core Voltage	V_{cc}	-0.5 to +2.5	V
Maximum Core Operating Voltage	V_{cc}	+1.32	V
Minimum Core Operating Voltage	V_{cc}	+1.08	V
Supply I/O Voltage	V_{cc}	-0.5 to +4.6	V
Maximum I/O Operating Voltage	V_{cc}	+3.6	V
Minimum I/O Operating Voltage	V_{cc}	+3.0	V
Input Voltage	V_{in}	–0.5 to +6.0	V
Storage Temperature Range	T_{stg}	–65 to +150	°C

Table 5 provides the recommended operating temperatures for the MCF5251 processor.

Table 5. Operating Temperature

Characteristic	Symbol	Value	Units
Maximum Operating Ambient Temperature	T_{Amax}	+85[1]	°C
Minimum Operating Ambient Temperature	T_{Amin}	-40	°C

[1] This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature does not exceed 125° C.

Table 6 provides the recommended operating supply voltages for the MCF5251 processor.

Table 6. Recommended Operating Supply Voltages

Pin Name	Min	Typ	Max	Unit
COREVDD	1.08	1.2	1.32	V
PADVDD	3.0	3.3	3.6	V
ADVDD	3.0	3.3	3.6	V
ADGND	–	GND	–	V
OSCPADVDD	3.0	3.3	3.6	V
OSCPADGND	–	GND	–	V
USBVDD	–	3.3	–	V
USBVDDP	–	1.2	–	V

Table 6. Recommended Operating Supply Voltages (continued)

Pin Name	Min	Typ	Max	Unit
USBGND	–	GND	–	V
RTCVDDA	3.0	–	4.2	V
RTCVSSA	–	GND	–	V
PLLCOREVDD	1.08	1.2	1.32	V
PLLCOREGND	–	GND	–	V
LININ	3.0	3.3	3.6	V
GND	–	GND	–	V

Table 7 provides the operating parameters for the linear regulator.

Table 7. Linear Regulator Operating Parameters

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage (LININ)	Vin	3.0	3.3	3.6	V
Output Voltage (LINOUT)	Vout	1.08	1.2	1.32	V
Output Current	Iout	–	100	–	mA
Power Dissipation	Pd	–	–	500	mW
Load Regulation 10% Iout ≥ 90% Iout	–	–	50	60	mV
Power Supply Rejection	PSRR	–	40	–	dB

NOTE

A pmos regulator is used as a current source in this linear regulator, so a 10 µF capacitor (ESR 0... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically, this requires the use of a tantalum type capacitor.

Table 8 provides the operating parameters for the ADC DC electrical characteristics.

Table 8. Operating Parameters for ADC DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Operation Voltage Range for ADC	ADVDD	3	–	3.6	V
Common Mode Rejection	CMR	0	–	ADVDD–1.1	v
Reference Voltage (external)	ADREF	0	–	ADVDD–1.1	v
Input offset voltage	V_{offset}	–	10	–	mV
Input Hysteresis (ADINx = ADVDD/2)	V_{hyst}	0.73	0.78	0.85	mV
ADC Input Linear Operating Range	ADINx	0	–	ADVDD–1.1	V

Table 9 provides the DC electrical specifications for the digital pins.

Table 9. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{in}	–	±1	μA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	μA
Output High Voltage I_{OH} = 11.9 mA[1], 6.3 mA[2],3.1 mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 7.1m A[1], 3.5 mA[2], 1.8 mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[4]	V_{T+}	1.67	1.79	V
Schmitt Trigger High to Low Threshold Point[4]	V_{T-}	1.01	1.15	V
Load Capacitance: D[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, IDE_DIOR, IDE_DIOW, IDE_IORDY, MCLK1, MCLK2	C_L	–	50	pF
Load Capacitance: A[24:9], ATA_CS0, ATA_CS1, ATA_A[2:0], ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_D[15:0], SDATAI[3,1]	C_L	15	40	pF
Load Capacitance: A[8:1], ADOUT, ATA_RST BCLK, BCLKE, SDCAS, SDRAS, SDLDQM, SDCS0, SDUDQM, SDWE, BUFENB[2:1], CAN0_TX, CAN1_TX, EBUIN1, RXD[2:0]	C_L	–	30	pF
Load Capacitance: SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, RW, TA, TXD[2:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], QSPICLK, GPIO[6:5]	C_L	–	20	pF
Load Capacitance: DDATA[3:0], PST[3:0], PSTCLK	C_L	–	15	pF
Capacitance[5], V_{in} = 0 V, f = 1 MHz	C_{IN}	–	6	pF

1 **8.0 mA:** SCL0, SDA0, SCL1, SDA1, PST[3:0], DDATA[3:0], TDSO, RW, ATA_RST, MCLK1, QSPICS2_MCLK2

2 **4.0 mA:** BUFENB1, BUFENB2, EBUOUT1, SCLKOUT, CMDSDIO, IDE_DIOR, IDE_DIOW, TOUT0, RTS[1:0], TXD[1:0], SCLK[4:1], LRCK[4:1], SDATAO1, SDATAO2, QSPICLK, QSPICS0, QSPICS1_EBUOUT2, QSPICS3, QSPIDOUT, RCK, XTRIM, A[8:1], ATA_CS0, ATA_CS1, ATA_A[2:0]

3 **2.0 mA:** TMS/BKPT, DSI/TDI, TRST/DSCLK

4 SCLK[4:1], SCL0, SCL1, SDA0, SDA1, ATA_DMARQ, ATA_INTRQ, ATA_IORDY

5 Capacitance C_{IN} is periodically sampled rather than 100% tested.

Figure 2 and Table 10 provide the clock timing diagram and timing parameters.

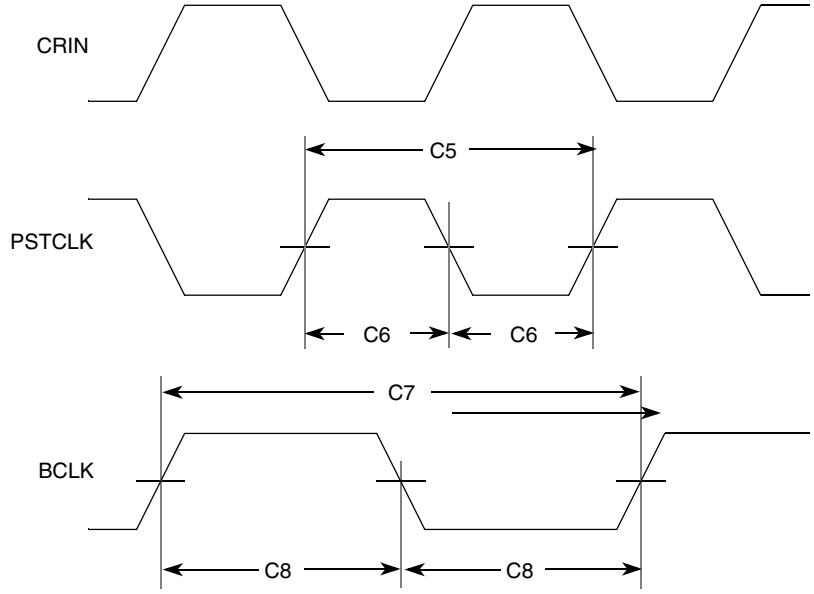


Figure 2. Clock Timing Definition

NOTE

Signals shown in Figure 2 are in relation to the SYSCLK clock. No relationship between signals is implied or intended.

Table 10. Clock Timing Parameters

ID	Characteristic	140 MHz CPU		Units
		Min	Max	
–	CRIN Frequency with external oscillator	5.00	33.86	MHz
–	CRIN Frequency with internal oscillator	5	16.94	MHz
C5	PSTCLK cycle time	7	–	ns
C6	PSTCLK duty cycle	40	60	%
C7	BCLK cycle time	14.0	–	ns
C8	BCLK duty cycle	35	65	%

4.1 SDRAM Bus Timing

The SDRAM bus is a synchronous bus. Propagation delays, set-up times and hold times with respect to the SDRAM clock BCLK are shown in Figure 3 and the parameters provided in Table 11. When BCLK clock is not active, SDRAM interface is not valid and the external bus cannot be used.

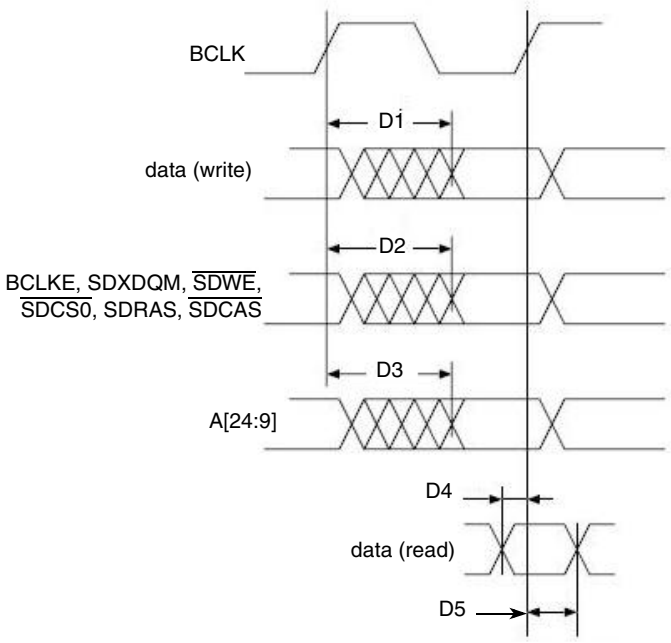


Figure 3. SDRAM Bus Timing Diagram

Table 11. SDRAM Bus Timing Parameters

ID	Characteristic	Timing to 50% Points Maximum			Units
		30 pF Load	40 pF Load	50 pF Load	
D1	Propagation delay BCLK rising to data valid	7.88	8.8	9.6	ns
D2	Propagation delay BCLK rising to BCLKE, SDLDQM, SDUDQM, SDWE, SDCS0, SDRAS, SDCAS valid	8.7	–	–	ns
D3	Propagation delay BCLK rising to A[24:9] valid	8.3	9.2	–	ns
D4	Set-up time data valid to BCLK rising	0	0	0	ns
D5	Hold time BCLK rising to data valid	0.7	0.7	0.7	ns

4.2 SPDIF Timing

The Sony/Philips Digital Interface (SPDIF) timing parameters are provided in Table 12. SPDIF timing is totally asynchronous, therefore there is no need for relationship with the clock. Table 12 shows the differences between high-low and low-high propagation delay which is called the skew.

Table 12. SPDIF Propagation Skew and Transition Parameters

Characteristic	Pin Load	Prop Delay Maximum	Skew[1] Maximum	Transition[2] Rise Maximum	Transition Fall Maximum	Units
EBUIN1, EBUIN2, EBUIN3, EBUIN4: asynchronous inputs, no specs apply	–	–	0.7	–	–	ns
EBUOUT1, EBUOUT2 output	40 pF	–	1.5	24.2	31.3	ns
EBUOUT1, EBUOUT2 output	20 pF	–	1.5	13.6	18.0	ns

1 Skew value does not include the skew introduced by different rise and fall times.

2 Transition times between 10% Vdd and 90% Vdd.

4.3 Serial Audio Interface Timing

The Serial Audio Interface fully complies with the Industry standard Philips IIS (InterIC Serial Audio Bus) timings.

4.4 DDATA/PST/PSTCLK Debug Interface

Table 13 provides the timing parameters.

Table 13. DDATA/PST/PSTCLK Debug Interface Timing Parameters

Characteristic	Pin Load	Min	Max	Units
PSTCLK clock rise edge to DDATA/PSTDATA[1] invalid	15 pF	–1.0	—	ns
PSTCLK clock rise edge to DDATA/PSTDATA[2] valid	15 pF	—	4.0	ns

1 Note that output data may go invalid *before* rising edge of the clock. To clock data in reliably, you need to sample data, for example, 2 ns before rising edge of clock.

2 Timing figure given takes 50% margin for noise and uncertainty on pin capacitance. Simulated clock-to-data, not taking noise effects into account is 2.7 ns.

4.5 BDM and JTAG Timing

Table 14 provides the BDM timing parameters.

Table 14. BDM Interface Timing Parameters

Characteristic	Min	Max	Units
Clock period for DSCLK clock	—	5T[1]	ns
Set-up time DSI, $\overline{\text{BKPT}}$, to DSCLK rising edge	4.0	—	ns
Hold time DSI, $\overline{\text{BKPT}}$ to DSCLK rising edge	—	T+ 4.0	ns
Propagation delay DSCLK rising edge to TDO/DSO change	3T	4T + 32	ns

1 T denotes the CPU clock period. E.g. if the CPU is running at 100 MHz, T = 10 ns

Figure 4 provides the JTAG timing diagram and Table 15 provides the JTAG timing parameters.

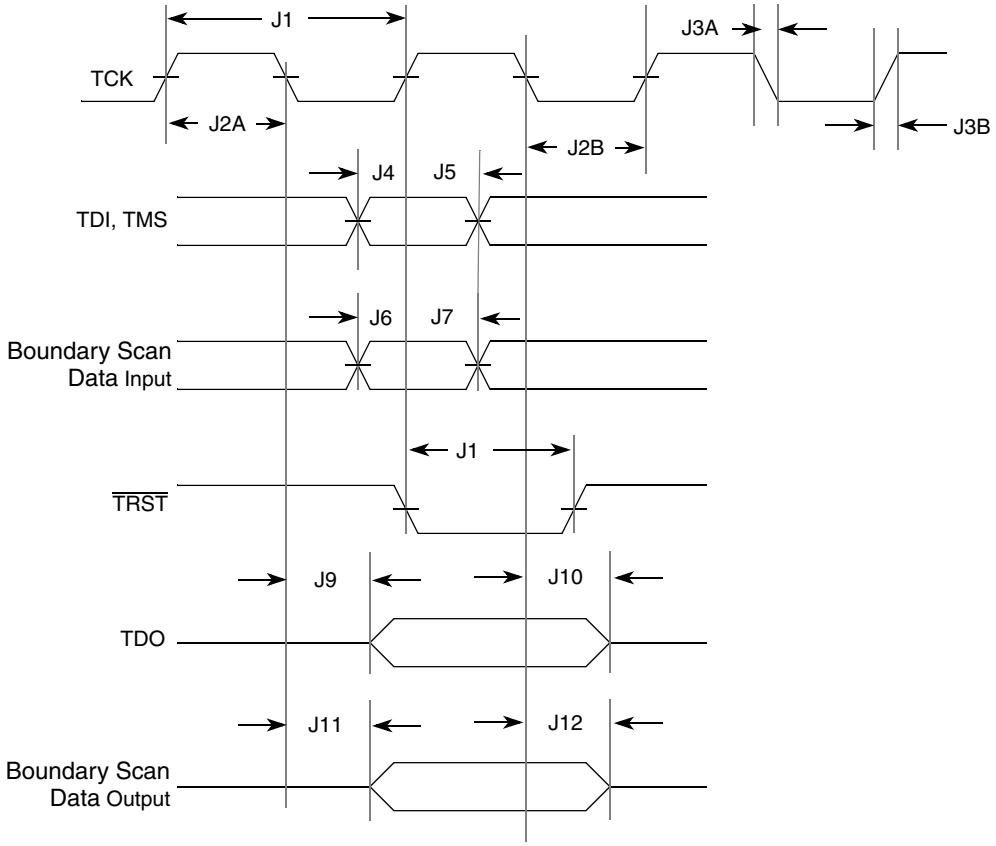


Figure 4. JTAG Timing Diagram

Table 15. JTAG Timing Parameters

ID	Characteristic	Min	Max	Units
–	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	—	ns
J2A	TCK Clock Pulse High Width	25	—	ns
J2B	TCK Clock Pulse Low Width	25	—	ns
J3A	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	—	5	ns
J3B	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	—	5	ns
J4	TDI, TMS to TCK rising (Input Setup)	8	—	ns
J5	TCK rising to TDI, TMS Invalid (Hold)	10	—	ns
J6	Boundary Scan Data Valid to TCK (Setup)	1	—	ns
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	10	—	ns
J8	$\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges)	12	—	ns
J9	TCK falling to TDO Valid (signal from driven or three-state)	—	15	ns
J10	TCK falling to TDO High Impedance	2	15	ns

Table 15. JTAG Timing Parameters (continued)

ID	Characteristic	Min	Max	Units
J11	TCK falling to Boundary Scan Data Valid (signal from driven or three-state)	—	15	ns
J12	TCK falling to Boundary Scan. Data High Impedance	1	15	ns

5 Package Information and Pinout

This section includes the pin assignment information, contact connection diagram, and the mechanical package drawing.

The MCF5251 device is available in the following package:

- 225 MAPBGA 13 x 13 mm 0.8 mm pitch package as shown in Figure 5.

5.1 Pin Assignment

Table 16 defines all the settings of each pad. See Figure 6 for the ball map of pin locations and Table 18 for the device pin list, sorted by signal identification.

Table 16. 225 MAPBGA Pin Assignment

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
Address Bus								
A1	O / 2 mA	30	–	–	–	–	X	–
A2	O / 2 mA	30	–	–	–	–	X	–
A3	O / 2 mA	30	–	–	–	–	X	–
A4	O / 2 mA	30	–	–	–	–	X	–
A5	O / 2 mA	30	–	–	–	–	X	–
A6	O / 2 mA	30	–	–	–	–	X	–
A7	O / 2 mA	30	–	–	–	–	X	–
A8	O / 2 mA	30	–	–	–	–	X	–
A9	O / 8 mA	30	–	–	–	–	X	–
A10	O / 8 mA	30	–	–	–	–	X	–
A11	O / 8 mA	30	–	–	–	–	X	–
A12	O / 8 mA	30	–	–	–	–	X	–
A13	O / 8 mA	30	–	–	–	–	X	–
A14	O / 8 mA	30	–	–	–	–	X	–
A15	O / 8 mA	30	–	–	–	–	X	–
A16	O / 8 mA	30	–	–	–	–	X	–
A17	O / 8 mA	30	–	–	–	–	X	–
A18	O / 8 mA	30	–	–	–	–	X	–
A19	O / 8 mA	30	–	–	–	–	X	–
A20/A24	O / 8 mA	30	A20	A24	31	–	X	Audio Clock Select: 1-LRCK3 pin; 0-CRIN pin
A21	O / 8 mA	30	–	–	–	–	X	–
A22	O / 8 mA	30	–	–	–	–	X	–
A23/GPO54	O / 8 mA	30	A23	–	–	O54	X	Boot Mode Select:1-Memory connected to $\overline{CS0}$; 0-Internal boot rom

Table 16. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
Data Bus								
D16	IO / 8 mA	40	–	–	–	–	HI_Z	–
D17	IO / 8 mA	40	–	–	–	–	HI_Z	–
D18	IO / 8 mA	40	–	–	–	–	HI_Z	–
D19	IO / 8 mA	40	–	–	–	–	HI_Z	–
D20	IO / 8 mA	40	–	–	–	–	HI_Z	–
D21	IO / 8 mA	40	–	–	–	–	HI_Z	–
D22	IO / 8 mA	40	–	–	–	–	HI_Z	–
D23	IO / 8 mA	40	–	–	–	–	HI_Z	–
D24	IO / 8 mA	40	–	–	–	–	HI_Z	–
D25	IO / 8 mA	40	–	–	–	–	HI_Z	–
D26	IO / 8 mA	40	–	–	–	–	HI_Z	–
D27	IO / 8 mA	40	–	–	–	–	HI_Z	–
D28	IO / 8 mA	40	–	–	–	–	HI_Z	–
D29	IO / 8 mA	40	–	–	–	–	HI_Z	–
D30	IO / 8 mA	40	–	–	–	–	HI_Z	–
D31	IO / 8 mA	40	–	–	–	–	HI_Z	–
Bus Control								
$\overline{OE}$	O / 4 mA	30	–	–	–	–	Negated	–
RW	O / 4 mA	30	–	–	–	–	H	–
$\overline{TA}$/GPIO12	IO / 2 mA	30	$\overline{TA}$	–	–	IO12	–	–
$\overline{BUFENB1}$/GPIO29	IO / 2 mA	30	$\overline{BUFENB1}$	–	–	IO29	–	–
$\overline{BUFENB2}$/GPIO30	IO / 2 mA	30	$\overline{BUFENB2}$	–	–	IO30	–	–
$\overline{IDE_DIOR}$/GPIO31	IO / 2 mA	30	$\overline{IDE_DIOR}$	–	–	IO31	–	Controlled by $\overline{CS2}$ registers
$\overline{IDE_DIOW}$/GPIO32	IO / 2 mA	30	$\overline{IDE_DIOW}$	–	–	IO32	–	Controlled by $\overline{CS2}$ registers
$\overline{IDE_IORDY}$/GPIO33	IO / 2 mA	30	$\overline{IDE_IORDY}$	–	–	IO33	–	–
Chip Selects								
$\overline{CS0}$/$\overline{CS4}$	O / 4 mA	30	$\overline{CS0}$	$\overline{CS4}$	–	–	Negated	Boot Mode Select:1-$\overline{CS0}$; 0-$\overline{CS4}$
$\overline{CS1}$/QSPICS3/ GPIO28	IO / 2 mA	30	$\overline{CS1}$	QSPICS3	25	IO28	Negated	–
SDRAM Controller								
BCLK/GPIO40	IO / 8 mA	15	BCLK	–	–	IO40	–	–
BCLKE/GPIO63	IO / 8 mA	20	BCLKE	–	–	IO63	–	–
$\overline{SDLDQM}$/GPO52	O / 8 mA	20	$\overline{SDLDQM}$	–	–	O52	–	–
$\overline{SDUDQM}$/GPO53	O / 8 mA	20	$\overline{SDUDQM}$	–	–	O53	–	–
$\overline{SDWE}$/GPIO38	IO / 8 mA	20	$\overline{SDWE}$	–	–	IO38	Negated	–
$\overline{SDCS0}$/GPIO60	IO / 8 mA	20	$\overline{SDCS0}$	–	–	IO60	Negated	–
$\overline{SDRAS}$/GPIO59	IO / 8 mA	20	$\overline{SDRAS}$	–	–	IO59	Negated	–
$\overline{SDCAS}$/GPIO39	IO / 8 mA	20	$\overline{SDCAS}$	–	–	IO39	Negated	–
ATA Interface								
ATA_A0	O / 2 mA	40	–	–	–	–	–	–
ATA_A1	O / 2 mA	40	–	–	–	–	–	–
ATA_A2	O / 2 mA	40	–	–	–	–	–	–
ATA_D0	IO / 8 mA	40	–	–	–	–	–	–
ATA_D1	IO / 8 mA	40	–	–	–	–	–	–

Table 16. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
ATA_D2	IO / 8 mA	40	–	–	–	–	–	–
ATA_D3	IO / 8 mA	40	–	–	–	–	–	–
ATA_D4	IO / 8 mA	40	–	–	–	–	–	–
ATA_D5	IO / 8 mA	40	–	–	–	–	–	–
ATA_D6	IO / 8 mA	40	–	–	–	–	–	–
ATA_D7	IO / 8 mA	40	–	–	–	–	–	–
ATA_D8	IO / 8 mA	40	–	–	–	–	–	–
ATA_D9	IO / 8 mA	40	–	–	–	–	–	–
ATA_D10	IO / 8 mA	40	–	–	–	–	–	–
ATA_D11	IO / 8 mA	40	–	–	–	–	–	–
ATA_D12	IO / 8 mA	40	–	–	–	–	–	–
ATA_D13	IO / 8 mA	40	–	–	–	–	–	–
ATA_D14	IO / 8 mA	40	–	–	–	–	–	–
ATA_D15	IO / 8 mA	40	–	–	–	–	–	–
ATA_CS0	O / 2 mA	40	–	–	–	–	–	–
ATA_CS1	O / 2 mA	40	–	–	–	–	–	–
ATA_DIOR	O / 8 mA	40	–	–	–	–	–	–
ATA_DIOW	O / 8 mA	40	–	–	–	–	–	–
ATA_IORDY	I	–	–	–	–	–	–	–
ATA_INTRQ	I	–	–	–	–	–	–	–
ATA_DMARQ	I	–	–	–	–	–	–	–
ATA_DMACK	O / 8 mA	40	–	–	–	–	–	–
$\overline{\text{ATA_RST}}$	O / 2 mA	40	–	–	–	–	–	–
Clock Generation								
CRIN	–	–	–	–	–	–	–	Main Processor Clock Input
CROUT	–	–	–	–	–	–	–	Main Processor Clock Output
RTC_CRIN	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Input
RTCCROUT	A	–	–	–	–	–	–	Real Time Clock (32.768 kHz) Output
USB_CRIN	A	–	–	–	–	–	–	USB Clock (24 MHz) Input
USB_CROUT	A	–	–	–	–	–	–	USB Clock (24 MHz) Output
XTRIM/TXD2/GPIO0	IO / 2 mA	30	XTRIM	TXD2	0	IO0	–	Interrupt Capable Input
JTAG/BDM/Test								
TDO/DSO	O / 4 mA	30	–	–	–	–	–	See TEST0 Description
TDI/DSI	I	–	–	–	–	–	–	See TEST0 Description
TMS/$\overline{\text{BKPT}}$	I	–	–	–	–	–	–	See TEST0 Description
TCK	I	–	–	–	–	–	–	–
$\overline{\text{TRST}}$/DSCLK	I	–	–	–	–	–	–	See TEST0 Description
$\overline{\text{HI_Z}}$	I	–	–	–	–	–	–	For Normal Operation Tie This Pin High
PSTCLK/GPIO51	IO / 8 mA	30	PSTCLK	–	–	IO51	–	–
PST0/GPIO50	IO / 4 mA	30	PST0	–	–	IO50	HI_Z	–
PST1/GPIO49	IO / 4 mA	30	PST1	–	–	IO49	HI_Z	–
PST2/INTMON2/ GPIO48	IO / 4 mA	30	PST2	INTMON2	17	IO48	HI_Z	–
PST3/INTMON1/ GPIO47	IO / 4 mA	30	PST3	INTMON1	18	IO47	HI_Z	–

Table 16. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
DDATA0/$\overline{\text{CTS1}}$/ SDATA0_SDIO1/GPIO1	IO / 4 mA	30	DDATA0	$\overline{\text{CTS1}}$/SDATA 0_SDIO1	14,13	IO1	HI_Z	Interrupt Capable Input
DDATA1/$\overline{\text{RTS1}}$/ SDATA2_BS2/GPIO2	IO / 4 mA	30	DDATA1	$\overline{\text{RTS1}}$/SDATA 2_BS2	24,23	IO2	HI_Z	Interrupt Capable Input
DDATA2/$\overline{\text{CTS0}}$/GPIO3	IO / 4 mA	30	DDATA2	$\overline{\text{CTS0}}$	22	IO3	HI_Z	Interrupt Capable Input
DDATA3/$\overline{\text{RTS0}}$/GPIO4	IO / 4 mA	30	DDATA3	$\overline{\text{RTS0}}$	21	IO4	HI_Z	Interrupt Capable Input
TEST0	I	–	–	–	–	–	–	BDM/JTAG Select: 1-BDM; 0-JTAG
TEST1	I	–	–	–	–	–	–	For normal operation, tie this pin low.
TEST2	I	–	–	–	–	–	–	For normal operation, tie this pin low.
Reset/Wake-up								
RSTI	I	–	–	–	–	–	–	–
$\overline{\text{WAKEUP}}$/GPIO21	IO / 2 mA	30	$\overline{\text{WAKEUP}}$	–	–	IO21	–	–
USB								
USBDN	A	–	–	–	–	–	–	–
USBDP	A	–	–	–	–	–	–	–
USBID	I	–	–	–	–	–	–	–
USBVBUS	A	–	–	–	–	–	–	–
USBRES	A	–	–	–	–	–	–	–
TESTOUT[1]	O	–	–	–	–	–	–	–
NC	–	–	–	–	–	–	–	–
Audio Interface								
SDATAI1/GPIO17	IO / 2 mA	30	SDATAI1	–	–	IO17	–	–
SDATAO1/TOUT0/ GPIO18	IO / 2 mA	30	SDATAO1	TOUT0	8	IO18	–	–
SCLK1/GPIO20	IO / 2 mA	30	SCLK1	–	–	IO20	–	–
LRCK1/GPIO19	IO / 2 mA	30	LRCK1	–	–	IO19	–	–
SDATAO2/GPIO34	IO / 2 mA	30	SDATAO2	–	–	IO34	–	–
SCLK2/GPIO22	IO / 2 mA	30	SCLK2	–	–	IO22	–	–
LRCK2/GPIO23	IO / 2 mA	30	LRCK2	–	–	IO23	–	–
SDATAI3/GPIO8	IO / 2 mA	30	SDATAI3	–	–	IO8	–	–
SCLK3/GPIO35	IO / 2 mA	30	SCLK3	–	–	IO35	–	–
LRCK3/AUDIOCLK/ GPIO43	IO / 2 mA	30	LRCK3	AUDIOCLK	–	IO43	–	See A20/A24 Description
EBUIN1/GPIO36	IO / 2 mA	30	EBUIN1	–	–	IO36	–	–
EBUIN2/SCLKOUT/ GPIO13	IO / 2 mA	30	EBUIN2	SCLKOUT	16	IO13	–	–
EBUIN3/ CMD_SDIO2/GPIO14	IO / 2 mA	30	EBUIN3	CMDSDIO2	15	IO14	–	–
QSPICS0/EBUIN4/ GPIO15	IO / 2 mA	30	QSPICS0	EBUIN4	30	IO15	–	–
EBUOUT1/GPIO37	IO / 2 mA	30	EBUOUT1	–	–	IO37	–	–
QSPICS1/ EBUOUT2/GPIO16	IO / 2 mA	30	QSPICS1	EBUOUT2	29	IO16	–	–
CFLG/GPIO5	IO / 2 mA	30	CFLG	–	–	IO5	–	Interrupt Capable Input
EF/RXD2/GPIO6	IO / 2 mA	30	EF	RXD2	–	IO6	–	Interrupt Capable Input

Table 16. 225 MAPBGA Pin Assignment (continued)

Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
MCLK1/GPIO11	IO / 4 mA	30	MCLK1	–	–	IO11	–	–
QSPICS2/MCLK2/ GPIO24	IO / 4 mA	30	QSPICS2	MCLK2	28	IO24	–	–
Analog-to-Digital Converter								
ADIN0/GPI52	A	–	ADIN0	–	–	I52	–	–
ADIN1/GPI53	A	–	ADIN1	–	–	I53	–	–
ADIN2/GPI54	A	–	ADIN2	–	–	I54	–	–
ADIN3/GPI55	A	–	ADIN3	–	–	I55	–	–
ADIN4/GPI56	A	–	ADIN4	–	–	I56	–	–
ADIN5/GPI57	A	–	ADIN5	–	–	I57	–	–
ADREF	A	–	–	–	–	–	–	–
ADOUT/SCLK4/ GPIO58	IO / 2 mA	30	ADOUT	SCLK4	9	IO58	–	–
FlexCAN								
CAN0_TX	O / 8 mA	30	–	–	–	–	–	–
CAN0_RX	I	–	–	–	–	–	–	–
CAN1_TX	O / 8 mA	30	–	–	–	–	–	–
CAN1_RX	I	–	–	–	–	–	–	–
QSPI								
QSPICLK/SUBR/ GPIO25	IO / 2 mA	30	QSPICLK	SUBR	27	IO25	–	–
RCK/QSPIDIN/ QSPIDOUT/GPIO26	IO / 2 mA	30	RCK	QSPIDIN/ QSPIDOUT	26	IO26	–	–
QSPIDOUT/SFSY/ GPIO27	IO / 2 mA	30	QSPIDOUT	SFSY	10	IO27	–	–
I^2C								
SDA0/SDATA3/ GPIO42	IO / 4 mA	30	SDA0	SDATA3	11	IO42	–	–
SCL0/SDATA1_BS1/ GPIO41	IO / 4 mA	30	SCL0	SDATA1_BS1	12	IO41	–	–
SDA1/RXD1/GPIO44	IO / 4 mA	30	SDA1	RXD1	19	IO44	–	–
SCL1/TXD1/GPIO10	IO / 4 mA	30	SCL1	TXD1	20	IO10	–	–
UART								
TXD0/GPIO45	IO / 2 mA	30	TXD0	–	–	IO45	–	–
RXD0/GPIO46	IO / 2 mA	30	RXD0	–	–	IO46	–	–
Power/Ground Pins								
LININ	–	–	–	–	–	–	–	3.3 Volt Supply Required
LINOUT	–	–	–	–	–	–	–	1.2 Volt Output (Approx 50% Efficient)
LINGND	–	–	–	–	–	–	–	–
PLLCOREVDD (3 Balls)	–	–	–	–	–	–	–	1.2 Volt Supply Required (M4, N3, P2)
PLLCOREGND (3 Balls)	–	–	–	–	–	–	–	N4,P3,R2
USBVDD (2 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (L13, M13)
USBVDDP	–	–	–	–	–	–	–	1.2 Volt Supply Required

Table 16. 225 MAPBGA Pin Assignment (continued)

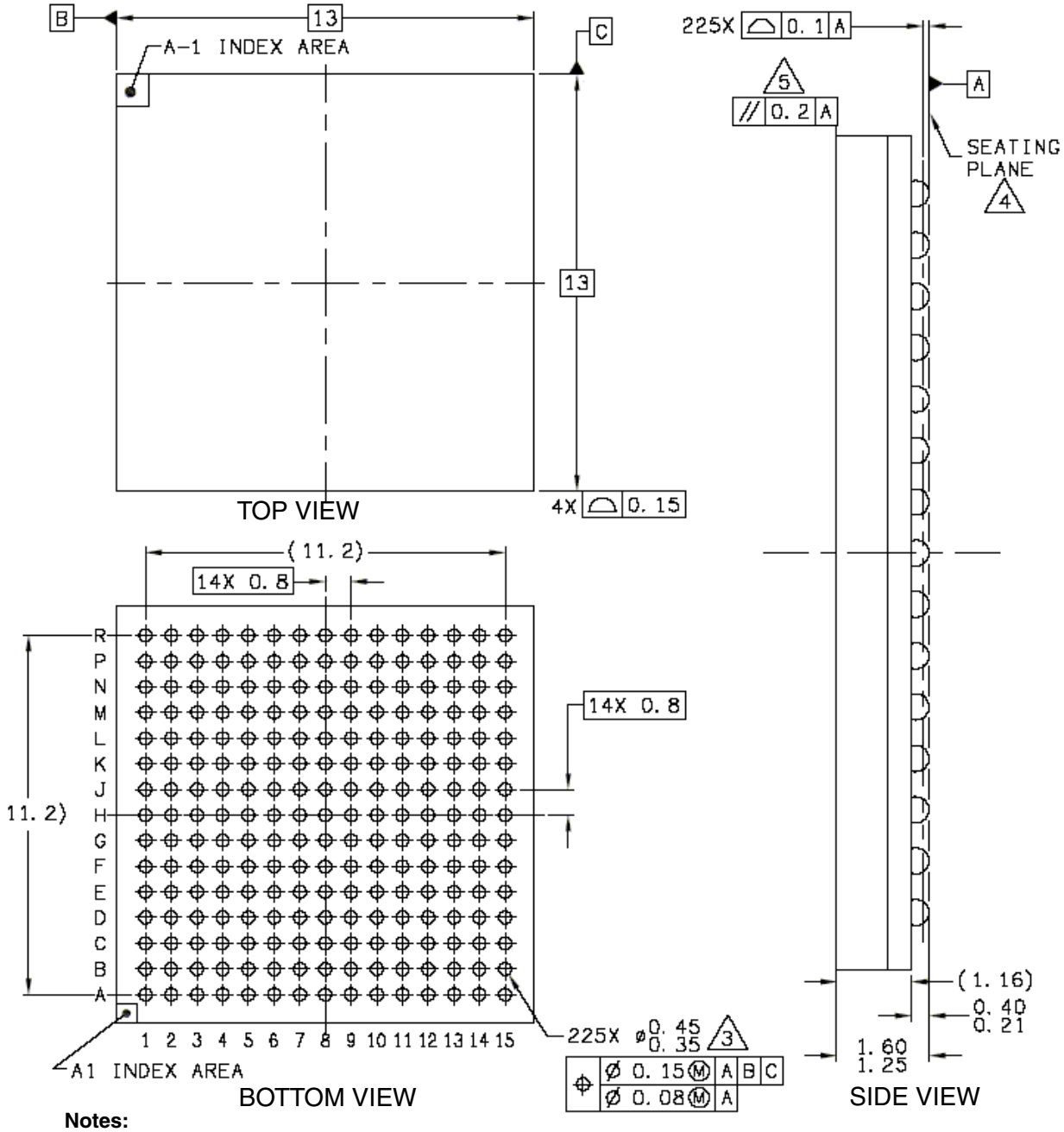
Name	Drive Type/ Strength	Load (pF)	1st Function	2nd Function	Pinconfig Register Bit	GP Pin	Reset	Notes
USBGND (3 Balls)	–	–	–	–	–	–	–	K11, L11, M12
OSCPADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
OSCPADGND	–	–	–	–	–	–	–	–
RTC_VDDA	–	–	–	–	–	–	–	3.3 Volt Supply Required
RTCVSSA	–	–	–	–	–	–	–	–
ADVDD	–	–	–	–	–	–	–	3.3 Volt Supply Required
ADGND	–	–	–	–	–	–	–	–
PADVDD (10 Balls)	–	–	–	–	–	–	–	3.3 Volt Supply Required (E7, E9, F10, H8, H11, K5, L6, L8, L10, R13)
COREVDD (4 Balls)	–	–	–	–	–	–	–	1.2 Volt Supply Required (G8, H7, H9, J8)
COREVSS/PADVSS (18 Balls)[2]	–	–	–	–	–	–	–	A1, A15, E8, E10, F7, G6, G7, G9, G11, J7, J9, J10, J11, L5, L7, L9, R1, R15

[1] For test purposes only. Leave ball as open circuit.

[2] These pads are listed as “GND” in the ball map and the rest of the tables.

5.2 Package Drawing

Figure 5 shows the package outline diagram for the MCF5251 processor.



Notes:

1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M–1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crown of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 5. MCF5251 Package Drawing

5.2.1 MAPBGA Pinout

Figure 6 shows the MCF5251 ball map of pad locations.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	GND	D24	D26	D30	SDUDQM/ GPO53	SDRAS/ GPIO59	ATA_DMARQ	ATA_A0	ATA_D1	ATA_D6	ATA_D11	ATA_D12	ATA_DIOW	LININ	GND	A
B	D19	D23	D25	D28	BCLK/ GPIO40	SDCS0/ GPIO60	ATA_A1	ATA_A2	ATA_D0	ATA_D4	ATA_D9	ATA_D14	HI_Z	LINOUT	ATA_DIOR	B
C	D16	D20	D22	D27	D31	SDLDQM/ GPO52	SDWE/ GPIO38	ATA_RST	ATA_CS0	ATA_D5	ATA_D10	ATA_DMACK	LINGND	CAN1_TX	CAN0_TX	C
D	A22	A23/GPO54	A21	D21	D29	SDCAS/ GPIO39	ATA_IORDY	ATA_INTRQ	ATA_CS1	ATA_D7	ATA_D8	ATA_D15	CAN0_RX	MCLK1/ GPIO11	SDATAO2/ GPIO34	D
E	A14	A16	A18	D17	D18	BCLKE/ GPIO63	PADVDD	GND	PADVDD	GND	ATA_D13	CAN1_RX	SCLK2/ GPIO22	LRCK2/ GPIO23	RSTI	E
F	A13	A10	A12	A17	A19	A20/A24	GND	ATA_D2	ATA_D3	PADVDD	TEST0	TMS/BKPT	TCK	TRST/ DSCLK	TDI/DSI	F
G	A5	A7	A6	A15	A11	GND	GND	COREVDD	GND	TEST1	GND	PST1/ GPIO49	TDO/DSO	PSTCLK/ GPIO51	PST0/ GPIO50	G
H	A3	A2	A1	A8	A4	A9	COREVDD	PADVDD	COREVDD	TEST2	PADVDD	TXD0/ GPIO45	PST3/ INTMON1/ GPIO47	PST2/ INTMON2/ GPIO48	RXD0/ GPIO46	H
J	RTC_CRIN	RTC_VDDA	CS0/CS4	RW	ADOUT/ SCLK4/ GPIO58	ADIN5/ GPI57	GND	COREVDD	GND	GND	GND	DDATA3/ RTS0/ GPIO4	SCL1/TXD1/ GPIO10	DDATA2/ CTS0/ GPIO3	SDA1/RXD1 /GPIO44	J
K	RTCVSSA	RTCCROUT	ADIN0/ GPI52	ADVDD	PADVDD	BUFENB2/ GPIO30	EBUIN3/CMD_SDIO2/ GPIO14	SCLK1/ GPIO20	SDA0/ SDATA3/ GPIO42	DDATA0/ CTS1/SDATA0_SDIO1/ GPIO1	USBGND	N/C	N/C	N/C	N/C	K
L	ADIN1/ GPI53	ADIN2/ GPI54	ADIN3/ GPI55	ADGND	GND	PADVDD	GND	PADVDD	GND	PADVDD	USBGND	USBVDDP	USBVDD	USB_CRIN	USB_CROUT	L
M	ADIN4/ GPI56	ADREF	CRIN	PLLCORE VDD	IDE_DIOR/ GPIO31	EBUIN2/ SCLKOUT/ GPIO13	CS1/ QSPICS3/ GPIO28	QSPIDOUT/ SFSY/ GPIO27	CFLG/ GPIO5	LRCK3/ AUDCLK/ GPIO43	USBID	USBGND	USBVDD	USBRES	USBDP	M
N	OSCPAD VDD	CROUT	PLLCORE VDD	PLLCORE GND	TA/GPIO12	EBUIN1/ GPIO36	RCK/QSPIDIN/QSPIDOUT/GPIO26	QSPICS1/ EBUOUT2/ GPIO16	SDATAI1/ GPIO17	SDATAI3/ GPIO8	N/C	N/C	N/C	USBVBUS	USBDN	N
P	OSCPAD GND	PLLCORE VDD	PLLCORE GND	IDE_DIOW/ GPIO32	BUFENB1/ GPIO29	EBUOUT1/ GPIO37	QSPICLK/ SUBR/ GPIO25	LRCK1/ GPIO19	QSPICS2/ MCLK2/ GPIO24	SCL0/SDATA1_BS1/ GPIO41	N/C	N/C	TESTOUT	N/C	N/C	P
R	GND	PLLCORE GND	OE	IDE_IORDY/ GPIO33	WAKEUP/ GPIO21	XTRIM/ TXD2/ GPIO0	QSPICS0/ EBUIN4/ GPIO15	SDATAO1/ TOUT0/ GPIO18	EF/RXD2/ GPIO6	SCLK3/ GPIO35	DDATA1/RTS1/SDATA2_BS2/ GPIO2	N/C	PADVDD	NC	GND	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 6. MCF5251 Ball Map

Table 17 shows the signal color and signal name legend.

Table 17. Signal Color/Name Legend

Color	Name
None	Signal name as listed
	GND
	PADVDD
	COREVDD
	USBGND

Table 18 shows the device pin list, sorted by signal identification.

Table 18. MCF5251 13 x 13 BGA (225 Signal ID by Pad Grid Location)

Signal ID	Pad Location
A1	H03
A10	F02
A11	G05
A12	F03
A13	F01
A14	E01
A15	G04
A16	E02
A17	F04
A18	E03
A19	F05
A2	H02
A20/A24	F06
A21	D03
A22	D01
A23/GPO54	D02
A3	H01
A4	H05
A5	G01
A6	G03
A7	G02
A8	H04
A9	H06
ADGND	L04
ADIN0/GPI52	K03
ADIN1/GPI53	L01
ADIN2/GPI54	L02
ADIN3/GPI55	L03
ADIN4/GPI56	M01
ADIN5/GPI57	J06
ADOUT/SCLK4/GPIO58	J05
ADREF	M02
ADVDD	K04

Table 18. MCF5251 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
ATA_A0	A08
ATA_A1	B07
ATA_A2	B08
ATA_CS0	C09
ATA_CS1	D09
ATA_D0	B09
ATA_D1	A09
ATA_D10	C11
ATA_D11	A11
ATA_D12	A12
ATA_D13	E11
ATA_D14	B12
ATA_D15	D12
ATA_D2	F08
ATA_D3	F09
ATA_D4	B10
ATA_D5	C10
ATA_D6	A10
ATA_D7	D10
ATA_D8	D11
ATA_D9	B11
ATA_DIOR	B15
ATA_DIOW	A13
ATA_DMACK	C12
ATA_DMARQ	A07
ATA_INTRQ	D08
ATA_IORDY	D07
$\overline{\text{ATA_RST}}$	C08
BCLK/GPIO40	B05
BCLKE/GPIO63	E06
$\overline{\text{BUFENB1}}$/GPIO29	P05
$\overline{\text{BUFENB2}}$/GPIO30	K06
CAN0_RX	D13
CAN0_TX	C15
CAN1_RX	E12
CAN1_TX	C14
CFLG/GPIO5	M09
COREVDD	G08
COREVDD	H07
COREVDD	H09
COREVDD	J08
CRIN	M03
CROUT	N02
$\overline{\text{CS0}}$/$\overline{\text{CS4}}$	J03
$\overline{\text{CS1}}$/QSPICS3/GPIO28	M07
D16	C01

Table 18. MCF5251 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
D17	E04
D18	E05
D19	B01
D20	C02
D21	D04
D22	C03
D23	B02
D24	A02
D25	B03
D26	A03
D27	C04
D28	B04
D29	D05
D30	A04
D31	C05
DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	K10
DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	R11
DDATA2/$\overline{\text{CTS0}}$/GPIO3	J14
DDATA3/$\overline{\text{RTS0}}$/GPIO4	J12
EBUIN1/GPIO36	N06
EBUIN2/SCLKOUT/GPIO13	M06
EBUIN3/CMD_SDIO2/GPIO14	K07
EBUOUT1/GPIO37	P06
EF/RXD2/GPIO6	R09
GND	A01
GND	A15
GND	E08
GND	E10
GND	F07
GND	G06
GND	G07
GND	G09
GND	G11
GND	J07
GND	J09
GND	J10
GND	J11
GND	L05
GND	L07
GND	L09
GND	R01
GND	R15
$\overline{\text{HI_Z}}$	B13
$\overline{\text{IDE_DIOR}}$/GPIO31	M05
$\overline{\text{IDE_DIOW}}$/GPIO32	P04
$\overline{\text{IDE_IORDY}}$/GPIO33	R04

Table 18. MCF5251 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
LINGND	C13
LININ	A14
LINOUT	B14
LRCK1/GPIO19	P08
LRCK2/GPIO23	E14
LRCK3/AUDIOCLK/GPIO43	M10
MCLK1/GPIO11	D14
NC	R14
$\overline{OE}$	R03
OSCPADGND	P01
OSCPADVDD	N01
PADVDD	E07
PADVDD	E09
PADVDD	F10
PADVDD	H08
PADVDD	H11
PADVDD	K05
PADVDD	L06
PADVDD	L08
PADVDD	L10
PADVDD	R13
PLLAVDD	M04
PLLCOREGND	N04
PLLCOREGND	P03
PLLCOREGND	R02
PLLCOREVDD	N03
PLLCOREVDD	P02
PST0/GPIO50	G15
PST1/GPIO49	G12
PST2/INTMON2/GPIO48	H14
PST3/INTMON1/GPIO47	H13
PSTCLK/GPIO51	G14
QSPICLK/SUBR/GPIO25	P07
QSPICS0/EBUIN4/GPIO15	R07
QSPICS1/EBUOUT2/GPIO16	N08
QSPICS2/MCLK2/GPIO24	P09
QSPIDOUT/SFSY/GPIO27	M08
RCK/QSPIDIN/QSPIDOUT/GPIO26	N07
RSTI	E15
RTC_CRIN	J01
RTC_VDDA	J02
RTCCROUT	K02
RTCVSSA	K01
RW	J04
RXD0/GPIO46	H15
SCL0/SDATA1_BS1/GPIO41	P10

Table 18. MCF5251 13 x 13 BGA (225 Signal ID by Pad Grid Location) (continued)

Signal ID	Pad Location
SCL1/TXD1/GPIO10	J13
SCLK1/GPIO20	K08
SCLK2/GPIO22	E13
SCLK3/GPIO35	R10
SDA0/SDATA3/GPIO42	K09
SDA1/RXD1/GPIO44	J15
SDATAI1/GPIO17	N09
SDATAI3/GPIO8	N10
SDATAO1/TOUT0/GPIO18	R08
SDATAO2/GPIO34	D15
$\overline{\text{SDCAS}}$/GPIO39	D06
$\overline{\text{SDCS0}}$/GPIO60	B06
$\overline{\text{SDLDQM}}$/GPO52	C06
$\overline{\text{SDRAS}}$/GPIO59	A06
$\overline{\text{SDUDQM}}$/GPO53	A05
$\overline{\text{SDWE}}$/GPIO38	C07
$\overline{\text{TA}}$/GPIO12	N05
TCK	F13
TDI/DSI	F15
TDO/DSO	G13
TEST0	F11
TEST1	G10
TEST2	H10
TESTOUT	P13
TMS/$\overline{\text{BKPT}}$	F12
$\overline{\text{TRST}}$/DSCLK	F14
TXD0/GPIO45	H12
USB_CRIN	L14
USB_CROUT	L15
USBDN	N15
USBDP	M15
USBGND	K11
USBGND	L11
USBGND	M12
USBID	M11
USBRES	M14
USBVBUS	N14
USBVDD	L13
USBVDD	M13
USBVDDP	L12
$\overline{\text{WAKEUP}}$/GPIO21	R05
XTRIM/TXD2/GPIO0	R06

6 Product Documentation

This section includes the related product documentation and references to information posted on Freescale's external web page.

This document is labeled as the type: Data Sheet: Technical Data. Definitions for all Freescale document types are available at: http://www.freescale.com.

You can also obtain information on the mechanical characteristics of the MCF5251 integrated microprocessor at http://www.freescale.com/digitalaudio.

The following documents are required for a complete description of the device and are necessary for proper design:

MCF5251 Reference Manual (order number: MCF5251RM)

MCF5251 Product Brief (order number: MCF5251PB)

6.1 Revision History

Table 19 summarizes revisions to this document since the release of Rev. 2.1.

Table 19. Revision History

Location	Revision
Table 1	Removed MCF5251CDVM140, MCF5251CEVM140, MCF5251DVM140, MCF5251EVM140.

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