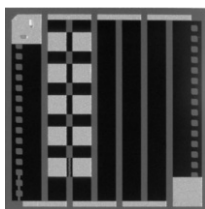


Thin Film Power Resistors

CHIP RESISTORS



Product may not be to scale

The PWB series resistor chips offer a 1 W power rating in a relatively small size. They offer one of the best combinations of size and power available.

The PWBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The PWBs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

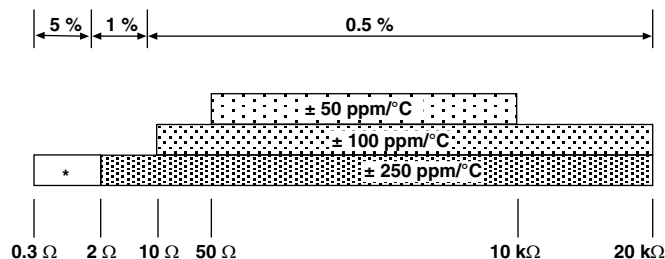
The PWB resistor chips are used mainly in higher power circuits of amplifiers where increased power loads require a more specialized resistor.

FEATURES

- Wire bondable
- Power: 1 W
- Chip size: 0.070 inches square
- Resistance range: 0.3 Ω to 20 k Ω
- Oxidized silicon substrate for good power dissipation
- Resistor material: Tantalum nitride, self-passivating

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES

Tightest Standard Tolerance Available

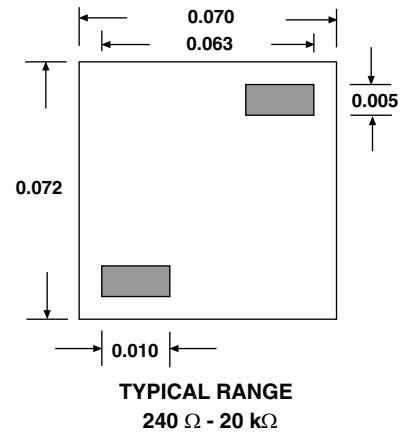
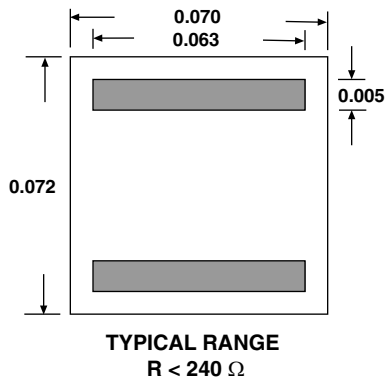


PROCESS CODE	
CLASS H*	CLASS K*
001	005
000	004
008	009

*MIL-PRF-38534 inspection criteria

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Noise, MIL-STD-202, Method 308 100 Ω - 250 k Ω < 100 Ω or > 251 k Ω	- 35 dB typ. - 20 dB typ.
Moisture Resistance, MIL-STD-202 Method 106	± 0.5 % max. $\Delta R/R$
Stability, 1000 h, + 125 $^{\circ}\text{C}$, 500 mW	± 0.5 % max. $\Delta R/R$
Operating Temperature Range	- 55 $^{\circ}\text{C}$ to + 125 $^{\circ}\text{C}$
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 % max. $\Delta R/R$
High Temperature Exposure, + 150 $^{\circ}\text{C}$, 100 h	± 0.2 % max. $\Delta R/R$
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10^{12} min.
Operating Voltage Steady State 5 x Rated Power	100 V max. 200 V max.
DC Power Rating at + 70 $^{\circ}\text{C}$ (Derated to Zero at + 175 $^{\circ}\text{C}$) (Conductive Epoxy Die Sttach to Alumina Substrate)	1 W
5 x Rated Power Short-Time Overload, + 25 $^{\circ}\text{C}$, 5 s	± 0.25 % max. $\Delta R/R$ %

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.070 x 0.070 ± 0.005 (1.781 x 1.781 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.010 (0.127 x 0.254 mm) minimum
Number of Pads	2
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Gold back for eutectic die attach
 Gold bonding pads, 15 kÅ minimum thickness
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 10 kΩ, ± 1 %, ± 100 ppm/°C TCR, aluminum pads, class H visual inspection					
W	PWB	000	1000	1	F
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883		See Process Code table	Use first 4 digits significant digits of the resistance	D = 0.0001 C = 0.001 B = 0.01 A = 0.1 0 = 1 1 = 10	D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %
X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)					



Disclaimer

All product specifications and data are subject to change without notice.

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