

## N-Channel 30-V (D-S) MOSFET

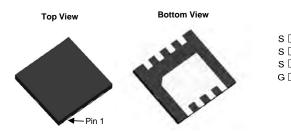
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
30	0.010 at V $_{\rm GS}$ = 10 V	30	26.5 nC			
30	0.018 at V $_{ m GS}$ = 4.5 V	25	20.5 110			

**FEATURES** 

- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested •

#### **APPLICATIONS**

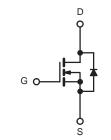
- DC/DC Conversion
  - Low-Side Switch
- Notebook PC
- Gaming



DFN 3x3 EP

Top View			
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N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
	T <sub>C</sub> = 25 °C		30		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C		22.6		
	T <sub>A</sub> = 25 °C	d'	21.5 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1 [	17.1 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	100	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	13		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	'S	3.1 <sup>b, c</sup>		
Single Pulse Avalanche Current         L = 0.1 mH           Avalanche Energy         L = 0.1 mH		I <sub>AS</sub>	10		
		E <sub>AS</sub>	5	mJ	
	T <sub>C</sub> = 25 °C		16.7		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	10.7	W	
Maximum r ower Dissipation	T <sub>A</sub> = 25 °C		3.7 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C	1 [	2.4 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	27	34	°C/W	
Maximum Junction-to-Foot (Drain) Steady State		R <sub>thJF</sub>	6	7.5	0/11	

Notes:

a. Based on  $T_C = 25 \text{ °C}$ . b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 85 °C/W.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 1 mA$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050		27		2400	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I <sub>D</sub> = 250 μΑ		- 5.6		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.0		3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zana Cata Maltana Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ	
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 \text{ °C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	30			А	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.010		Ω	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.018			
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		75		S	
Dynamic <sup>b</sup>	I	•	I	1	<u> </u>		
Input Capacitance	C <sub>iss</sub>			650			
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		236		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			20			
Total Gate Charge	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		10	20	nC	
				4.5	9		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		2.1			
Gate-Drain Charge	Q <sub>gd</sub>			0.7			
Gate Resistance	Rg	f = 1 MHz	0.2	1.1	2.2	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	- ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		16	30		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong$ 10 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		17	35		
Fall Time	t <sub>f</sub>			7	15		
Turn-On Delay Time	t <sub>d(on)</sub>			14	30		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		50	100		
Turn-Off Delay Time	t <sub>d(off)</sub>	$\rm I_D \cong 10$ A, $\rm V_{GEN}$ = 10 V, $\rm R_g$ = 1 $\Omega$		16	30		
Fall Time	t <sub>f</sub>			8	18		
Drain-Source Body Diode Characteristi	cs						
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			13	^	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A		Ī	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>				40	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C			20	nC	
Reverse Recovery Fall Time	ta	$r_{\rm F} = 10$ A, $u/u_{\rm I} = 100$ A/µs, $r_{\rm J} = 25$ °C		12.5			
Reverse Recovery Rise Time	t <sub>b</sub>	1		7.5		ns	

Notes:

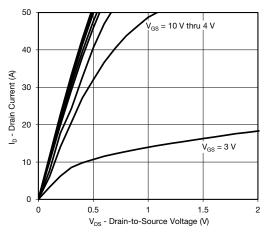
a. Pulse test; pulse width  $\leq$  300  $\mu s$ , duty cycle  $\leq$  2 % b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

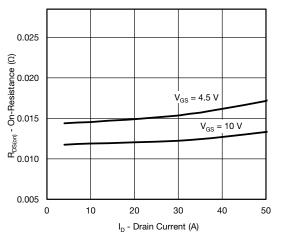
emi



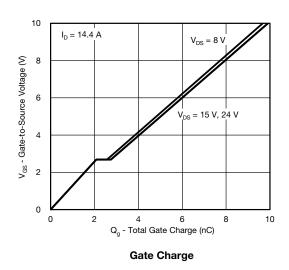
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

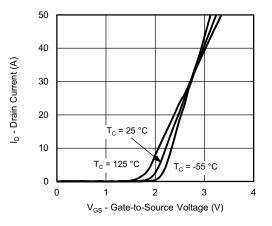


**Output Characteristics** 

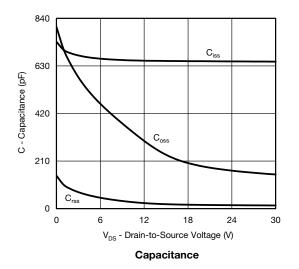


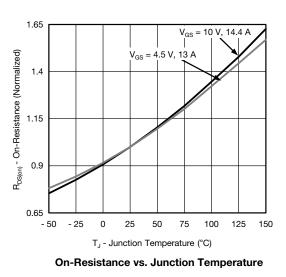
**On-Resistance vs. Drain Current** 





**Transfer Characteristics** 

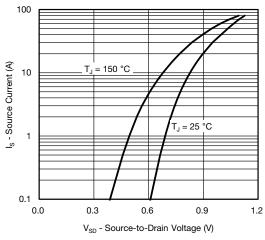




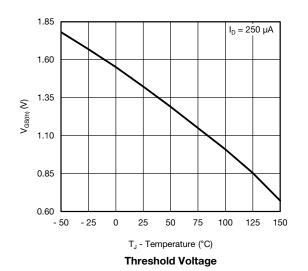
### SI7326DN-T1-GE3



#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



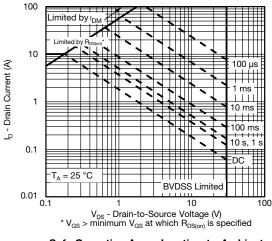
Source-Drain Diode Forward Voltage



0.025 I<sub>D</sub> = 15 A 0.020  $R_{DS(on)}$  - On-Resistance  $(\Omega)$ 0.015 0.010 0.005 T<sub>J</sub> = 25 °C 0.000 2 0 1 3 4 5 6 7 8 9 10 V<sub>GS</sub> - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage

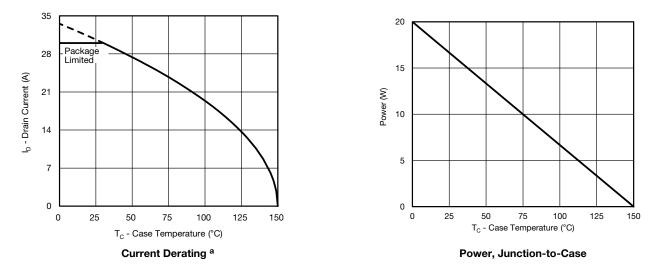




Safe Operating Area, Junction-to-Ambient



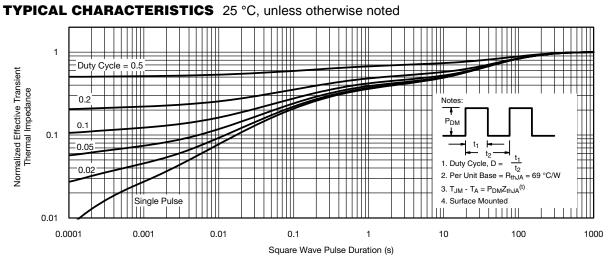
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



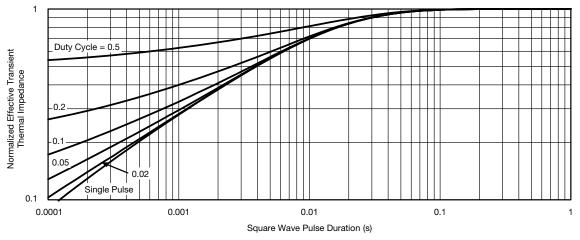
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## SI7326DN-T1-GE3



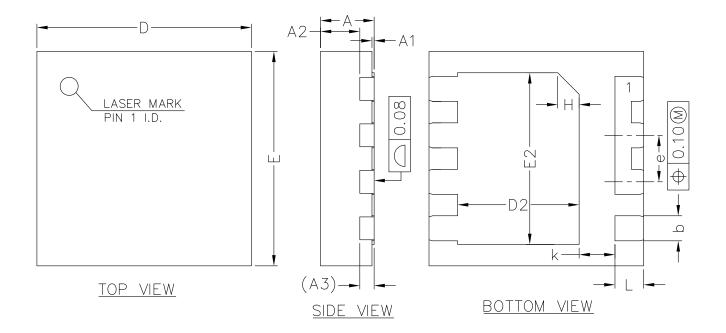
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

semi







<u>SIDE VIEW</u>

SYMBOL	MIN	NOM	MAX		
А	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
А3	0.20REF				
b	0.30	0.35	0.40		
D	2.90	3.00	3.10		
E	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
К	0.40	0.50	0.60		
L	0.35	0.40	0.45		

# COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)



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