- **Organization**
  TM893NBM36H/I . . . 8 388 608 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Leadless Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM893NBM36H/I – Uses Sixteen 16M-Bit and Eight 4M-Bit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  32 ms (2 048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Present Detect**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'893NBM36H/I-60	60 ns	30 ns	15 ns	110 ns
'893NBM36H/I-70	70 ns	35 ns	18 ns	130 ns
'893NBM36H/I-80	80 ns	40 ns	20 ns	150 ns

- **Gold-Tabbed Versions Available:†**
  TM893NBM36H
- **Tin-Lead (Solder)-Tabbed Versions Available:**
  TM893NBM36I

description

The TM893NBM36H/I is a 32M-byte dynamic random-access memory (DRAM) organized as four times 8 388 608 × 9 (bit 9 is generally used for parity) in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS417400ADJ 4 194 304 × 4-bit DRAMs, each in a 24/26-lead plastic SOJ package, and eight TMS44100DJ 4 194 304 × 1-bit DRAMs, each in a 20/26-lead plastic SOJ package, mounted on a substrate with decoupling capacitors. The TMS417400ADJ and TMS44100DJ are described in the TMS417400A (literature number SMKS889) and TMS44100 (literature number SMHS561) data sheets, respectively. The TM893NBM36A SIMM is available in the double-sided, BM leadless module for use with sockets.

operation

The TM893NBM36H/I operates as sixteen TMS417400ADJ DRAMs and eight TMS44100DJ DRAMs connected as shown in the functional block diagram and in Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

Table 1. Connection Table

DATA BLOCK	$\overline{RAS}$x		$\overline{CAS}$x
	SIDE 1	SIDE 2	
DQ0–DQ8	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ9–DQ17	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ18–DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Part numbers in this data sheet refer only to the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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refresh

The refresh period is extended to 32 ms, and, during this period, each of the 2048 rows must be strobed with $\overline{RAS}$ to retain data. Address line A10 must be used as the most significant refresh address line (lowest frequency) to ensure correct refresh for both TMS417400A and TMS44100. Address lines A0–A9 must be refreshed every 16 ms as required by the TMS44100 DRAM. To conserve power, $\overline{CAS}$ can remain high during the refresh sequence.

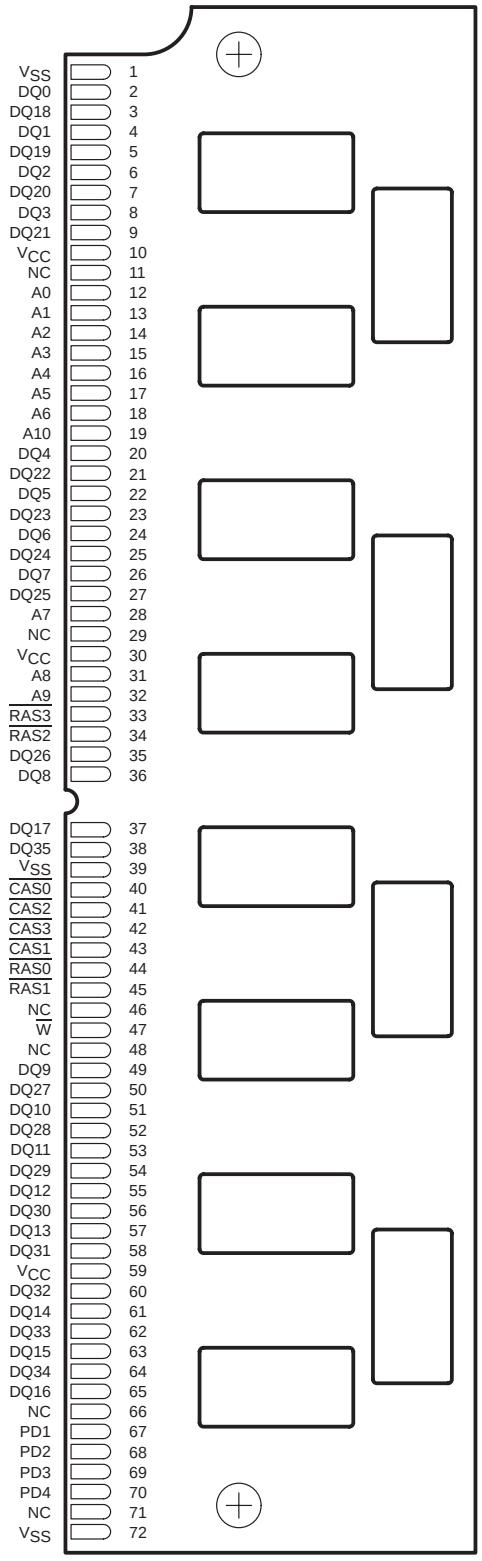
power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles must include at least one refresh ($\overline{RAS}$-only or CBR-refresh) cycle.

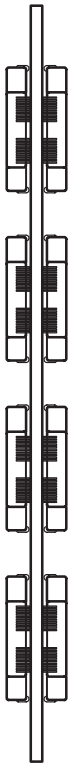
single in-line memory module and components

PC substrate: 1, 27 ± 0,1 mm (0.05 inch) nominal thickness; inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM893NBM36H: Nickel plate and gold plate over copper
Contact area for TM893NBM36I: Nickel plate and tin/lead over copper

BM SINGLE IN-LINE PACKAGE
(TOP VIEW)



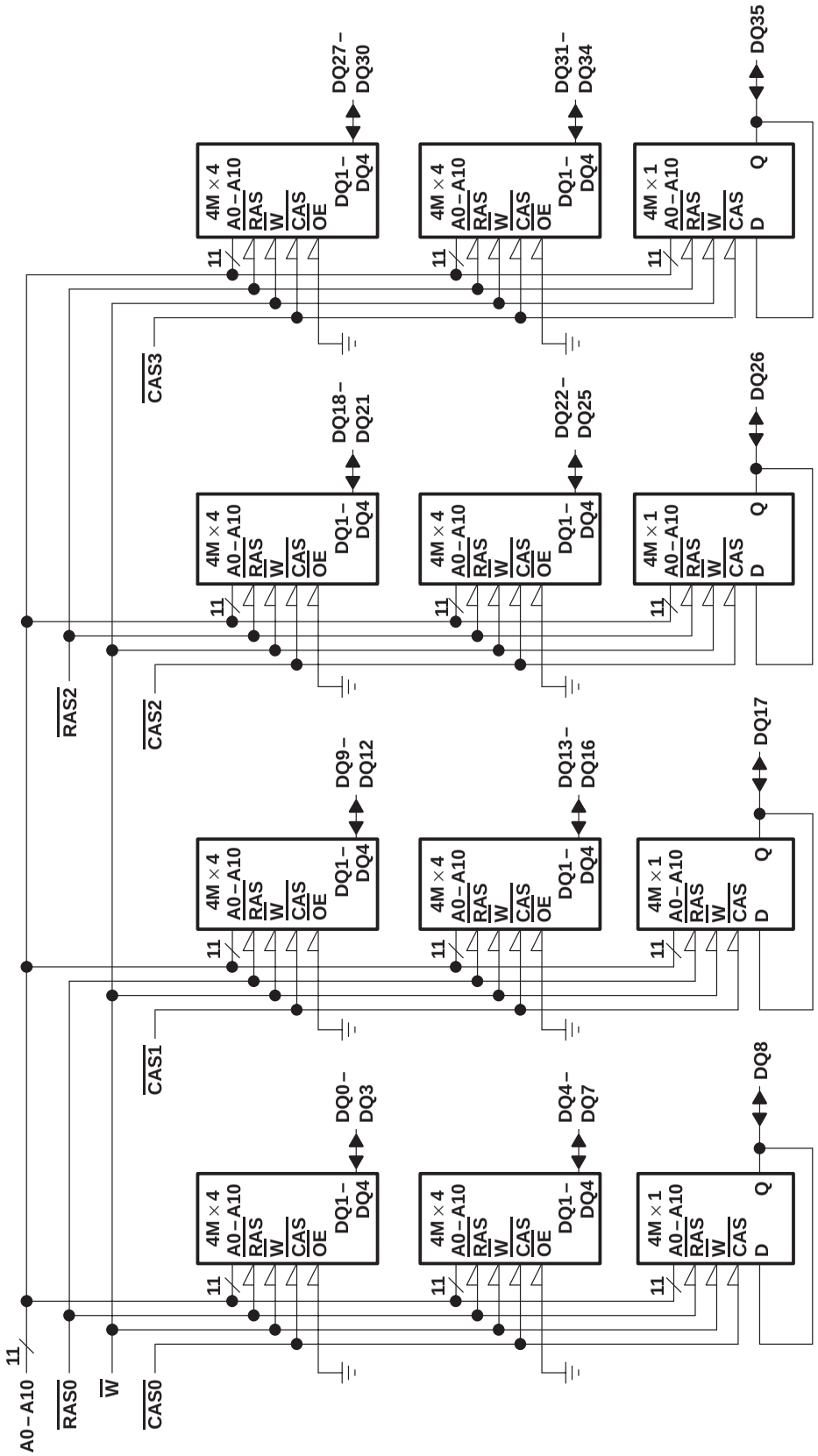
TM893NBM36H/I
(SIDE VIEW)



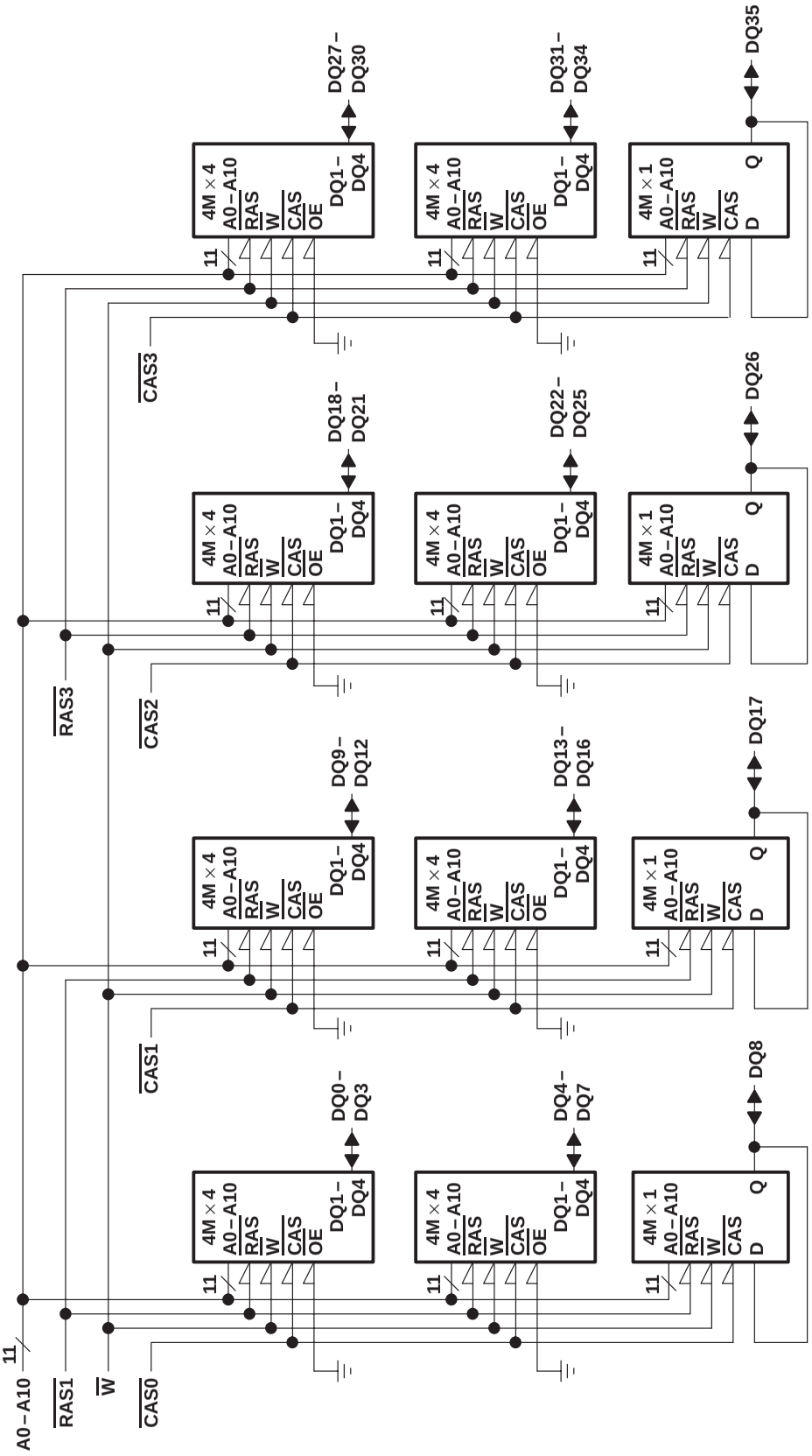
PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM893NBM36H/I	80 ns	NC	V_{SS}	NC	V_{SS}
	70 ns	NC	V_{SS}	V_{SS}	NC
	60 ns	NC	V_{SS}	NC	NC

functional block diagram (TM893NBM36H/I, side 1)



functional block diagram (TM893NBM36H/I, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM893NBM36H, TM893NBM36I . . . . . 24 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†	'893NBM36H/I-60		'893NBM36H/I-70		'893NBM36H/I-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (one $\overline{RAS}$ active, see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1324		1184		1064	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		48		48		48	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		24		24		24	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR, see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1324		1184		1064	mA
I_{CC4}	Average page current (one $\overline{RAS}$ active, see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		944		824		704	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 5)

PARAMETER			'893NMB36H/I		UNIT
			MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10			120	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs			42	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs			42	pF
$C_{i(W)}$	Input capacitance, write-enable input			168	pF
$C_{o(DQ)}$	Output capacitance	DQ pins		14	pF
		Parity pins		24	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'893NBM36H/I-60		'893NBM36H/I-70		'893NBM36H/I-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ low to output in the low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'893NBM36H/I-60		'893NBM36H/I-70		'893NBM36H/I-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

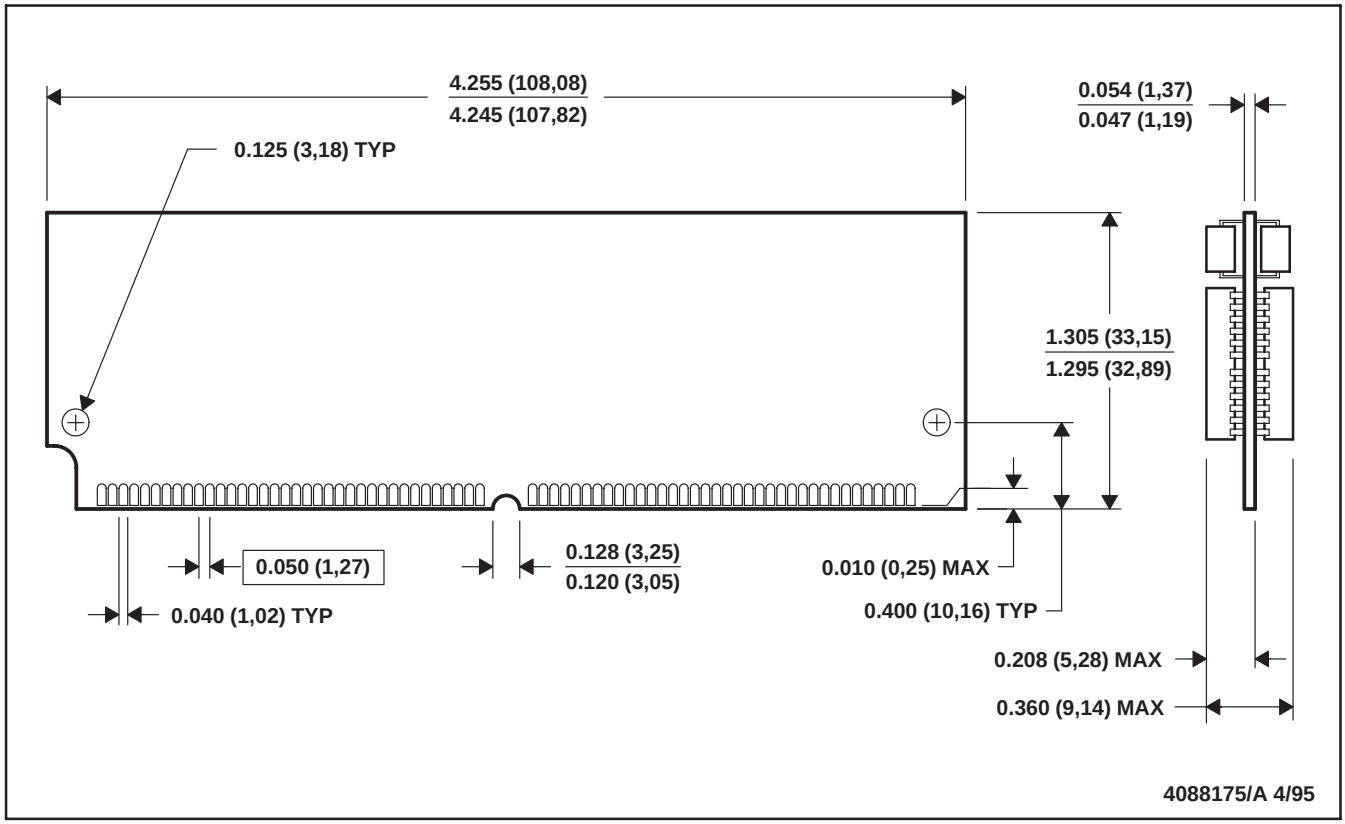
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’893NBM36H/I-60		’893NBM36H/I-70		’893NBM36H/I-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR refresh only)	5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

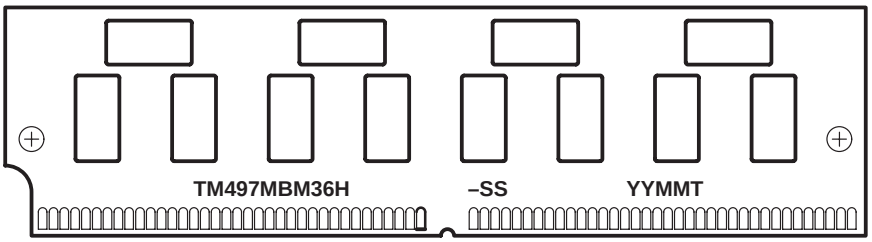
MECHANICAL DATA

BM (R-PSIM-N72) **SINGLE/DOUBLE-SIDED IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization (TM497MBM36H illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

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