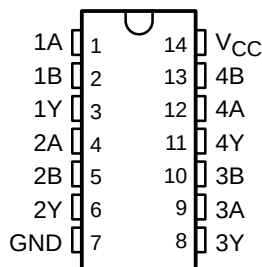


SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

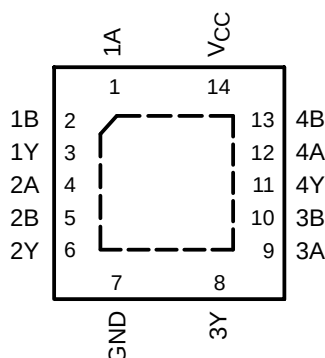
SCLS365G – MAY 1997 – REVISED SEPTEMBER 2002

- Operating Range 2-V to 5.5-V V_{CC}
- Operation From Very Slow Input Transitions
- Temperature-Compensated Threshold Levels
- High Noise Immunity
- Same Pinouts as 'AHC00
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

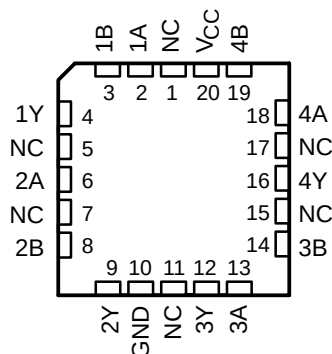
SN54AHC132 ... J OR W PACKAGE
SN74AHC132 ... D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHC132 ... RGY PACKAGE
(TOP VIEW)



SN54AHC132 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'AHC132 devices are quadruple positive-NAND gates designed for 2-V to 5.5-V V_{CC} operation.

These devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC132RGYR	HA132
	PDIP – N	Tube	SN74AHC132N	SN74AHC132N
	SOIC – D	Tube	SN74AHC132D	AHC132
		Tape and reel	SN74AHC132DR	
	SOP – NS	Tape and reel	SN74AHC132NSR	AHC132
	SSOP – DB	Tape and reel	SN74AHC132DBR	HA132
	TSSOP – PW	Tape and reel	SN74AHC132PWR	HA132
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHC132DGV	HA132
	CDIP – J	Tube	SNJ54AHC132J	SNJ54AHC132J
	CFP – W	Tube	SNJ54AHC132W	SNJ54AHC132W
	LCCC – FK	Tube	SNJ54AHC132FK	SNJ54AHC132FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
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SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS365G – MAY 1997 – REVISED SEPTEMBER 2002

description/ordering information (continued)

Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals.

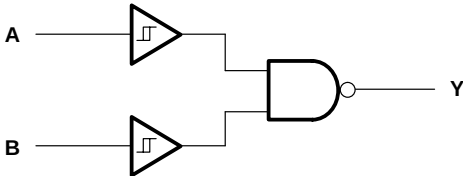
These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean jitter-free output signals.

FUNCTION TABLE

(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS365G – MAY 1997 – REVISED SEPTEMBER 2002

recommended operating conditions (see Note 4)

			SN54AHC132		SN74AHC132		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50		–50		μA
		V _{CC} = 3.3 V ± 0.3 V	–4		–4		mA
		V _{CC} = 5 V ± 0.5 V	–8		–8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 3.3 V ± 0.3 V	4		4		mA
		V _{CC} = 5 V ± 0.5 V	8		8		
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^{\circ}\text{C}$			SN54AHC132		SN74AHC132		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage		3 V	1.2		2.2	1.2	2.2	1.2	2.2	V
		4.5 V	1.75		3.15	1.75	3.15	1.75	3.15	
		5.5 V	2.15		3.85	2.15	3.85	2.15	3.85	
V_{T-} Negative-going input threshold voltage		3 V	0.9		1.9	0.9	1.9	0.9	1.9	V
		4.5 V	1.35		2.75	1.35	2.75	1.35	2.75	
		5.5 V	1.65		3.35	1.65	3.35	1.65	3.35	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		3 V	0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5 V	0.4		1.4	0.4	1.4	0.4	1.4	
		5.5 V	0.5		1.6	0.5	1.6	0.5	1.6	
V_{OH}	$I_{OH} = -50\text{ }\mu\text{A}$	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		2.48		
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50\text{ }\mu\text{A}$	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V			0.36		0.5		0.44	
	$I_{OL} = 8\text{ mA}$	4.5 V			0.36		0.5		0.44	
I_I	$V_I = 5.5\text{ V}$ or GND	0 V to 5.5 V			± 0.1		$\pm 1^*$		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20		20	μA
C_i	$V_I = V_{CC}$ or GND	5 V		1.9	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0\text{ V}$.

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SN54AHC132, SN74AHC132

QUADRUPLE POSITIVE-NAND GATES

WITH SCHMITT-TRIGGER INPUTS

SCLS365G – MAY 1997 – REVISED SEPTEMBER 2002

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	5.6*	11.9*	1*	14*	1	14	14	ns
t_{PHL}				5.6*	11.9*	1*	14*	1	14	14	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	7.6	15.4	1	17.5	1	17.5	17.5	ns
t_{PHL}				7.6	15.4	1	17.5	1	17.5	17.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC132		SN74AHC132		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	3.9*	7.7*	1*	9*	1	9	9	ns
t_{PHL}				3.9*	7.7*	1*	9*	1	9	9	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	5.3	9.7	1	11	1	11	11	ns
t_{PHL}				5.3	9.7	1	11	1	11	11	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74AHC132			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.45	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.35	-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.8			V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5		V

NOTE 5: Characteristics are for surface-mount packages only.

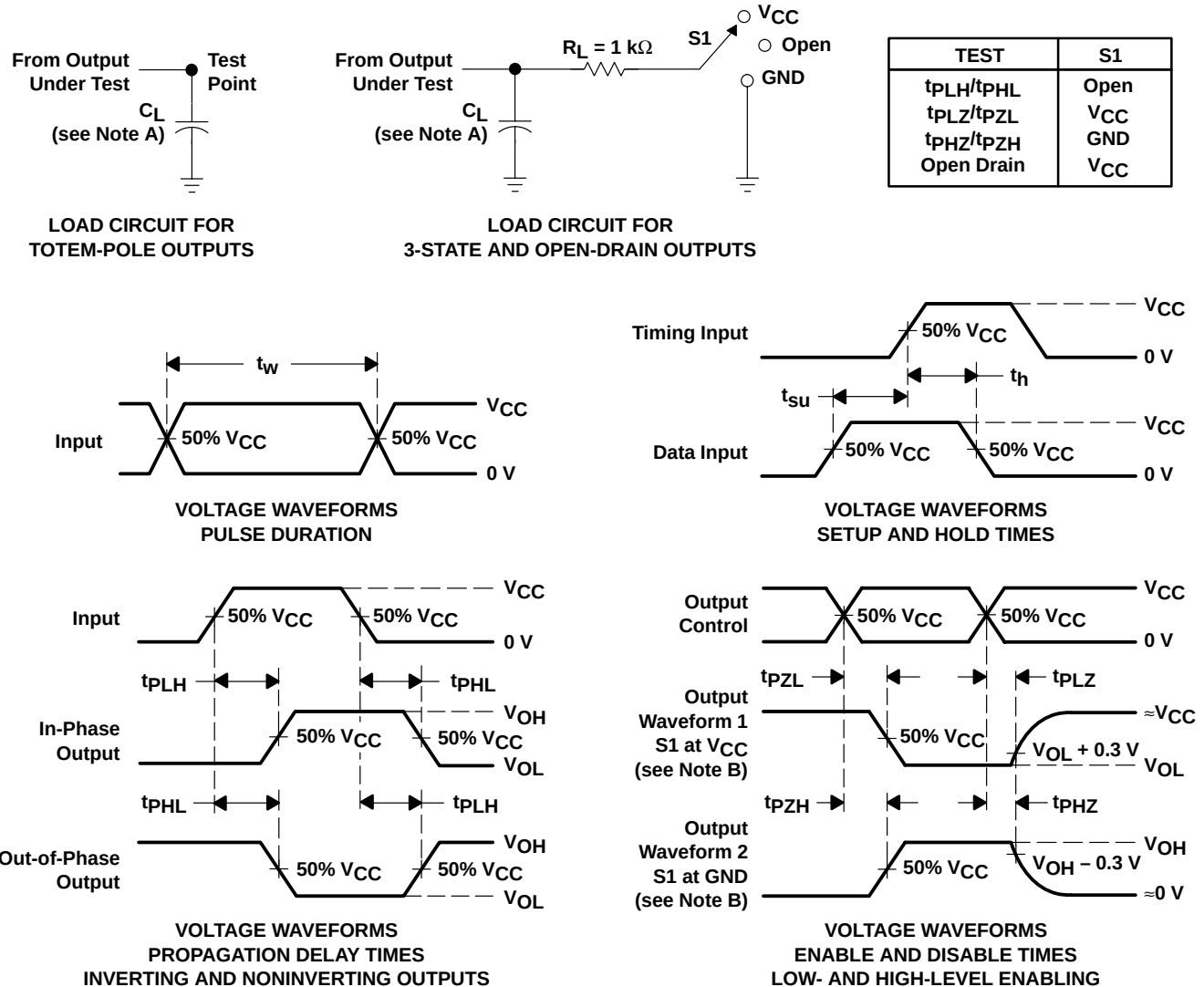
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	11	pF

SN54AHC132, SN74AHC132 QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS

SCLS365G – MAY 1997 – REVISED SEPTEMBER 2002

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC132	Samples
SN74AHC132DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA132	Samples
SN74AHC132DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC132	Samples
SN74AHC132DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA132	Samples
SN74AHC132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC132	Samples
SN74AHC132DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC132	Samples
SN74AHC132N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC132N	Samples
SN74AHC132NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC132N	Samples
SN74AHC132NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC132	Samples
SN74AHC132PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA132	Samples
SN74AHC132PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA132	Samples
SN74AHC132PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA132	Samples
SN74AHC132RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HA132	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

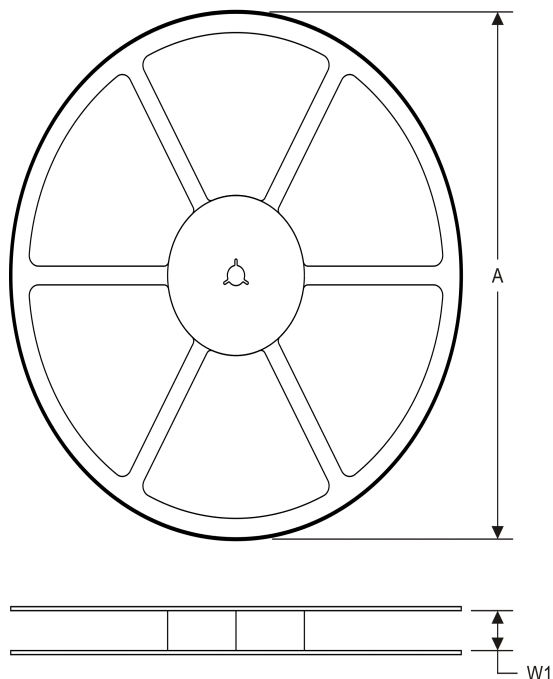
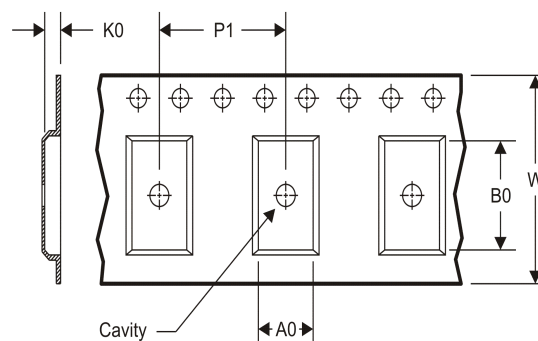
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


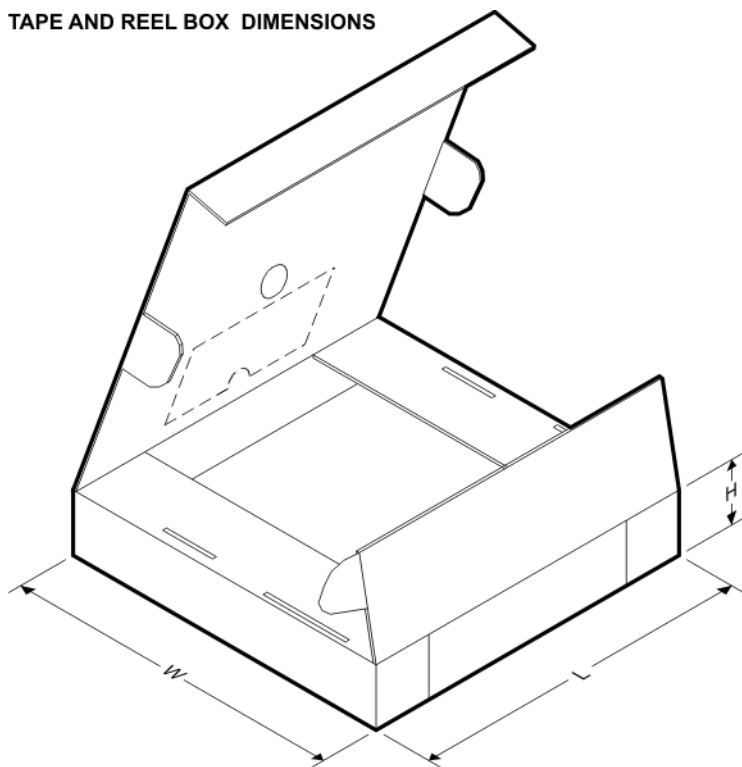
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC132DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC132DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC132NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC132PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC132RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC132DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHC132DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74AHC132DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHC132NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AHC132PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AHC132RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

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