NL27WZ00

Dual 2-Input NAND Gate

The NL27WZ00 is a high performance dual 2−input NAND Gate operating from a 1.65 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.4 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- LVTTL Compatible − Interface Capability With 5.0 V TTL Logic with V_{CC} = 3.0 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ00
- Chip Complexity: FET = 112
- Pb−Free Package is Available

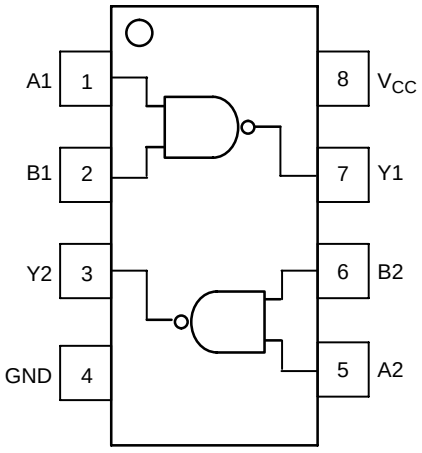

Figure 1. Pinout

Figure 2. Logic Symbol

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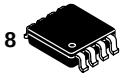
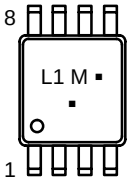
http://onsemi.com

MARKING DIAGRAM



US8
US SUFFIX
CASE 493



L1 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V_{CC}

FUNCTION TABLE

Y = $\overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	−0.5 to +7.0	V
DC Input Voltage		V_I	−0.5 to +7.0	V
DC Output Voltage		V_O	−0.5 to +7.0	V
DC Input Diode Current	V_I < GND	I_{IK}	−50	mA
DC Output Diode Current	V_O < GND	I_{OK}	−50	mA
DC Output Sink Current		I_O	±50	mA
DC Supply Current per Supply Pin		I_{CC}	±100	mA
DC Ground Current per Ground Pin		I_{GND}	±100	mA
Storage Temperature Range		T_{STG}	−65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds		T_L	260	°C
Junction Temperature under Bias		T_J	+150	°C
Thermal Resistance (Note 1)		θ_{JA}	250	°C/W
Power Dissipation in Still Air at 85°C		P_D	250	mW
Moisture Sensitivity		MSL	Level 1	
Flammability Rating	Oxygen Index: 28 to 34	F_R	UL 94 V−0 @ 0.125 in	
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	> 2000 > 200 N/A	V
Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	$I_{Latchup}$	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Max	Unit
Supply Voltage	Operating Data Retention Only	V_{CC}	1.65 1.5	5.5 5.5	V
Input Voltage (Note 6)		V_I	0	5.5	V
Output Voltage	(HIGH or LOW State)	V_O	0	V_{CC}	V
Operating Free−Air Temperature		T_A	−40	+85	°C
Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	$\Delta t/\Delta V$	0 0 0	20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high− or low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Parameter	Condition	Symbol	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
High−Level Input Voltage		V_{IH}	1.65 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V
Low−Level Input Voltage		V_{IL}	1.65 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 0.3 V_{CC}	V
High−Level Output Voltage V_{IN} = V_{IL} or V_{IH}	I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	V_{OH}	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.5 2.1 2.4 2.7 2.5 4.0		V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
Low−Level Output Voltage V_{IN} = V_{IH} or V_{OH}	I_{OL} = 100 μA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	V_{OL}	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.0 0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
Input Leakage Current	V_{IN} = V_{CC} or GND	I_{IN}	0 to 5.5			±0.1		±1.0	μA
Quiescent Supply Current	V_{IN} = V_{CC} or GND	I_{CC}	5.5			1.0		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Parameter	Condition	Symbol	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
Propagation Delay (Figure 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	t_{PLH} t_{PHL}	1.8 ± 0.15	2.0	5.7	10.5	2.0	11.0	ns
			2.5 ± 0.2	1.2	3.2	5.3	1.2	5.7	
	R_L = 1 MΩ, C_L = 15 pF		3.3 ± 0.3	0.8	2.4	3.7	0.8	4.0	
	R_L = 500 Ω, C_L = 50 pF			1.2	3.0	4.6	1.2	4.9	
	R_L = 1 MΩ, C_L = 15 pF		5.0 ± 0.5	0.5	1.9	2.9	0.5	3.2	
	R_L = 500 Ω, C_L = 50 pF			0.8	2.4	3.6	0.8	3.9	

CAPACITIVE CHARACTERISTICS

Parameter	Condition	Symbol	Typical	Unit
Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	C_{IN}	2.5	pF
Power Dissipation Capacitance (Note 7)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	C_{PD}	9 11	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no−load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}.

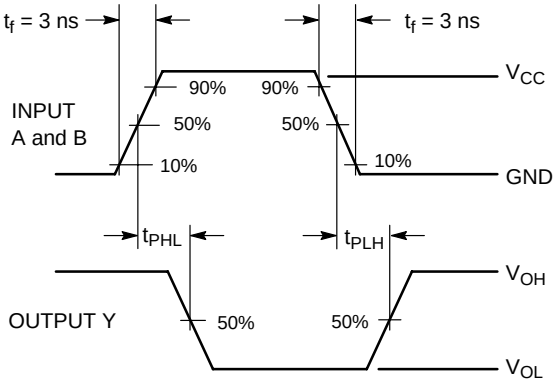


Figure 3. Switching Waveform

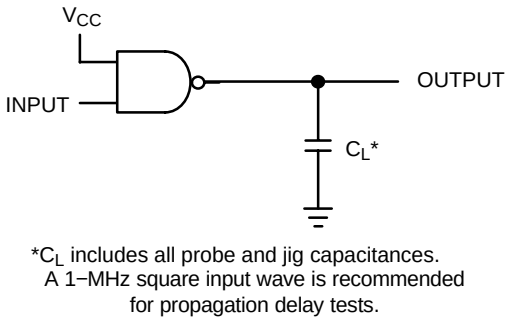


Figure 4. Test Circuit

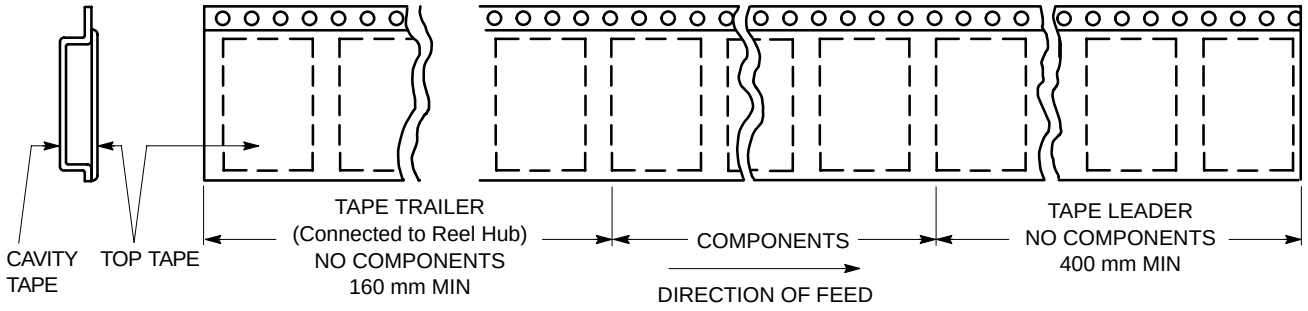


Figure 5. Tape Ends for Finished Goods

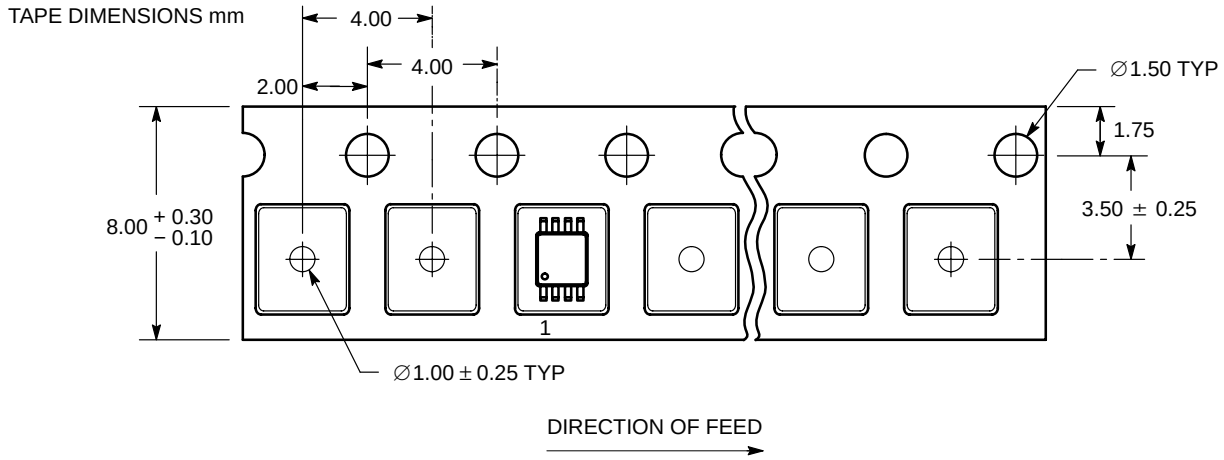


Figure 6. US8 Reel Configuration/Orientation

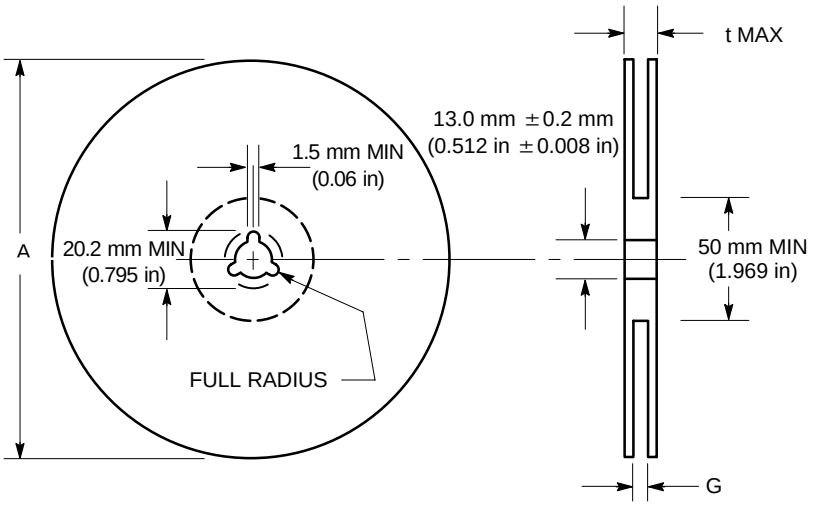


Figure 7. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, −0.0 (0.33 in + 0.059 in, −0.00)	14.4 mm (0.56 in)

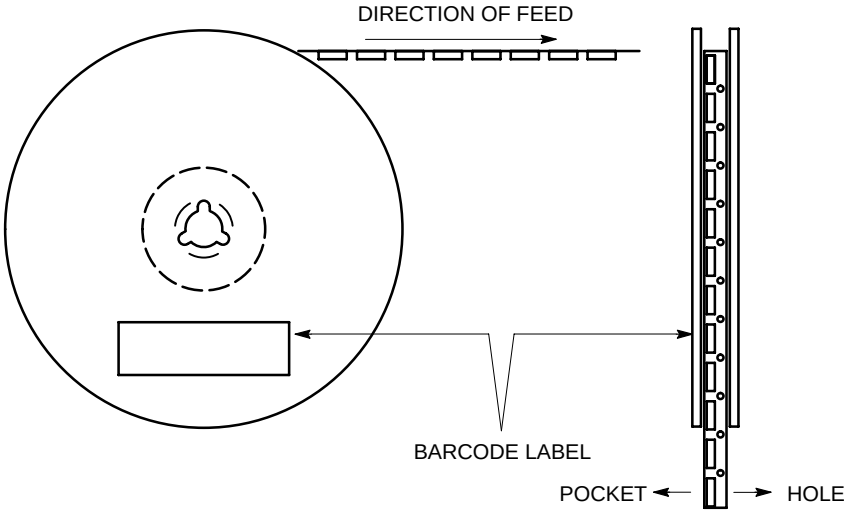


Figure 8. Reel Winding Direction

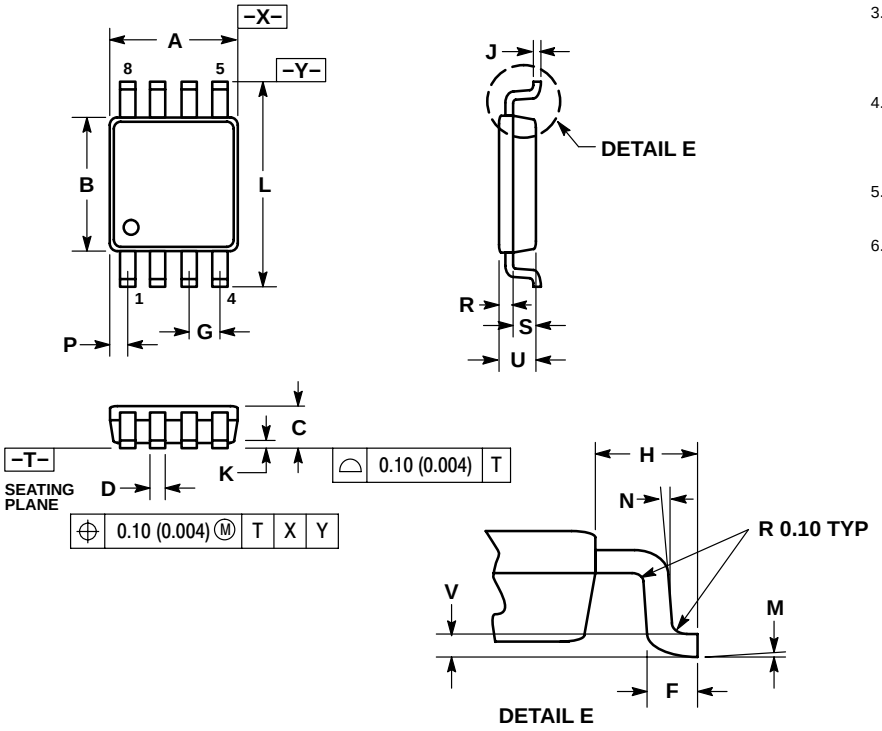
ORDERING INFORMATION

Device	Device Nomenclature						Package	Shipping†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL27WZ00US	NL	2	7	WZ	00	US	US8	3000/Tape & Reel
NL27WZ00USG								

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

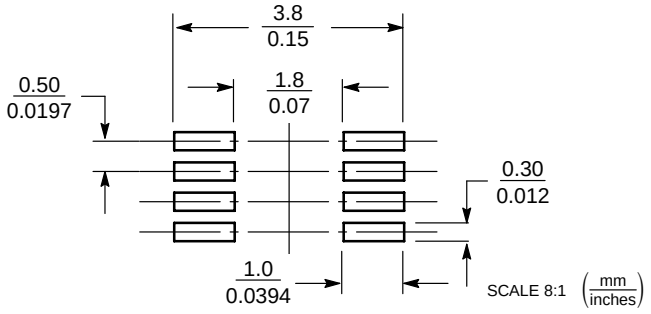
US8
CASE 493−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055”) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSION. INTER−LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055”) PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203 MM. (300−800 “).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 “).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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