SC561

Dual Output Low Noise LDO Linear Regulator

POWER MANAGEMENT

Features

- Input voltage range — 2.5V to 5.5V
- Output voltage — V_{LDOA} = 3.1V; V_{LDOB} = 2.85V
- Maximum output current — 300mA (each LDO)
- Dropout at 200mA load — 200mV max.
- Quiescent supply current — 40µA (both LDOs enabled)
- Shutdown current — 100nA (typ)
- Output noise < 50µV_{RMS}
- PSRR >65dB at 1kHz
- Over-temperature protection
- Short-circuit protection
- Under-voltage lockout
- Power good monitor for output A
- MLPQ-UT8, 1.5mm x 1.5mm x 0.6mm package

Applications

- PDAs and cellular phones
- GPS devices
- Palmtop computers and handheld instruments
- TFT/LCD applications
- Wireless handsets
- Digital cordless phones and PCS phones
- Personal communicators
- Wireless LAN

Description

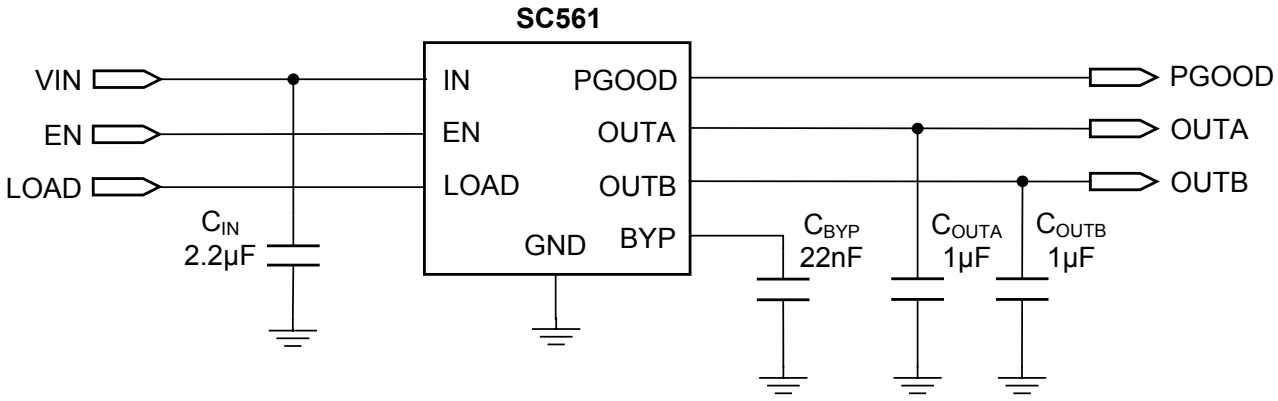
The SC561 is a dual output, ultra-low dropout linear voltage regulator designed for use in battery powered applications. The SC561 provides fixed output voltages of V_{LDOA} = 3.1V and V_{LDOB} = 2.85V, and up to 300mA of load current per channel.

In applications where maximum battery life is essential, the SC561 can operate in an extremely low power state by setting the dynamic bias control. At very light loads, the LOAD pin can be pulled low so that the device consumes only 40µA of quiescent current.

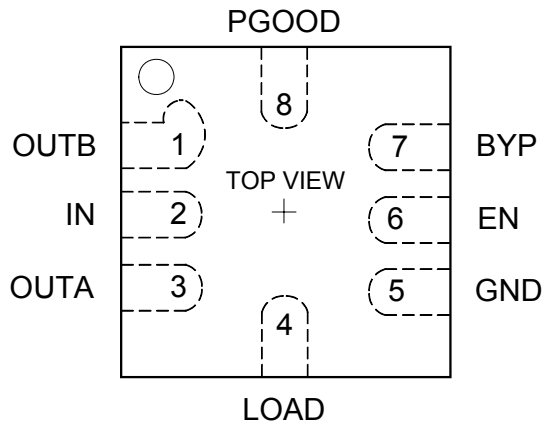
The SC561 provides superior low-noise performance by using an external bypass capacitor to filter the bandgap reference. The device also has a PGOOD output to hold a processor in reset when the voltage on OUTA is not in regulation.

The device provides protection circuitry such as short-circuit protection, under-voltage lockout, and thermal protection to prevent device failures. Stability is maintained by using 1µF capacitors on the output pins. The MLPQ-UT8 package and small ceramic bypass capacitors minimize the required PCB area.

Typical Application Circuit



Pin Configuration



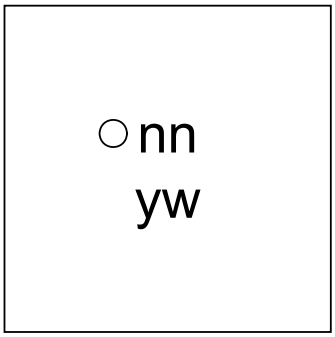
MLPQ-UT-8; 1.5x1.5, 8 LEAD
θ_{JA} = 157°C/W

Ordering Information

Device	Package
SC561ULTRT[1][2]	MLPQ-UT8 1.5×1.5
SC561EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



nn = Part No. Code — See the Voltage Options Table for details
yw = Datecode — See package marking design guidelines document #ALOW-693AQX

Voltage Options

Device	Output Voltage Options		Part Number Code
	V_{LDOA}	V_{LDOB}	
SC561	3.1	2.85	0V

SEMTECH

Absolute Maximum Ratings

IN (V) ..... -0.3 to +6.5
EN, LOAD(V) ..... -0.3 to (V_{IN} + 0.3)
PGOOD (V) ..... -0.3 to (V_{IN} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUTA, OUTB, Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
V_{IN} (V) ..... 2.5 to 5.5

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) ... 157
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted V_{IN} = 3.6V, C_{IN} = 2.2µF, C_{OUTA} = C_{OUTB} = 1µF, V_{EN} = V_{LOAD} = V_{IN}, T_A = -40 to +85°C. Typical values are at T_A = 25°C. All specifications apply to both LDOs unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply Voltage Range	V_{IN}		2.5		5.5	V
Output Voltage	V_{OUTA}			3.1		V
	V_{OUTB}			2.85		
Output Voltage Accuracy	ΔV_{OUTx}	V_{IN} = 2.5V to 5.5V, I_{OUTx} = 0 to 300mA, $V_{IN} \ge V_{OUTx}$ + 0.3	-3		3	%
Maximum Output Current	I_{MAX}	Each LDO	300			mA
Dropout Voltage[1]	V_D	I_{OUTx} = 250mA, V_{OUTx} = 2.5V to 3.3V		150	250	mV
		I_{OUTx} = 50mA, V_{OUTx} = 2.5V to 3.3V		50	100	mV
Shutdown Current	I_{SD}	T_A = 25°C		0.1	1	µA
Quiescent Current	I_Q	I_{OUTA} = I_{OUTB} = 0mA, LOAD = V_{IN}		55	85	µA
		I_{OUTA} = I_{OUTB} = 1mA, LOAD = 0V		40	60	µA
Load Regulation	ΔV_{LOAD}	I_{OUTx} = 1mA to I_{MAX}			20	mV
Line Regulation	ΔV_{LINE}	I_{OUTx} = 1mA	-6		6	mV

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Limit	I_{LIMx}		350		850	mA
Noise	e_N	I_{OUTx} = 50mA , 10Hz < f < 100kHz, C_{BYP} = 22nF		50	100(2)	μV_{RMS}
Power Supply Rejection Ratio	PSRR	I_{OUTx} = 50mA, f = 1kHz, C_{BYP} = 22nF	50(2)	65		dB
PGOOD Delay	t_{DELAY}		160	200	240	ms
PGOOD Threshold	$V_{TH-PGOOD}$	Percentage of nominal output, V_{OUTA} falling	82	87	92	%
PGOOD Threshold Hysteresis	$V_{PGOOD-HYS}$			3		%
Start-Up Time	t_{SU}	From OFF to 87% V_{OUTx}, I_{OUTx} = 50mA, C_{BYP} = 22nF		1		ms
Under Voltage Lockout	V_{UVLO}	V_{IN} Rising	2.20	2.30	2.40	V
UVLO Hysteresis	$V_{UVLO-HYS}$			100		mV
Over Temperature Protection Threshold(3)	T_{OT}	Temperature Rising		160		°C
Over Temperature Threshold Hysteresis	V_{OT-HYS}			20		°C
Digital Inputs						
Logic Input High Threshold	V_{IH}	V_{IN} = 5.5V	1.25			V
Logic Input Low Threshold	V_{IL}	V_{IN} = 2.5V			0.4	V
Logic Input High Current	I_{IH}	V_{IN} = 5.5V			1	µA
Logic Input Low Current	I_{IL}	V_{IN} = 5.5V			1	µA
Digital Outputs						
PGOOD Output voltage Low	V_{OL}	I_{SINK} = 500µA,V_{IN}=3.7V	7		20	mV

Notes:

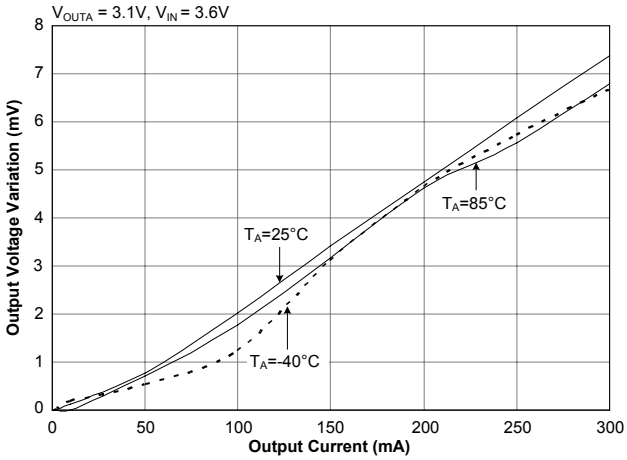
(1) Dropout voltage is defined as V_{IN} - V_{OUTx} , when V_{OUTx} is 100mV below the value of V_{OUTx} at V_{IN} = V_{OUTx} + 0.5V.

(2) Guaranteed by design

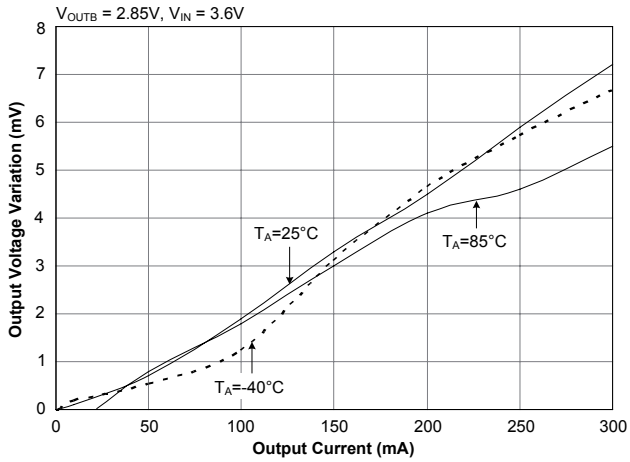
(3) Thermal shutdown latches both LDOs off. Cycle EN or VIN pin to reset.

Typical Characteristics

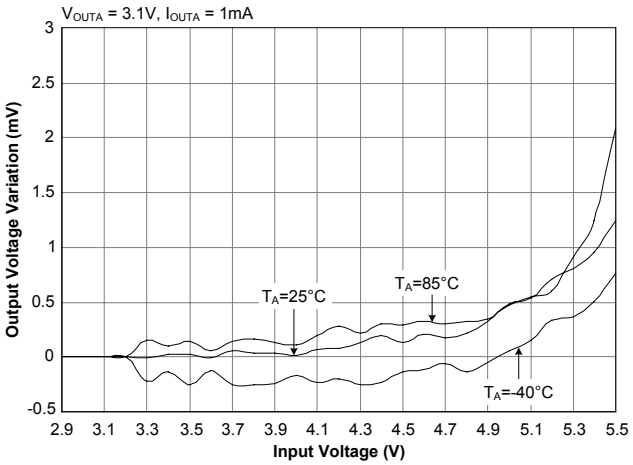
Load Regulation (LDOA)



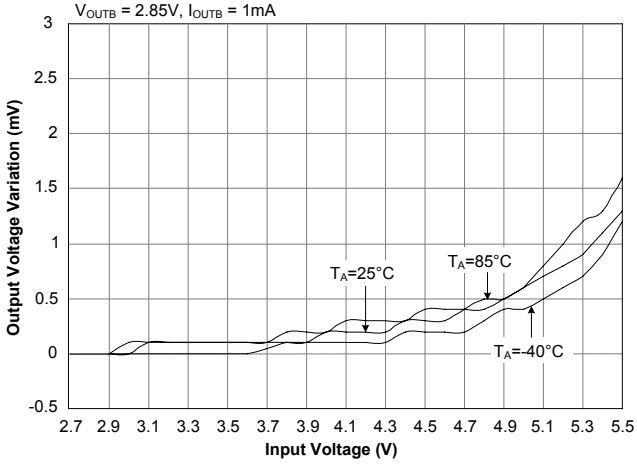
Load Regulation (LDOB)



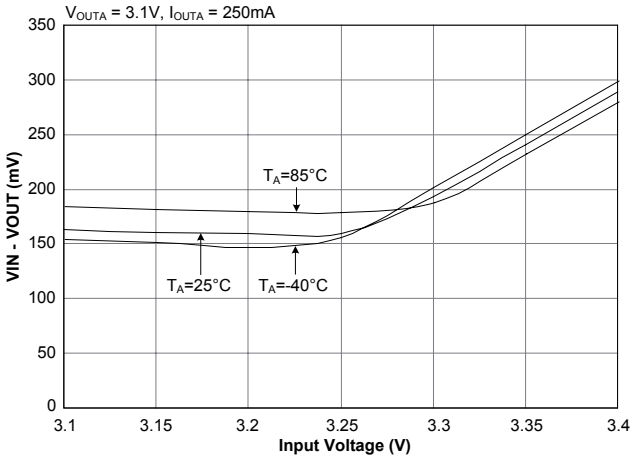
Line Regulation (LDOA)



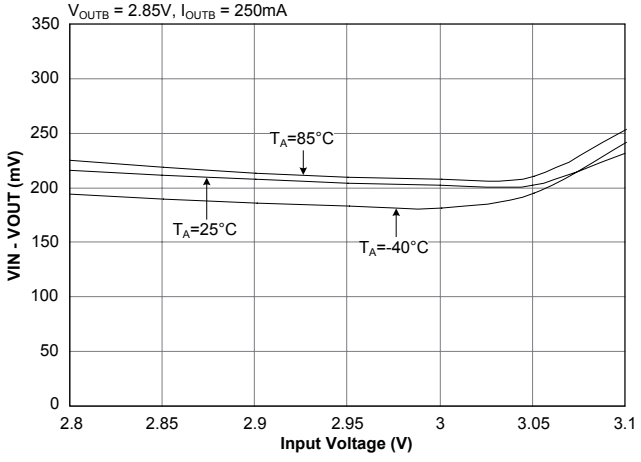
Line Regulation (LDOB)



Dropout Voltage (LDOA)

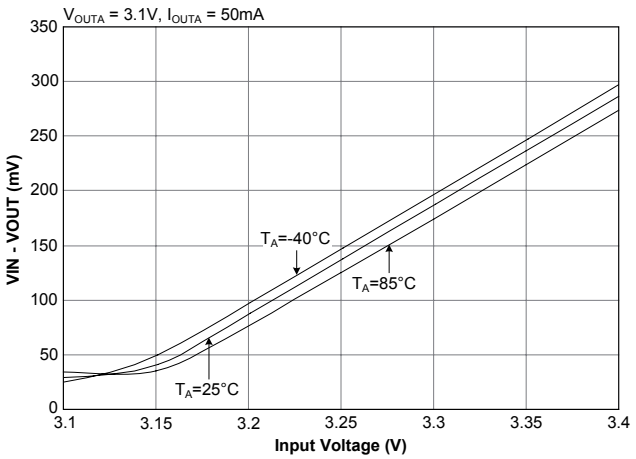


Dropout Voltage (LDOB)

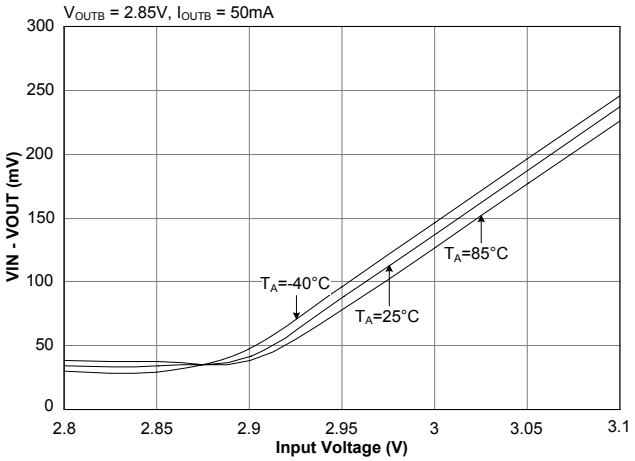


Typical Characteristics (continued)

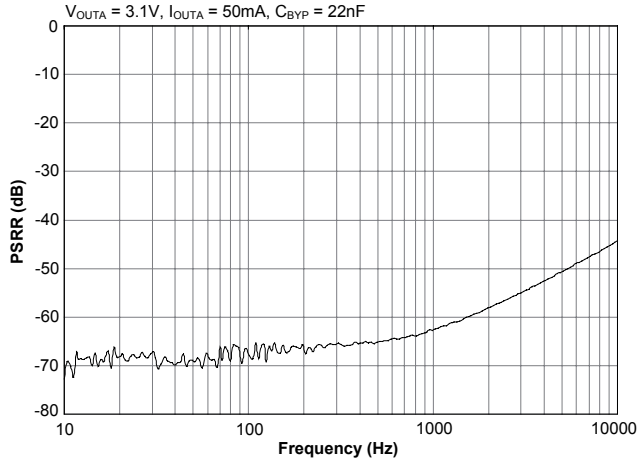
Dropout Voltage (LDOA)



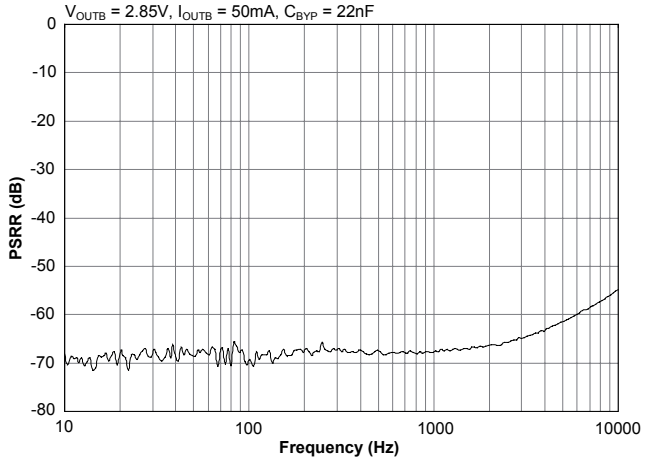
Dropout Voltage (LDOB)



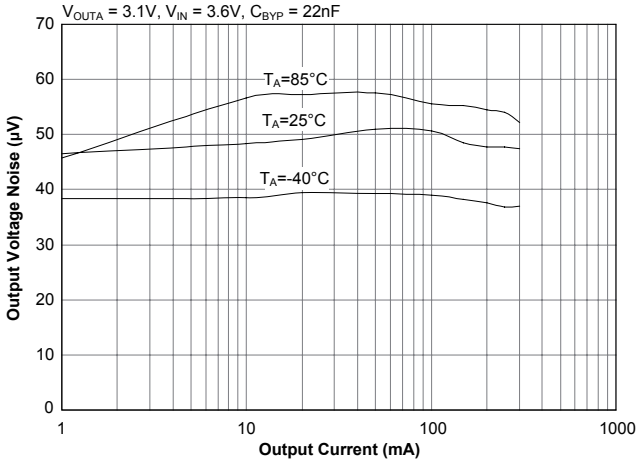
PSRR vs. Frequency (LDOA)



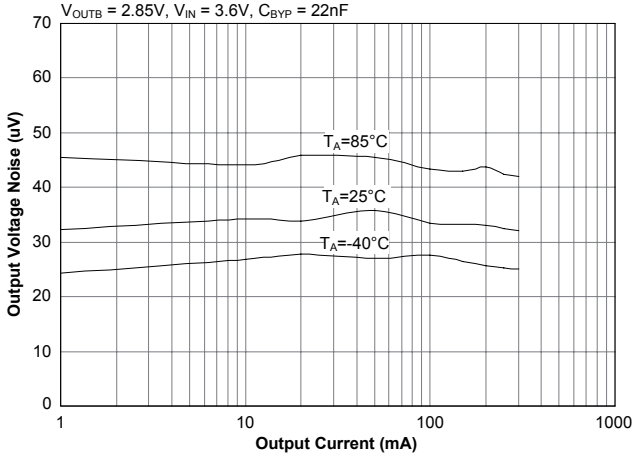
PSRR vs. Frequency (LDOB)



Output Noise vs. Load Current (LDOA)

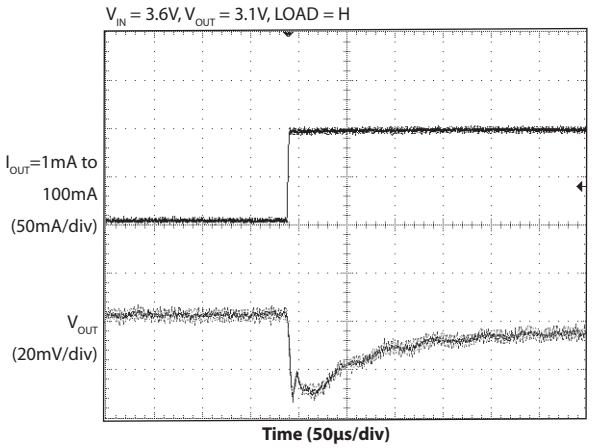


Output Noise vs. Load Current (LDOB)

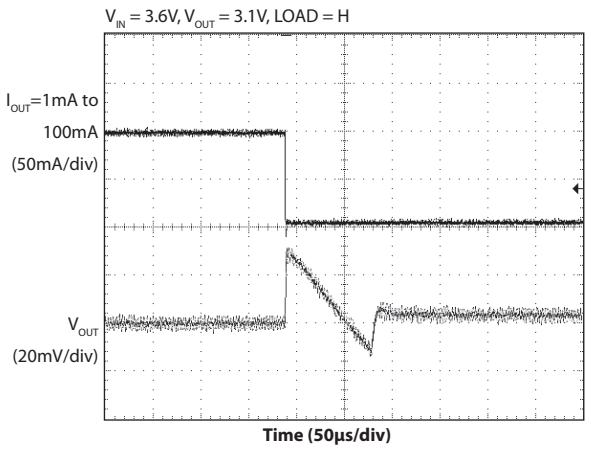


Typical Characteristics (continued)

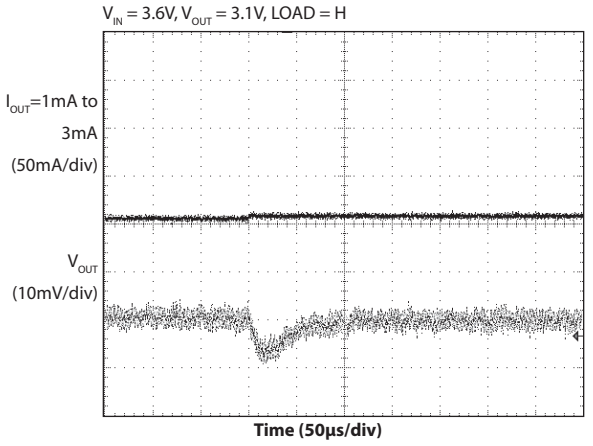
Load Transient Response Rising Edge (Both LDOs)



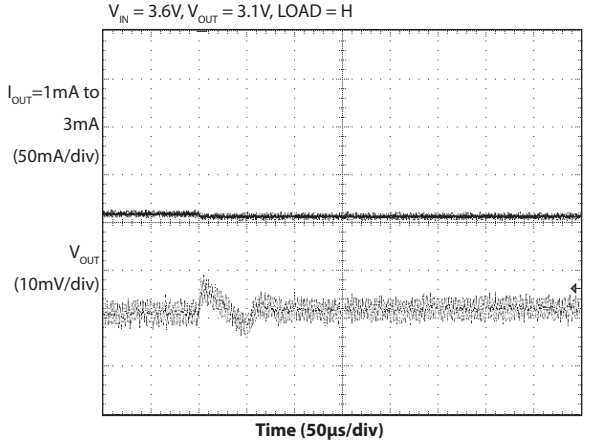
Load Transient Response Falling Edge (Both LDOs)



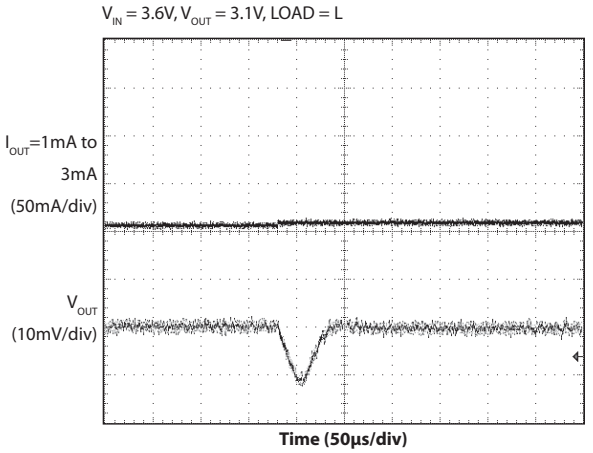
Load Transient Response Rising Edge (Both LDOs)



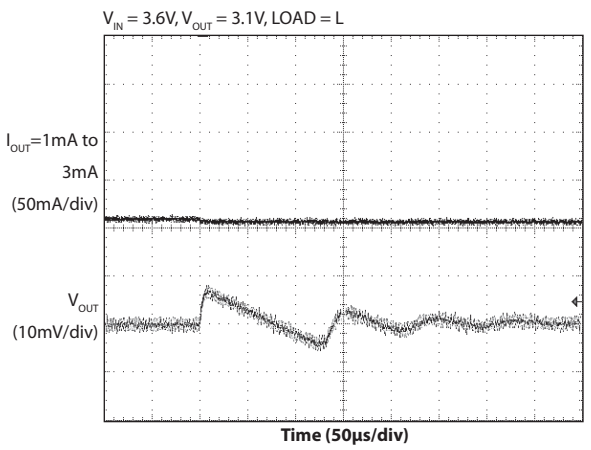
Load Transient Response Falling Edge (Both LDOs)



Load Transient Response Rising Edge (Both LDOs)



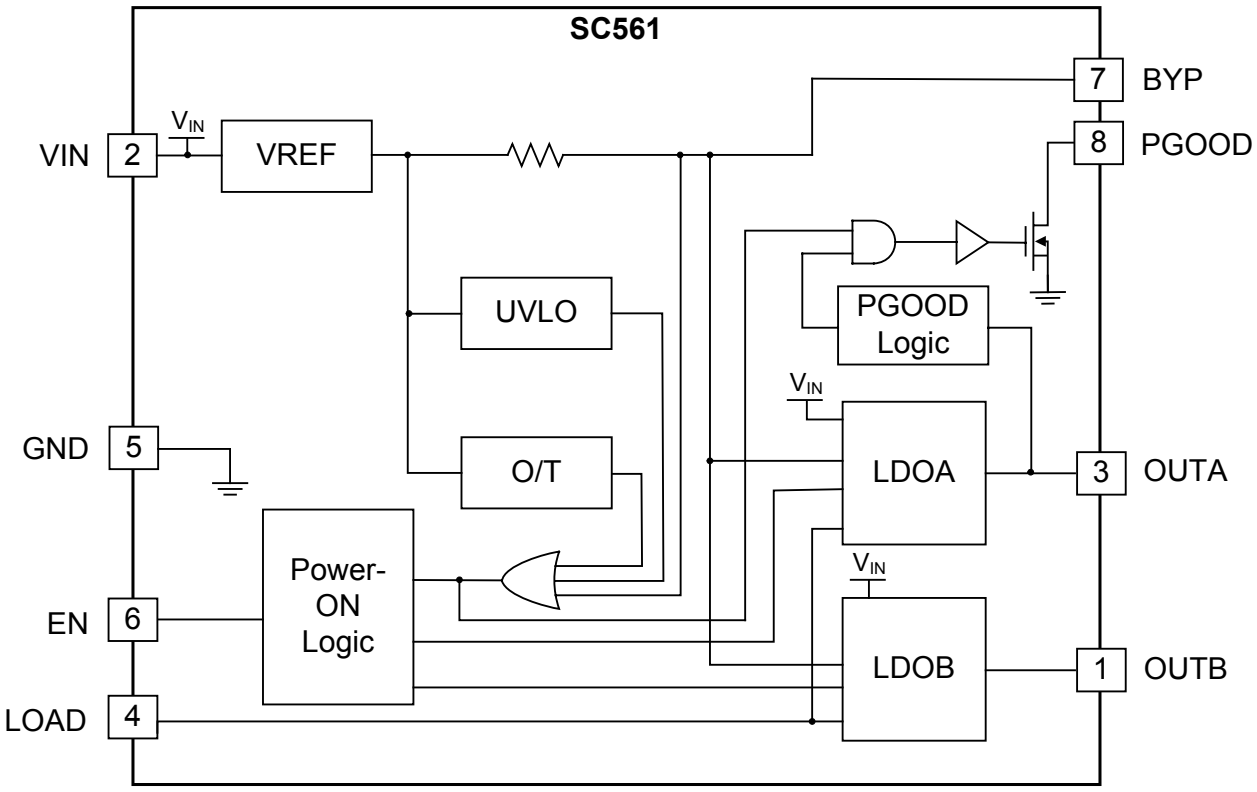
Load Transient Response Falling Edge (Both LDOs)



Pin Configurations and Descriptions

SC561	Pin Name	Pin Function
1	OUTB	Output for LDOB
2	VIN	Input supply voltage terminal
3	OUTA	Output for LDOA
4	LOAD	Dynamic bias control — pull this pin high for normal operation at all load currents. Pull this pin low for lowest I_Q at loads less than 2mA. This pin is a logic input and cannot be left unconnected.
5	GND	Analog and digital ground
6	EN	Logic input — active HIGH enables both LDOs
7	BYP	LDO bypass output — bypass with a 22nF capacitor
8	PGOOD	Power Good open-drain output — monitors the level of LDOA, switches low when the output drops out of regulation. Tie to VIN or OUTA via a 100k Ω resistor. Leave floating when function is not required.

Block Diagram



Applications Information

General Description

The SC561 is a dual output linear regulator device intended for applications where low dropout voltage, low supply current, and low output noise are critical. The device provides a simple, low cost solution for two separate regulated outputs. Minimal PCB area is required due to the miniature package size and the need for only four external capacitors.

The linear regulators LDOA and LDOB are powered from a single input supply rail, and each provides up to 300mA of output current. The SC561 provides output voltages in the range 1.2V to 3.3V. Available voltage values are shown in the Voltage Options table on page 2.

Power On Control

The SC561 device has a single enable pin (EN) that controls both LDO outputs. Pulling this pin low causes the device to enter a low power shutdown mode where it typically draws 100nA from the input supply.

The outputs of both LDOA and LDOB are enabled when EN transitions high. When the output voltage of LDOA reaches 87% of its regulation point, the delay timer starts and the PGOOD signal transitions high after a delay of 200ms. The power up/down sequence is shown in the timing diagram in Figure 1.

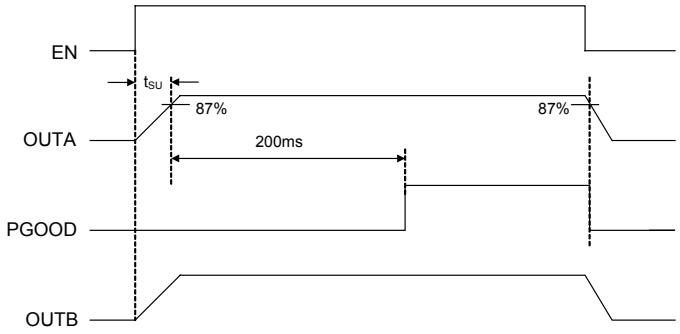


Figure 1 — Timing Diagram

As PGOOD is an open-drain output, it can be left unconnected when it is not in use without affecting the performance of the device.

Dynamic Bias Control

The LOAD pin provides dynamic bias control which allows the device to be operated in a low quiescent current mode at light loads. At loads less than 2mA, the LOAD pin should be pulled low in order to force the device into an ultra-low quiescent current mode. When the load is increased above 2mA, the LOAD pin should be pulled high to ensure normal operation. This pin is a logic input, therefore it must never be left unconnected. Figure 2 shows the quiescent current versus load current with both LDOs enabled.

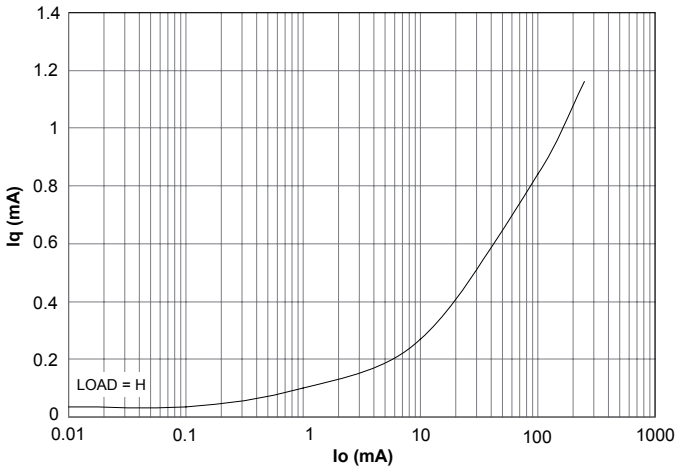


Figure 2a - Quiescent Current versus Output Current

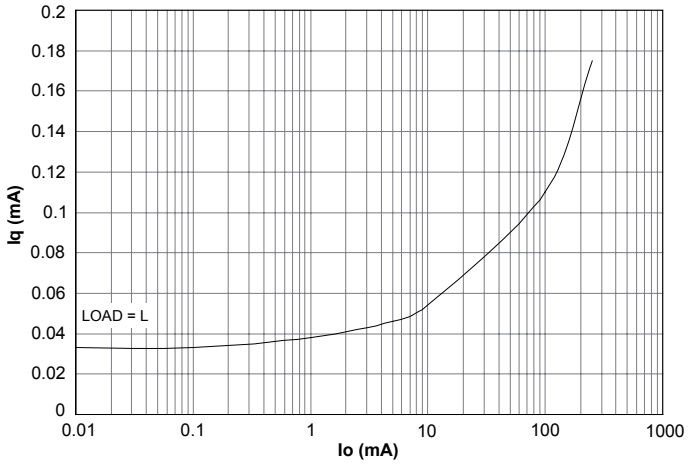


Figure 2b - Quiescent Current versus Output Current

Applications Information (continued)

Protection Features

The SC561 provides protection features to ensure that no damage is incurred in the event of a fault condition. These functions include:

- Under-Voltage Lockout
- Over-Temperature Protection
- Short-Circuit Protection

Under-Voltage Lockout

The Under-Voltage Lockout (UVLO) circuit protects the device from operating in an unknown state if the input voltage supply is too low.

When the V_{IN} drops below the UVLO threshold, as defined in the Electrical Characteristics section, the LDOs are disabled and PGOOD is held low. The LDOs are re-enabled into their previous states when VIN is increased above the hysteresis level. When powering up with V_{IN} below the UVLO threshold, the LDOs remain disabled and PGOOD is held low.

Over-Temperature Protection

An internal Over-Temperature (OT) protection circuit is provided that monitors the internal junction temperature. When the temperature exceeds the OT threshold as defined in the Electrical Characteristics section, the OT protection disables both LDO outputs and holds the PGOOD signal low. The LDOs can only be re-enabled by cycling the EN pin.

Short-Circuit Protection

Each output has short-circuit protection. If the output current exceeds the current limit, the output voltage will drop and the output current will be limited until the load current returns to a specified level.

Component Selection

A minimum capacitance of 1µF on each output is required to ensure stability. This must be considered when choosing very small size capacitors as the dc bias must be included in their derating to ensure this required value. For example, a 1µF 0402 size capacitor may work at low output voltages, but the capacitance may be too low at higher output voltages. Although there is no maximum value of output capacitor specified, very large values may increase the rise time of the output voltages without affecting stability. It is recommended that the value of output capacitance be restricted to a maximum of 10µF. Ceramic capacitors of type X5R or X7R should be used because of their low ESR and stable temperature coefficients. It is also recommended that the input be bypassed with a 2.2µF, low ESR X5R or X7R capacitor to minimize noise and improve transient response. Note: Tantalum and Y5V capacitors are not recommended.

The BYP pin on the SC561 must have a minimum of 22nF connected to ground to meet all noise-sensitive requirements. This value can be increased to a maximum of 1µF to improve noise and PSRR. However, larger values of bypass capacitor will increase the start-up time of the SC561.

Applications Information (continued)

Thermal Considerations

Although each of the two LDOs in the SC561 can provide 300mA of output current, the maximum power dissipation in the device is restricted by the miniature package size. The graphs in Figures 3 and 4 can be used as a guideline to determine whether the input voltage, output voltages, output currents, and ambient temperature of the system result in power dissipation within the operating limits are met or if further thermal relief is required.

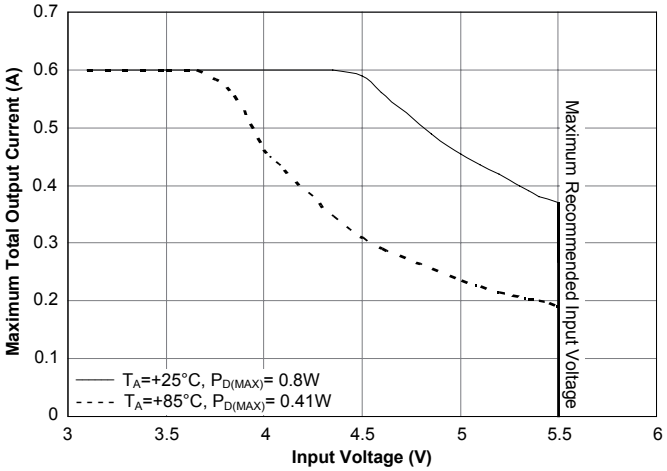


Figure 3 — Safe Operating Limit

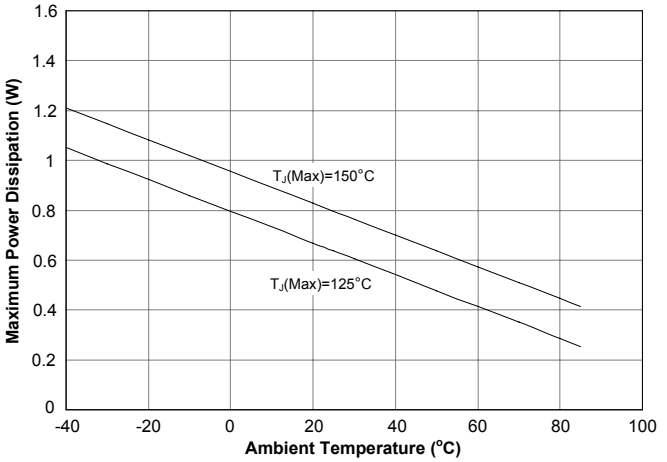


Figure 4 — Maximum P_D vs. T_A

The following procedure can be followed to determine if the thermal design of the system is adequate. The junction temperature of the SC561 can be determined in known operating conditions using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

where

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipation (W)

θ_{JA} = Thermal Resistance Junction to Ambient (°C/W)

Example

A SC561 is used to provide outputs of 3.1V, 150mA from LDOA and 2.85V, 250mA from LDOB. The input voltage is 4.2V, and the ambient temperature of the system is 40°C.

$$P_D = 0.15(4.2 - 3.1) + 0.25(4.2 - 2.85)$$

$$= 0.503W$$

and

$$T_J = 40 + (0.503 \times 157) = 118.9°C$$

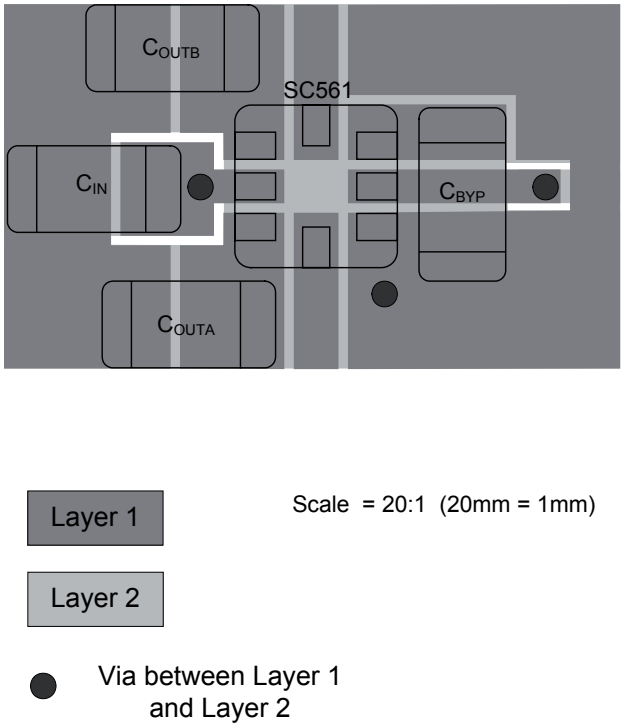
Figure 4 shows that the junction temperature would be within the maximum specification of 150°C for this power dissipation. This means that operation of the SC561 under these conditions is within the specified limits and the device would not require further thermal relief measures.

Applications Information (continued)

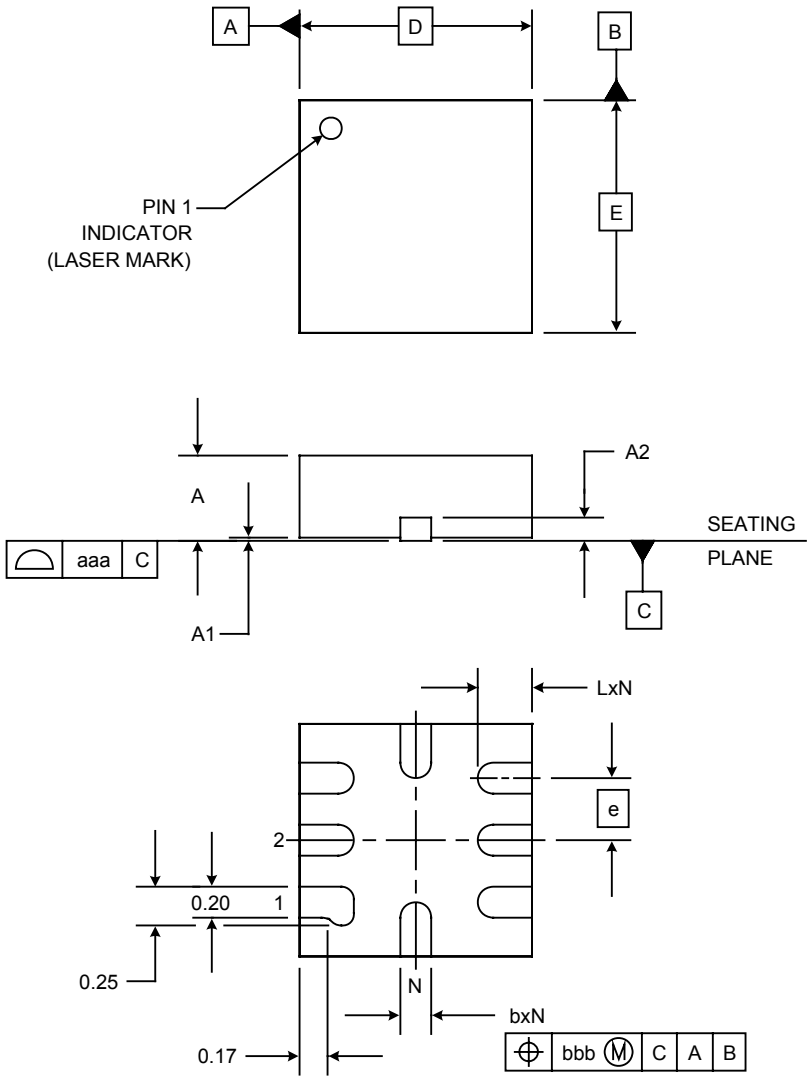
Layout Considerations

While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation. The diagram below illustrates proper layout of a circuit.

- Attach the part to a large copper footprint, to enable better heat transfer from the device on PCBs where there are internal power and ground planes.
- Place the input, output, and bypass capacitors close to the device for optimal transient response and device behavior.
- Connect all ground connections directly to the ground plane whenever possible to minimize ground potential differences on the PCB.



Outline Drawing — MLPQ-UT8

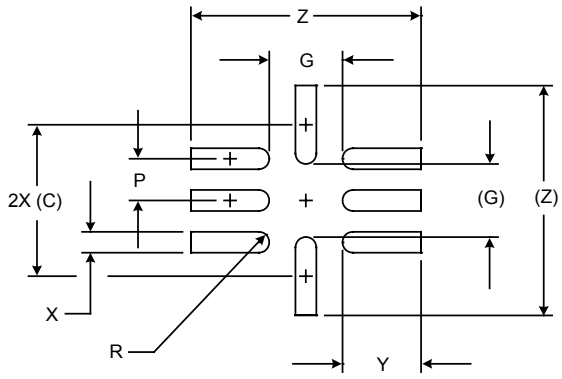


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D		.059 BSC			1.50 BSC	
E		.059 BSC			1.50 BSC	
e		.016 BSC			0.40 BSC	
L	0.12	.014	0.16	0.30	0.35	0.40
N		8			8	
aaa		.004			0.10	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern — MLPQ-UT8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.057)	(1.45)
G	.028	0.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.030	0.75
Z	.087	2.20

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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