DATA SHEET

LinearDimensions
SEMICONDUCTOR

LND3842A/43A/44A/45A
LND3842B/43B/44B/45B

Current Mode PWM Controller

GENERAL DESCRIPTION

The LND3842B/43B/44B/45B and LND3842A /43A/44A/45A are fixed frequency current mode PWM controllers. They are specially designed for OFF-line and DC to DC converter applications with a minimal of external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator. Protection circuitry includes undervoltage lockout and current limiting.

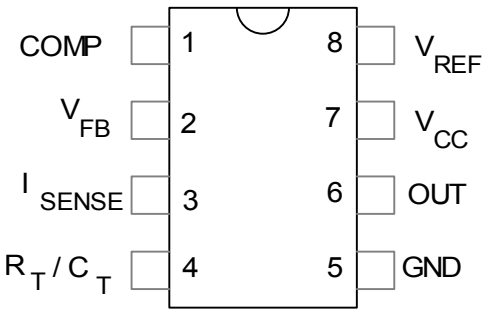
The LND3843B, A and LND3844B, A have UVLO thresholds of 16V(on) and 10 V (off). The corresponding thresholds for the LND3843B, A/ 45B,A are 8.4 V (on) and 7.6(off). The LND3842B, A and LND3843B, A can operate within 100% duty cycle. The LND3844B, A and LND3845B, A can operate within 50% duty cycle.

The LND384XB has Start-Up current of .45mA(typ). The LND384XA has Start-Up current of .17mA(typ).

FEATURES

- Low start-up and operating Current
- High Current Totem Pole Output
- Undervoltage Lockout with Hysterisis
- Operating Frequency up to 500KHZ

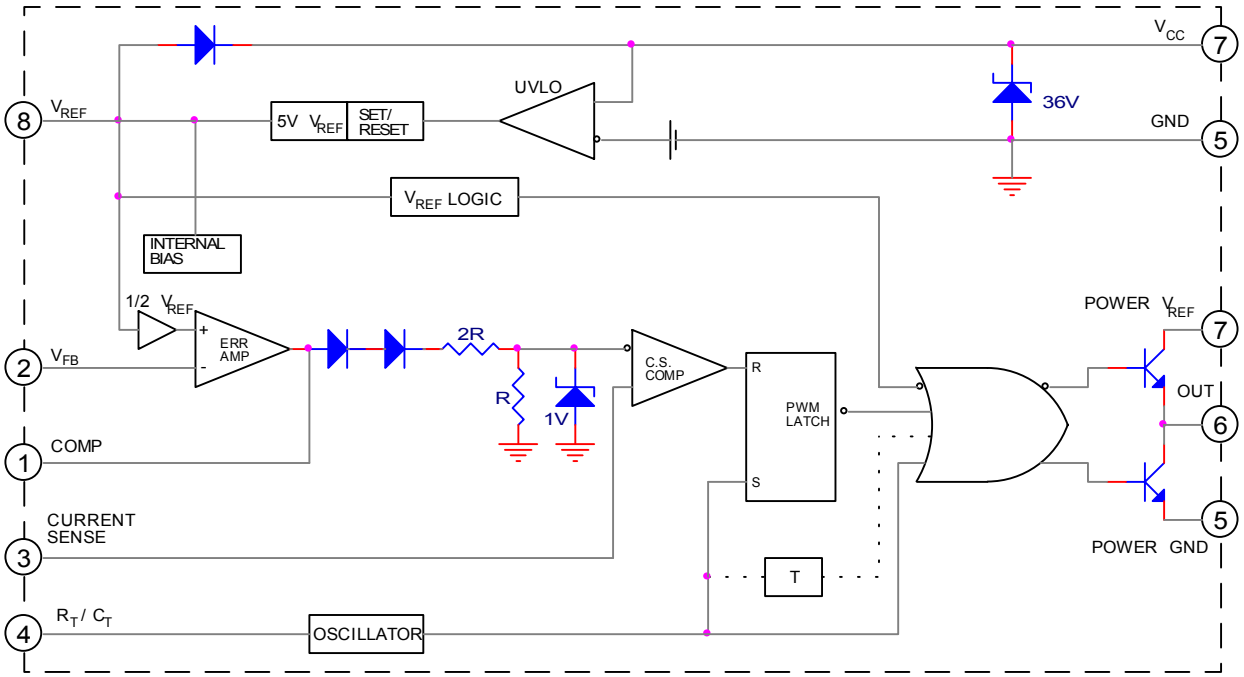
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Units
Supply voltage (low impedance source)	Vcc	30	V
Output Current	I_O	±1	A
Input Voltage (Analog Inputs pins 2,3)	V_I	-0.3 to 5.5	V
Error Amp Output Sink Current	$I_{SINK(E.A)}$	10	mA
Power Dissipation (T_A =25°C)	P_O	1	W
Storage Temperature Range	T_{stg}	-65 to 150	°C
Lead Temperature (soldering 5 sec.)	T_L	260	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(*Vcc =15 V, R_T=10kΩ ,C_T=3.3nF, T_A=0 to 70° C, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Section						
Reference Output Voltage	V_{REF}	T_J =25°C, I_{REF}=1mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	12V≤V_{CC}≤25V		6.0	20	mV
Load Regulation	ΔV_{REF}	1mA≤ I_{REF}≤20mA		6.0	25	
Short Circuit Output Current	I_{SC}	T_A=25°C		100	180	mA
Oscillator Section						
Oscillation Frequency	f	T_J=25°C	47	52	57	KHz
Frequency change with Voltage	$\Delta f/\Delta V_{cc}$	12V≤V_{CC}≤25V		0.05	1.0	%
Oscillator Amplitude	$V_{(OSC)}$	(Peak to Peak)		1.6		V
Error Amplitude Section						
Input Bias Current	I_{BIAS}	V_{FB}=3V		-0.1	-2	µA
Input Voltage	$V_{I(E,A)}$	V_{pin1}=2.5V		2.5	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V≤V_O≤4V	65	90		dB
Power Supply Rejection ratio	PSRR	12V≤V_{CC}≤25V	60	70		
Output Sink Current	I_{SINK}	V_{pin2} =2.7V, Vpin1=1.1V	2	7		mA
Output Source current	I_{SOURCE}	V_{pin2}=2.3V, V_{pin1}=5V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{pin2}=2.3V,R_L=15kΩ to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{pin2}=2.7V,R_L=15kΩ t o PIN 8		0.8	1.1	
Current Sense Section						
Gain	G_V	(Note 1& 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{pin1} =5V(note 1)	0.9	1.0	1.1	V
Supply Voltage rejection	SVR	12V≤V_{cc}≤25V(note 1)		70		dB
Input Bias Current	I_{BIAS}	Vpin3= 3V		-3.0	-10	µA
Output Section						
Low Output Voltage	V_{OL}	I_{sink}=20mA		0.08	0.4	V
		I_{sink}=200mA		1.4	2.2	
High Output Voltage	V_{OH}	I_{sink}=20mA	13	13.5		
		I_{sink}=200mA	12	13.0		
Rise Time	t_R	T_J=25°C, C_L =1nF(note 3)		45	150	nS
Fall time	t_F	T_J=25°C, C_L =1nF(note 3)		35	150	nS
Undervoltage Lockout Section						
Start Threshold	$V_{TH(ST)}$	LND3842A,B/44A,B	14.5	16.0	17.5	V
		LND3842A,B/45A,B	7.8	8.4	9.0	
Min. Operating Voltage (After Turn on)	$V_{OPR(MIN)}$	LND3842A,B/44A,B	8.5	10	11.5	V
		LND3842A,B/45A,B	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	$D_{(MAX)}$	LND3842A,B/43A,B	95	97	100	%
		LND3842A,B/45A,B	47	48	50	
Min. Duty cycle	$D_{(MAX)}$				0	
Total Standby Current						
Start-Up current	I_{ST}	LND3842A/43A/44A/45A		0.17	0.3	mA
		LND3842B/43B/44B/45B		0.45	1	
Operating Supply Current	$I_{CC(OPR)}$	V_{PIN3}=V_{PIN2} =0V		13	17	mA
Zener Voltage	V_Z	I_{CC}=25mA	30	38		V

*Adjust V_{CC} above the start threshold before setting it to 15V.

Note 1: Parameter measured at trip point of latch with $V_{pin2=0}$
Note 2: Gain defined as $A=\Delta V_{pin1}/=\Delta V_{pin3}$: $0\leq V_{pin3}\leq 0.8V$.
Note 3: These parameters, although guaranteed, are not 100% tested in production.

PIN DESCRIPTION

No	FUNCTION	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made for loop compensation
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
5	GROUND	This pin is the combined control circuitry and power ground
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sinked by this pin.
7	V_{CC}	This pin is the positive supply of the integrated circuit.
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

TYPICAL APPLICATIONS

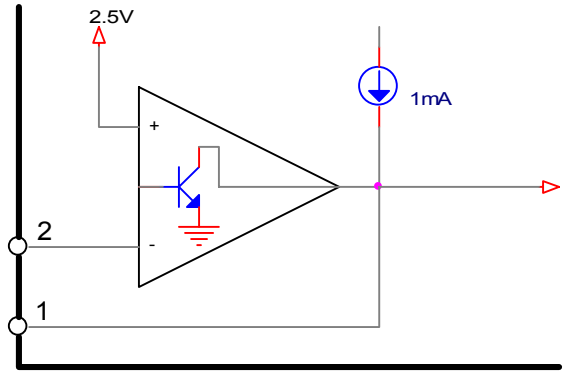
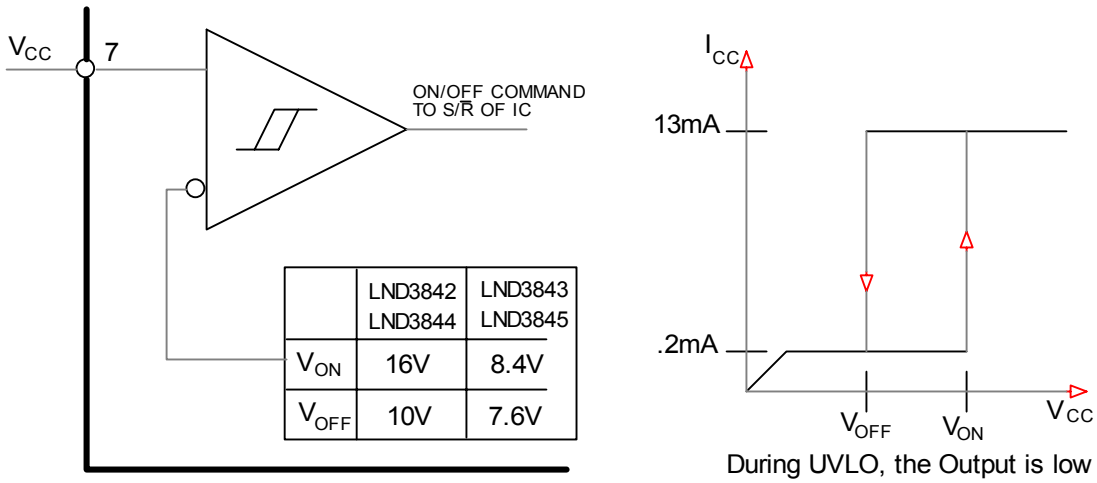
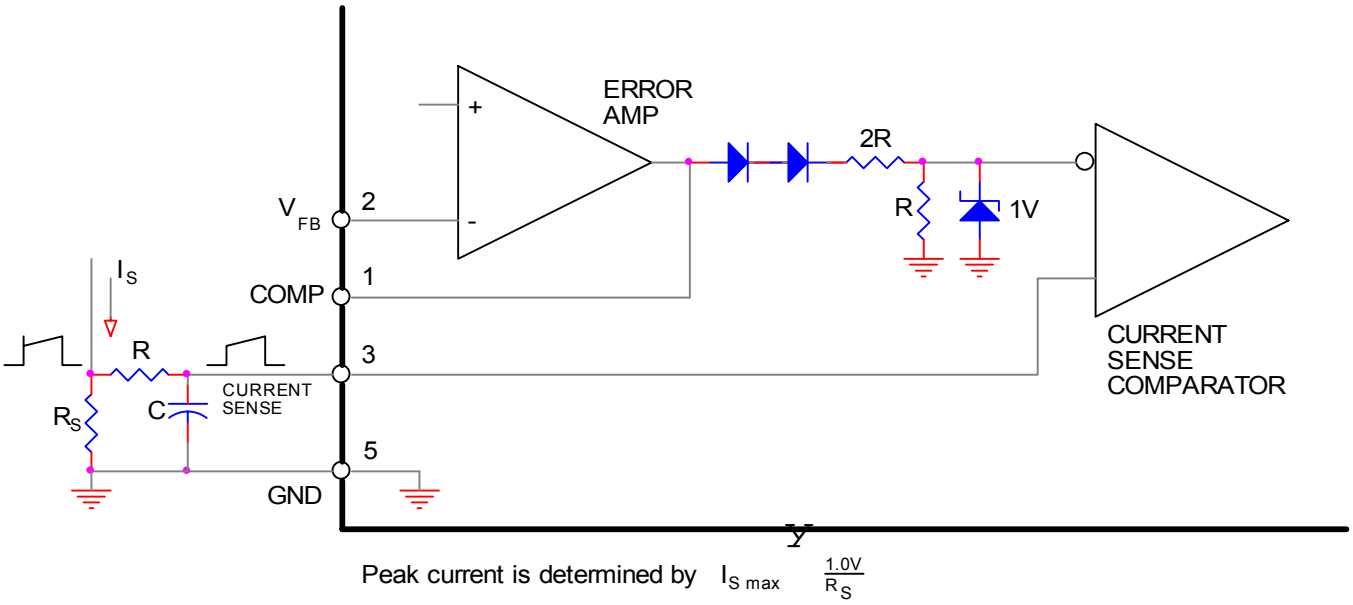


Figure 1. Error Amp Configuration



	LND3842 LND3844	LND3843 LND3845
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

Figure 2. Undervoltage Lockout



Peak current is determined by $I_{S\,max}$ $\frac{1.0V}{R_S}$

Figure 3. Current Sense Circuit

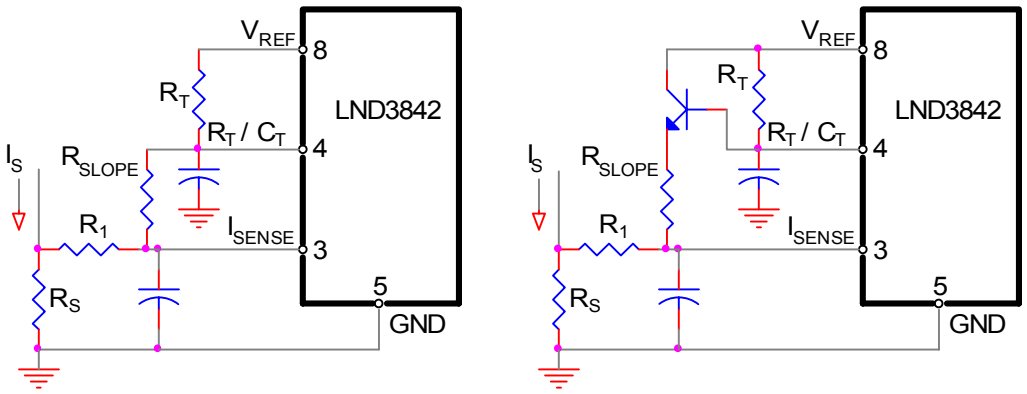
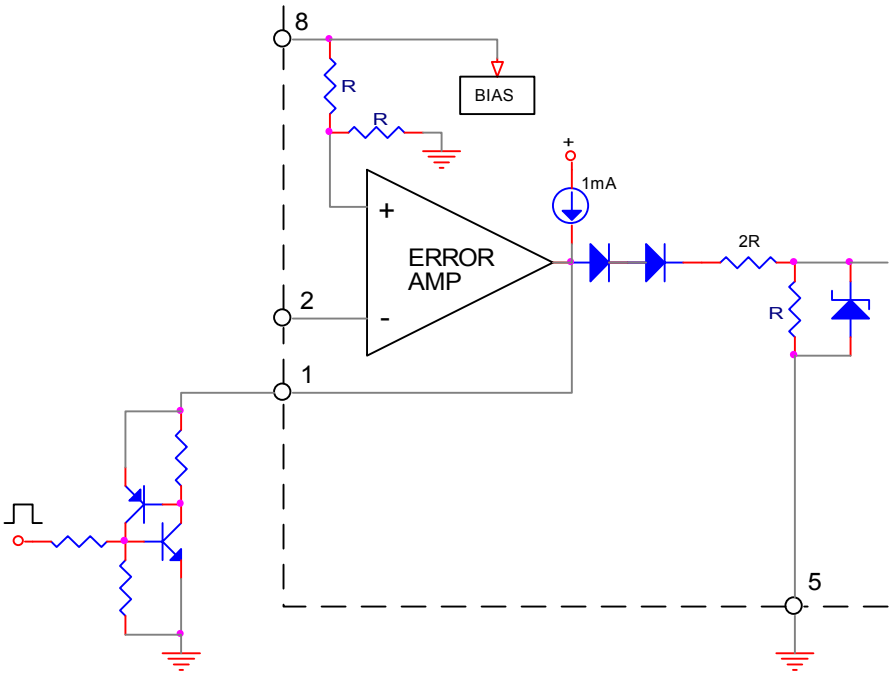
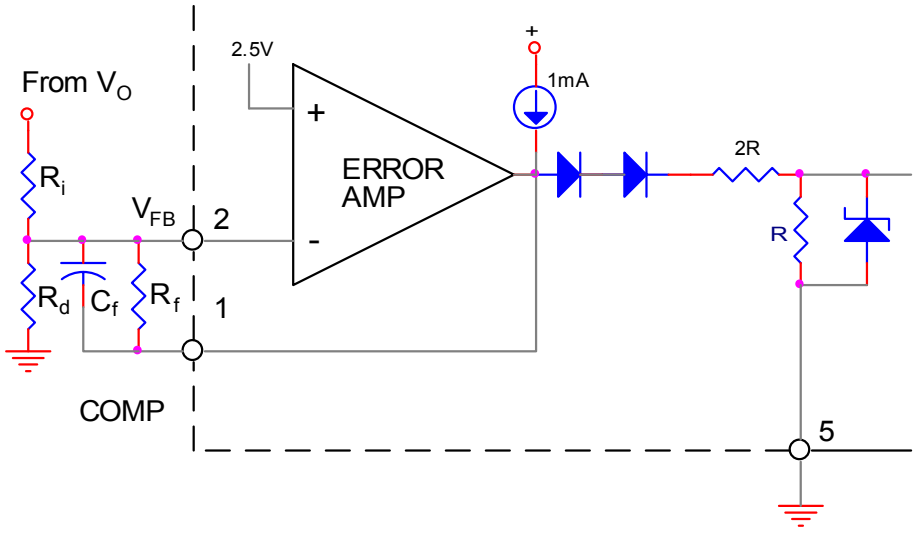


Figure 4. Slope Compensation Techniques

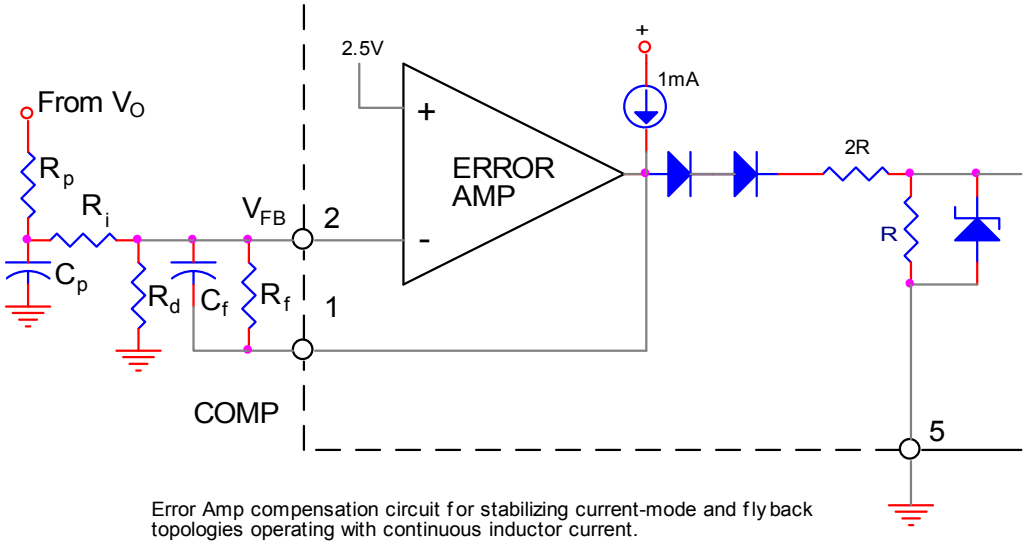


SCR must be selected for a holding current of less than 0.5 mA. A simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

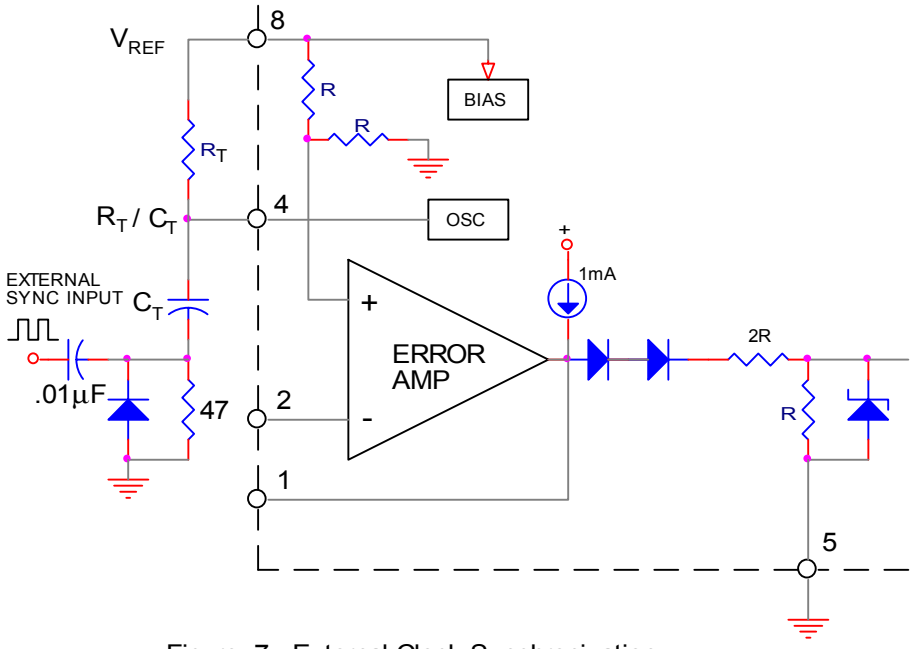


Figure 7. External Clock Synchronization

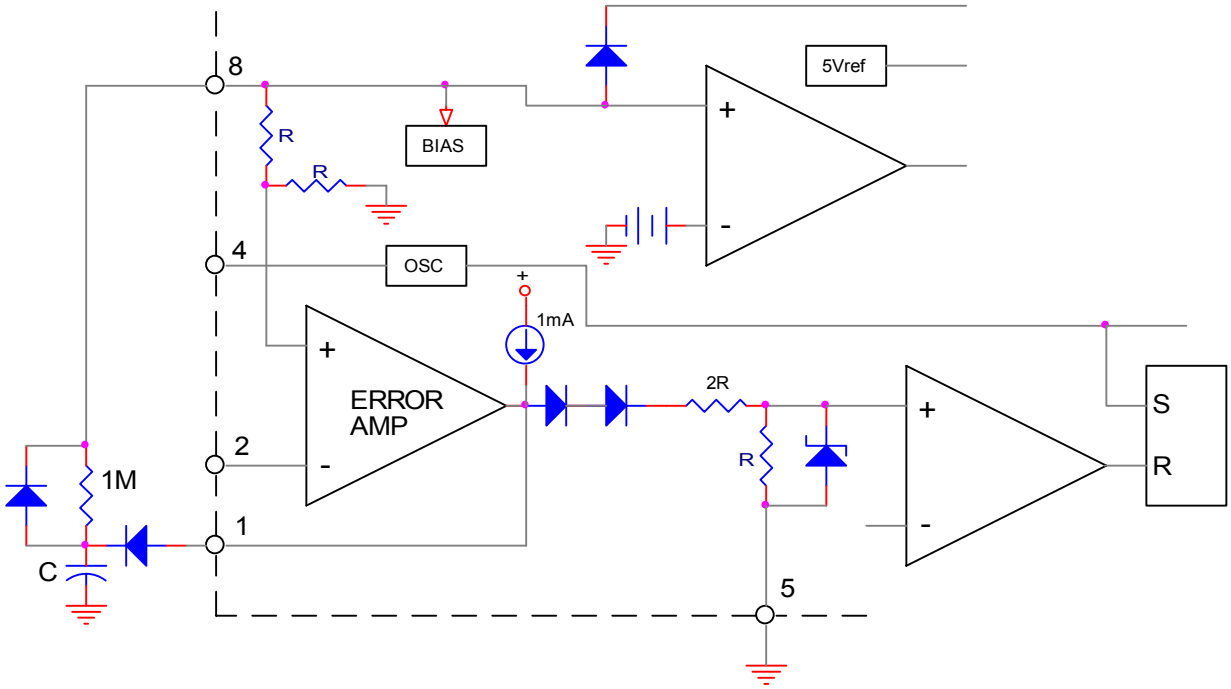


Figure 8. Soft-Start Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

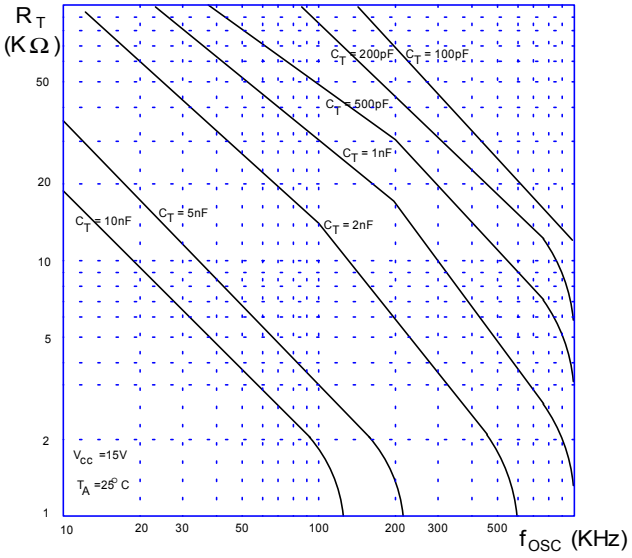


Figure 1. Timing Resistor vs. Oscillator Frequency

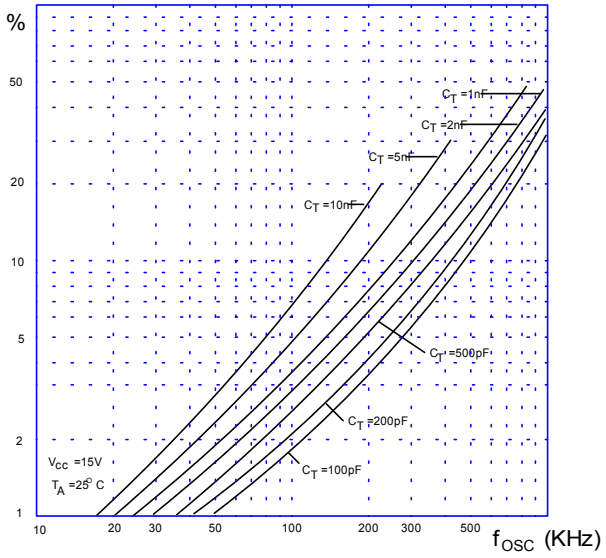


Figure 2. Output Dead-Time vs. Oscillator Frequency

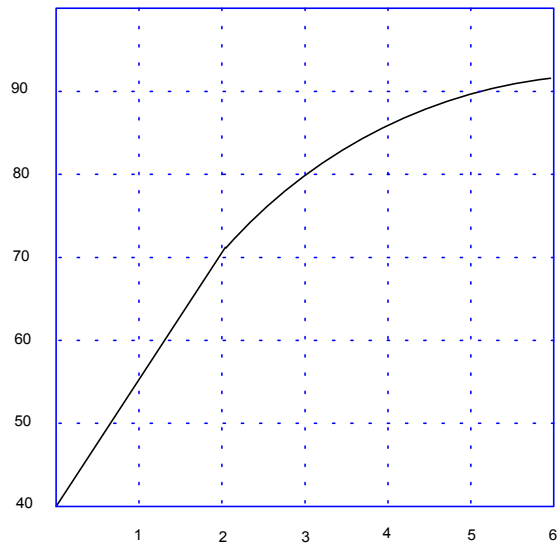


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor

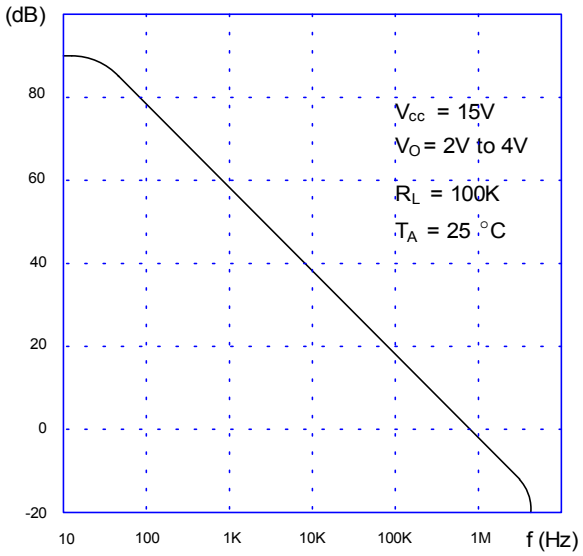


Figure 4. Error Amp Open-Loop Gain vs. Frequency

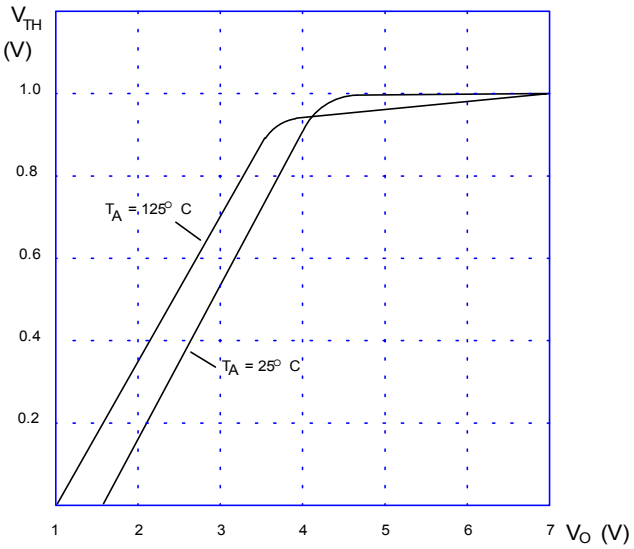


Figure 5. Current Sense Input Threshold vs. Output

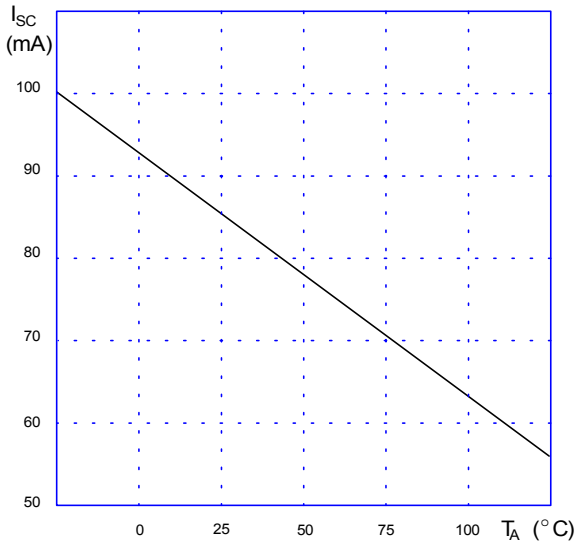


Figure 6. Reference Short Circuit Current vs. Temperature

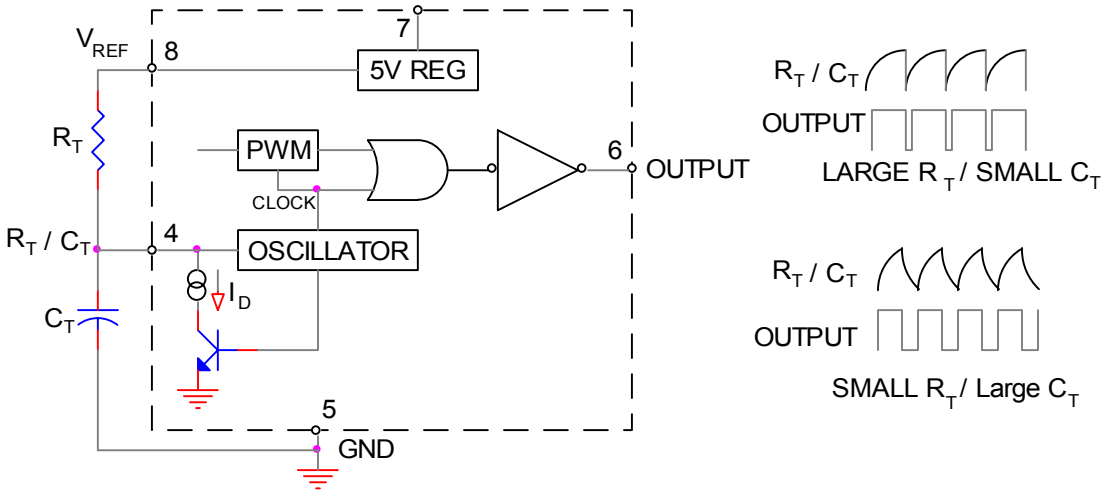


Figure 7. Oscillator and Output Waveforms