TMUX1072 2-Channel 2:1 Analog Multiplexer with Overvoltage Detection and Protection

1 Features

- Supply Range 2.3 V to 5.5 V
- Powered Off Protection: I/O pins Hi-Z When V_{CC} = 0 V
- Overvoltage and Overtemperature detection
- 0-V to 20-V Overvoltage Protection (OVP) on Common Pins
- Low R_{ON} of 6 Ω
- BW of 1.2 GHz Typical
- C_{ON} of 4.5 pF Typical
- Low Power Disable Mode
- 1.8-V Compatible Logic Inputs
- ESD Protection Exceeds JESD22
  - 2000-V Human Body Model (HBM)
- Small 2.00mm x 1.70mm QFN Package available

2 Applications

- Data Aquisition (DAQ)
- Field Instrumentation
- Video Surveillance
- HVAC Systems
- Rear Camera

3 Description

The TMUX1072 is a high-speed, 2-channel, 2:1, analog switch with integrated overvoltage detection and powered off protection. The device is bidirectional and can be used as a 2:1 or 1:2 switch.

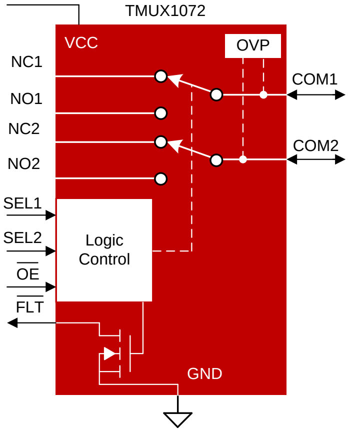
The protection on the I/O pins of the TMUX1072 can tolerate up to 20 V with automatic shutoff circuitry to protect system components behind the switch. This protection is also used for power sequencing where some boards in the system maybe powered up before others are ready to receive signals. The device also detects overvoltage and overtemperature events and provides an open drain output signal through the FLT pin.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX1072	UQFN (12)	2.00 mm × 1.70 mm
	VSSOP (10)	3.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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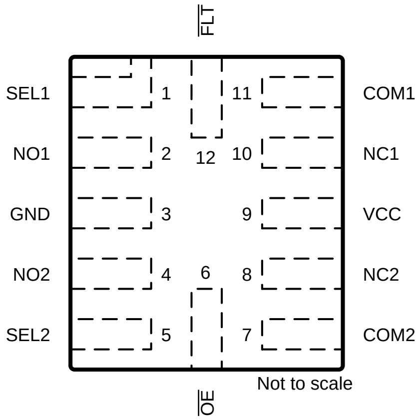
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2018	*	initial release

5 Pin Configuration and Functions

RUT Package
12-Pin UQFN
Top View



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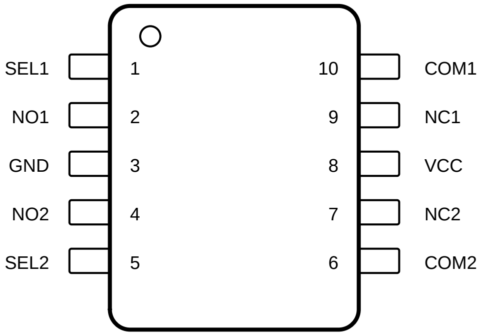
DGS Package
10-Pin VSSOP
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	RUT	DGS		
SEL1	1	1	I	Switch select 1
NO1	2	2	I/O	Signal path NO1
GND	3	3	GND	Ground
NO2	4	4	I/O	Signal path NO2
SEL2	5	5	I	Switch select 2
$\overline{\text{OE}}$	6	-	I	Output enable (Active low)
COM2	7	6	I/O	Common signal path 2
NC2	8	7	I/O	Signal path NC2
VCC	9	8	PWR	Supply Voltage
NC1	10	9	I/O	Signal path NC1
COM1	11	10	I/O	Common signal path 1
$\overline{\text{FLT}}$	12	-	O	Fault indicator output pin (Active low) - open drain

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	6	V
$V_{I/O}$	Input/Output DC voltage (COM1, COM2)(3)		–0.5	20	V
	Input/Output DC voltage (NC1, NO1, NC2, NO2) (3)		–0.5	6	V
V_I	Digital input voltage (SEL1, SEL2, $\overline{OE}$)		–0.5	6	V
V_O	Digital output voltage ($\overline{FLT}$)		–0.5	6	V
I_K	Input-output port diode current (COM1, COM2,NC1, NO1, NC2, NO2)	$V_{IN} < 0$	–50		mA
I_{IK}	Digital logic input clamp current (SEL1, SEL2, $\overline{OE}$) (3)	$V_I < 0$	–50		mA
I_{CC}	Continuous current through VCC			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Operating Junction Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
$V_{I/O}$	Analog input/output	COM1, COM2	0	18	V
$V_{I/O}$		(NC1, NO1, NC2, NO2)	0	5.5	V
$I_{I/O}$		COM1, COM2	-50	50	mA
$I_{I/O}$		(NC1, NO1, NC2, NO2)	-50	50	mA
V_I	Digital input voltage	SEL1, SEL2, $\overline{OE}$	0	5.5	V
V_O	Digital output voltage	$\overline{FLT}$	0	5.5	V
$I_{I/O}$	Analog input/output port continuous current	(COM1, COM2, NC1, NO1, NC2, NO2)	-50	50	mA
I_{OL}	Digital output current			3	mA
T_A	Operating free-air temperature		–40	85	ºC
T_J	Junction temperature		–40	125	ºC

6.4 Thermal Information

THERMAL METRIC (1)		TMUX1072		UNIT
		RUT (UQFN)	DGS (VSSOP)	
		12 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127	175	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.5	61.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.7	96.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	8.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.3	95.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to +85°C , V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC}	Power supply voltage		2.3		5.5	V
I_{CC}	Active supply current	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} 0 V < $V_{I/O}$ < 3.6 V		75	100	µA
	Supply current during OVP condition	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} $V_{I/O} > V_{POS\_THLD}$		65	100	µA
I_{CC_PD}	Standby powered down supply current	$\overline{OE}$ = 1.8 V or V_{CC} SEL1 = 0 V, 1.8 V, or VCC SEL2 = 0 V, 1.8 V, or VCC		3	10	µA
DC Characteristics						
R_{ON}	ON-state resistance	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		6	15	Ω
ΔR_{ON}	ON-state resistance match between channels	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		0.07	0.3	Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	$V_{I/O}$ = 0 V to V_{CC} I_{SINK} = 8 mA Refer to ON-State Resistance Figure		2.5	6	Ω
I_{OFF}	I/O pin OFF leakage current	$V_{COM1/2}$ = 0 V or 3.6 V V_{CC} = 2.3 V to 5.5 V $V_{NC1/2}$ or $V_{NO1/2}$ = 3.6 V or 0 V Refer to Off Leakage Figure		3.6		µA
		$V_{COM1/2}$ = 0 V or 20 V V_{CC} = 2.3 V to 5.5 V $V_{NC1/2}$ or $V_{NO1/2}$ = 0 V Refer to Off Leakage Figure		165		µA
I_{ON}	ON leakage current	$V_{COM1/2}$ = 0 V or 3.6 V $V_{NC1/2}$ and $V_{NO1/2}$ = high-Z Refer to On Leakage Figure		1.2		µA
Digital Characteristics						
V_{IH}	Input logic high	SEL1, SEL2, $\overline{OE}$	1.4			V
V_{IL}	Input logic low	SEL1, SEL2, $\overline{OE}$			0.5	V
V_{OL}	Output logic low	$\overline{FLT}$ I_{OL} = 3 mA			0.4	V
I_{IH}	Input high leakage current	SEL1, SEL2, $\overline{OE}$ = 1.8 V, V_{CC}	-1	2	5	µA
I_{IL}	Input low leakage current	SEL1, SEL2, $\overline{OE}$ = 0 V	-1	±0.2	5	µA

Electrical Characteristics (continued)

T_A = –40°C to +85°C , V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Internal pull-down resistor on digital input pins	SEL1, SEL2		6		MΩ
		$\overline{OE}$		3		MΩ
C_I	Digital input capacitance	SEL1, SEL2 = 0 V, 1.8 V or VCC f = 1 MHz		TBD		pF
Protection and Detection						
V_{OVP_TH}	OVP positive threshold		5.55	5.8	6.0	V
V_{OVP_HYST}	OVP threshold hysteresis		40	100	300	mV
T_{OTD_TH}	Overtemperature detection threshold		135		165	°C
V_{CLAMP_V}	Maximum voltage to appear on NC1/2 and NO1/2 pins during OVP scenario	$V_{COM1/2}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = Open Switch on or off $\overline{OE}$ = 0 V	0		9.6	V
		$V_{COM1/2}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = 50Ω Switch on or off $\overline{OE}$ = 0 V	0		9.0	V
t_{EN_OVP}	OVP enable time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		0.6	3	µs
t_{REC_OVP}	OVP recovery time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		1.5	5	µs

6.6 Dynamic Characteristics

T_A = –40°C to +85°C , V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

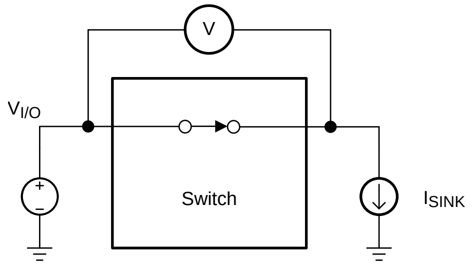
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	COM1, COM2 off capacitance	$V_{COM1/2}$ = 0 or 3.3 V, $\overline{OE}$ = V_{CC} f = TBD MHz	Switch OFF	1.2	TBD	6.2	pF
	NC1, NO1, NC2, NO2 off capacitance	$V_{COM1/2}$ = 0 or 3.3 V, $\overline{OE}$ = V_{CC} or $\overline{OE}$ = 0V with SEL1, SEL2 (switch not selected) f = TBD MHz	Switch OFF or not selected	1.2	TBD	6.2	pF
C_{ON}	IO pins ON capacitance	$V_{COM1/2}$ = 0 or 3.3 V, f = TBD MHz	Switch ON	1.4	TBD	6.2	pF
O_{ISO}	Differential off isolation	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Off Isolation Figure	Switch OFF		TBD		dB
		RL = 50 Ω CL = 5 pF f = TBD MHz Refer to Off Isolation Figure	Switch OFF		TBD		dB
X_{TALK}	Channel to Channel crosstalk	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Crosstalk Figure	Switch ON		TBD		dB
BW	Bandwidth	RL = 50 Ω; Refer to BW and Insertion Loss Figure	Switch ON		1.2		GHz
I_{LOSS}	Insertion loss	RL = 50 Ω f = TBD MHz; Refer to BW and Insertion Loss Figure	Switch ON		TBD		dB

6.7 Timing Requirements

T_A = –40°C to +85°C , V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{switch}	Switching time between channels (SEL1, SEL2 to output)	$V_{COM1/2}$ = V_{CC} Refer to Tswitch Timing Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		0.9	TBD	µs
t_{on}	Device turn on time ($\overline{OE}$ to output)	$V_{COM1/2}$ = V_{CC} Refer to Ton and Toff Figure			200	TBD	µs
t_{off}	Device turn off time ($\overline{OE}$ to output)	$V_{COM1/2}$ = V_{CC} Refer to Ton and Toff Figure			1	TBD	µs
$t_{SK(P)}$	Skew of opposite transitions of same output (between COM1 and COM2)	$V_{COM1/2}$ = V_{CC} Refer to Tsk Figure	R_L = 50 Ω, C_L = 1 pF, V_{CC} = 2.3 V to 5.5 V		9	TBD	ps
t_{pd}	Propagation delay	$V_{COM1/2}$ = V_{CC} Refer to Tpd Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		200	TBD	ps

7 Parameter Measurement Information



Channel ON, $R_{ON} = V/I_{SINK}$

Figure 1. ON-State Resistance (R_{ON})

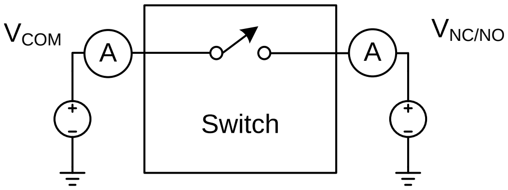


Figure 2. Off Leakage

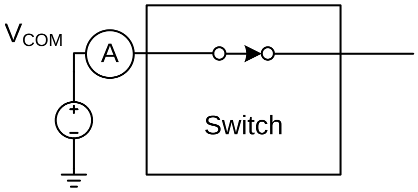
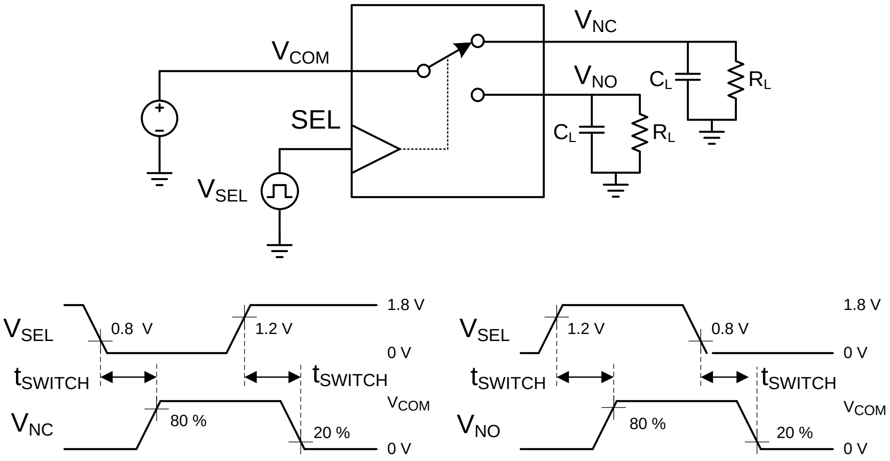


Figure 3. On Leakage

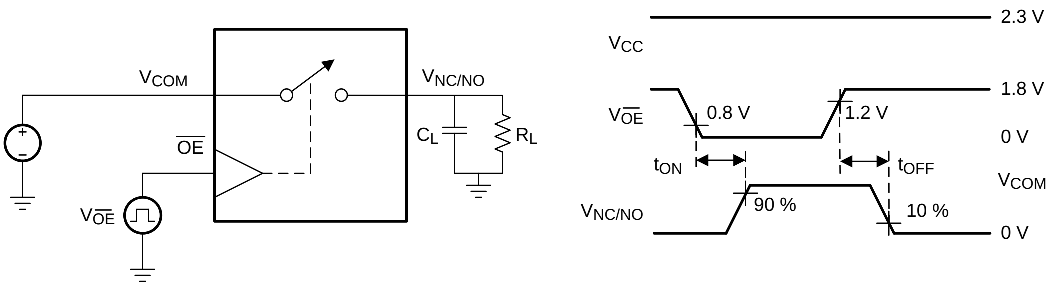


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r < 500$ ps, $t_f < 500$ ps.

(2) C_L includes probe and jig capacitance.

Figure 4. t_{SWITCH} Timing

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

Figure 5. t_{ON}, t_{OFF} for $\overline{OE}$

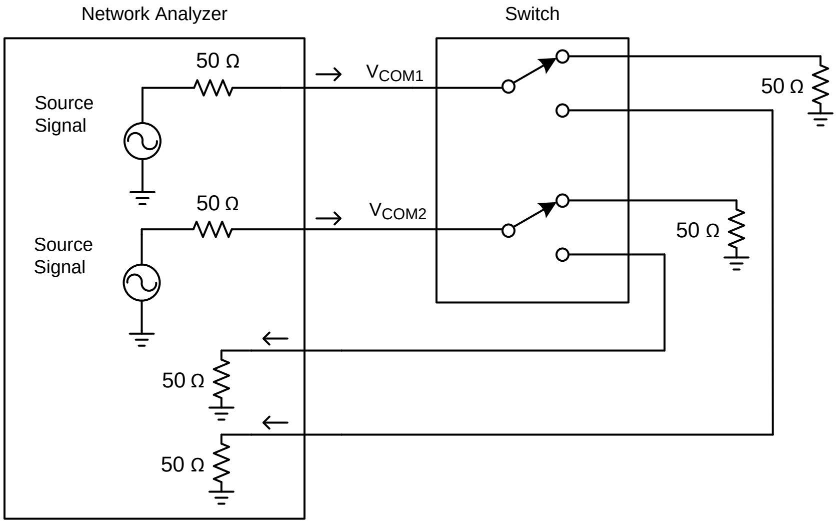


Figure 6. Off Isolation

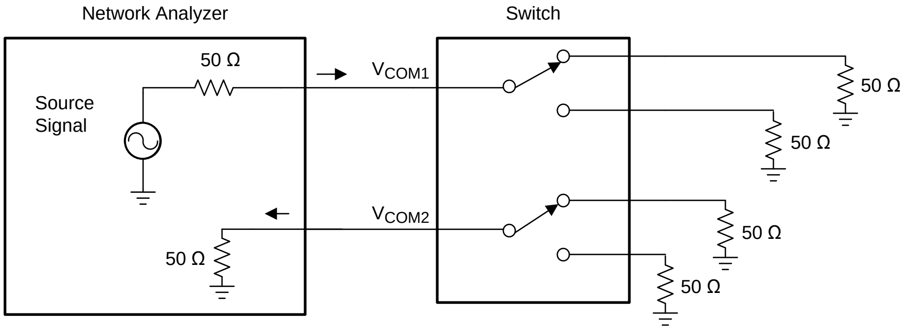


Figure 7. Cross Talk

Parameter Measurement Information (continued)

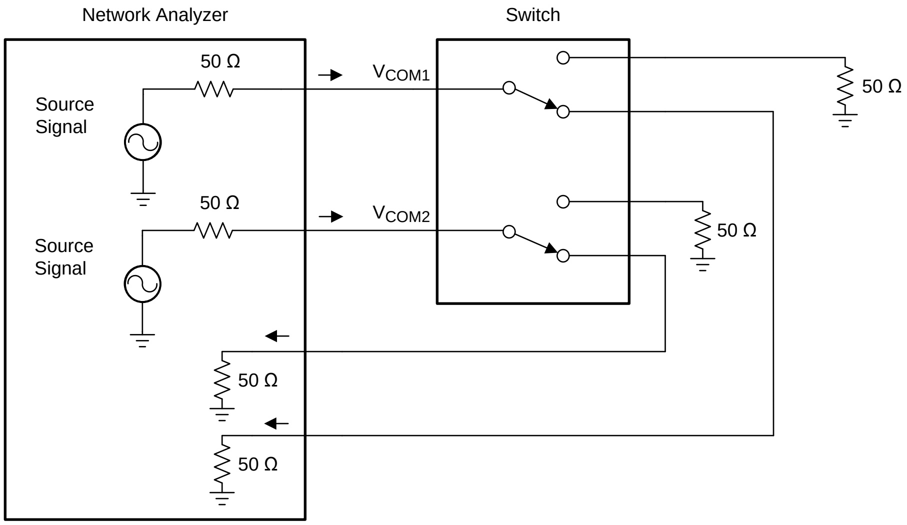


Figure 8. BW and Insertion Loss

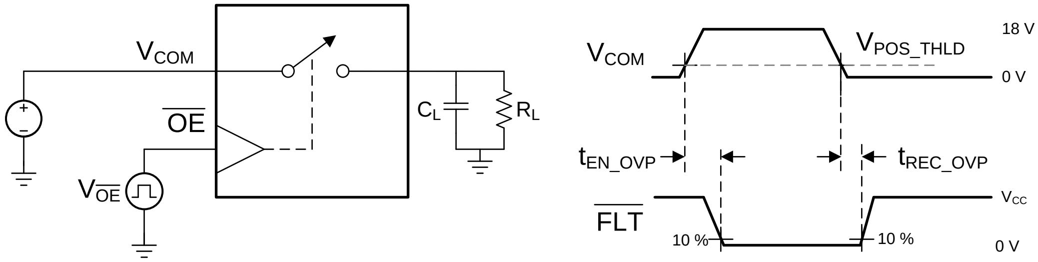
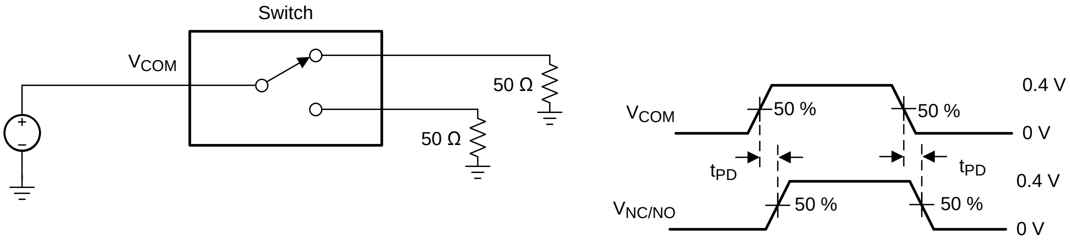


Figure 9. t_{EN_OVP} and t_{DIS_OVP} Timing Diagram

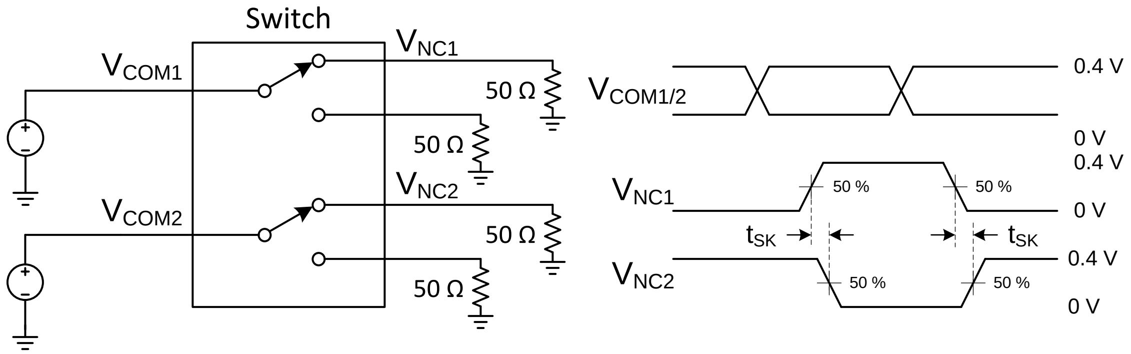


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

Figure 10. t_{PD}

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

Figure 11. t_{SK}

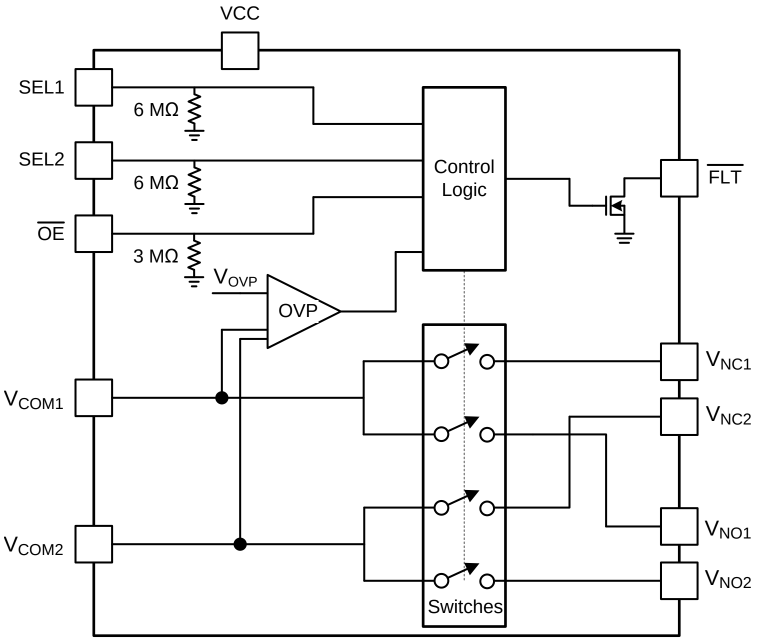
8 Detailed Description

8.1 Overview

The TMUX1072 is a highspeed, 2-channel 2:1 analog switch with overvoltage protection. The device is bidirectional and can be used as a dual 2:1 or 1:2 switch but OVP only applies to the COM pins. The device also contains a fault detection pin which can signal to the system of either an overvoltage or overtemperature event.

The device maintains excellent signal integrity through the optimization of both R_{ON} and BW while protecting the system with 0 V to 20 V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Powered-off Protection

When the TMUX1072 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the *Electrical Specifications*

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

8.3.2 Overvoltage Detection

When a voltage on the COM pin exceeds the V_{OVP_TH}, the open drain output FLT pin pulls the pin low to indicate an overvoltage event has been detected. The open drain output will release the FLT pin when the voltage on the COM pin returns below the V_{OVP_TH}.

8.3.3 Overtemperature Detection

When the junction temperature of the device exceeds the overtemperature detection threshold T_{OTD_TH}, the open drain output FLT pin pulls the pin low to indicate an overtemperature event has been detected. The open drain output releases the FLT pin when the junction temperature returns below the T_{OTD_TH}.

8.3.4 Overvoltage Protection

The OVP of the TMUX1072 is designed to protect the system from overvoltage conditions up to 20 V on the COM1 and COM2 pins. Figure 12 depicts an event where up to 20 V could appear on COM1 and COM2 that could pass through the device and damage components behind the device.

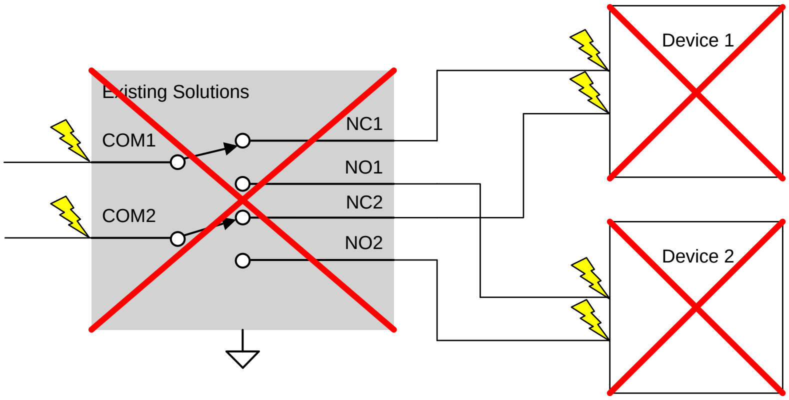


Figure 12. Existing Solution Being Damaged by a Short, 20 V

The TMUX1072 opens the switches and protect the rest of the system by blocking the 20 V as depicted in Figure 13.

ADVANCE INFORMATION

Feature Description (continued)

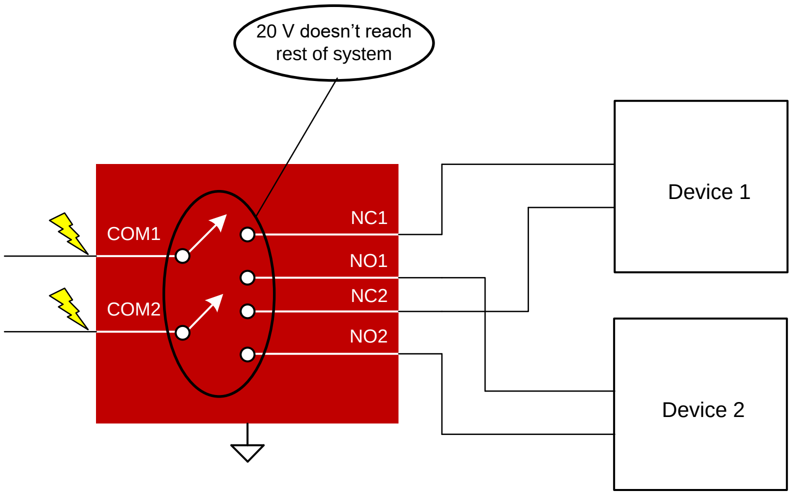


Figure 13. Protecting During a 20-V Short

Figure 14 is a waveform showing the voltage on the pins during an overvoltage scenario.

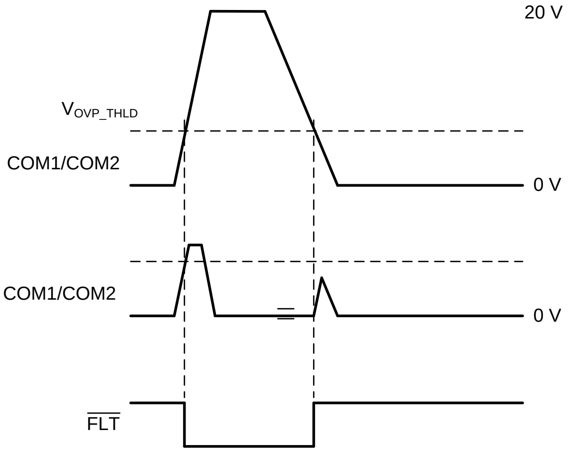


Figure 14. Overvoltage Protection Waveform, 20 V

8.4 Device Functional Modes

8.4.1 Pin Functions

Table 1. Function Table

$\overline{OE}$	SEL1	SEL2	COM1 Connection	COM2 Connection
H	X	X	High-Z	High-Z
L	L	L	COM1 to NC1	COM2 to NC2
L	L	H	COM1 to NC1	COM2 to NO2
L	H	L	COM1 to NO1	COM2 to NC2
L	H	H	COM1 to NO1	COM2 to NO2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many applications in which processors and microcontrollers have a limited number of I/Os. This IC can effectively expand the limited number of I/Os by switching between multiple signal paths in order to interface them to a single processor or microcontroller. The device can also be used to connect a single microcontroller to two signal paths. With independent control of the two switches using SEL1 and SEL2, TMUX1072 can be used to cross switch single ended signals.

9.2 Typical Application

The TMUX1072 is used to switch signals between the high speed signal paths that may be exposed to a connector or near a bus which could experience an overvoltage condition. The TMUX1072 has internal pull-down resistors on SEL1, SEL2, and $\overline{\text{OE}}$. The pull-down on SEL1 and SEL2 pins ensure the NC1/NC2 channel is selected by default. The pull-down on $\overline{\text{OE}}$ enables the switch when power is applied.

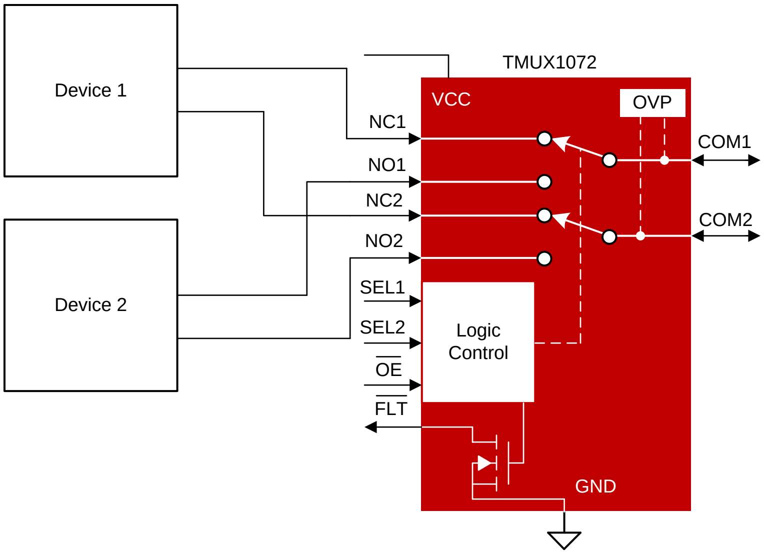


Figure 15. Typical TMUX1072 Application

9.2.1 Design Requirements

The TMUX1072 has internal pulldown resistors on SEL1, SEL2, and $\overline{\text{OE}}$, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the NC1 and NC2 channels are selected by default. The internal pull-down resistor on $\overline{\text{OE}}$ enables the switch when power is applied to VCC.

9.2.2 Detailed Design Procedure

The TMUX1072 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI does recommend a 100-nF bypass capacitor placed close to TMUX1072 VCC pin.

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin. TI recommends placing a 100-nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the signal traces.
2. The high-speed traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded.
3. Route the high-speed signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC’s that use or duplicate clock signals.
6. Avoid stubs on the high-speed signals because they cause signal reflections.
7. Route all high-speed signal traces over continuous planes (VCC or GND), with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. For high frequency systems, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see High Speed Layout Guidelines (SCAA082)

11.2 Layout Example

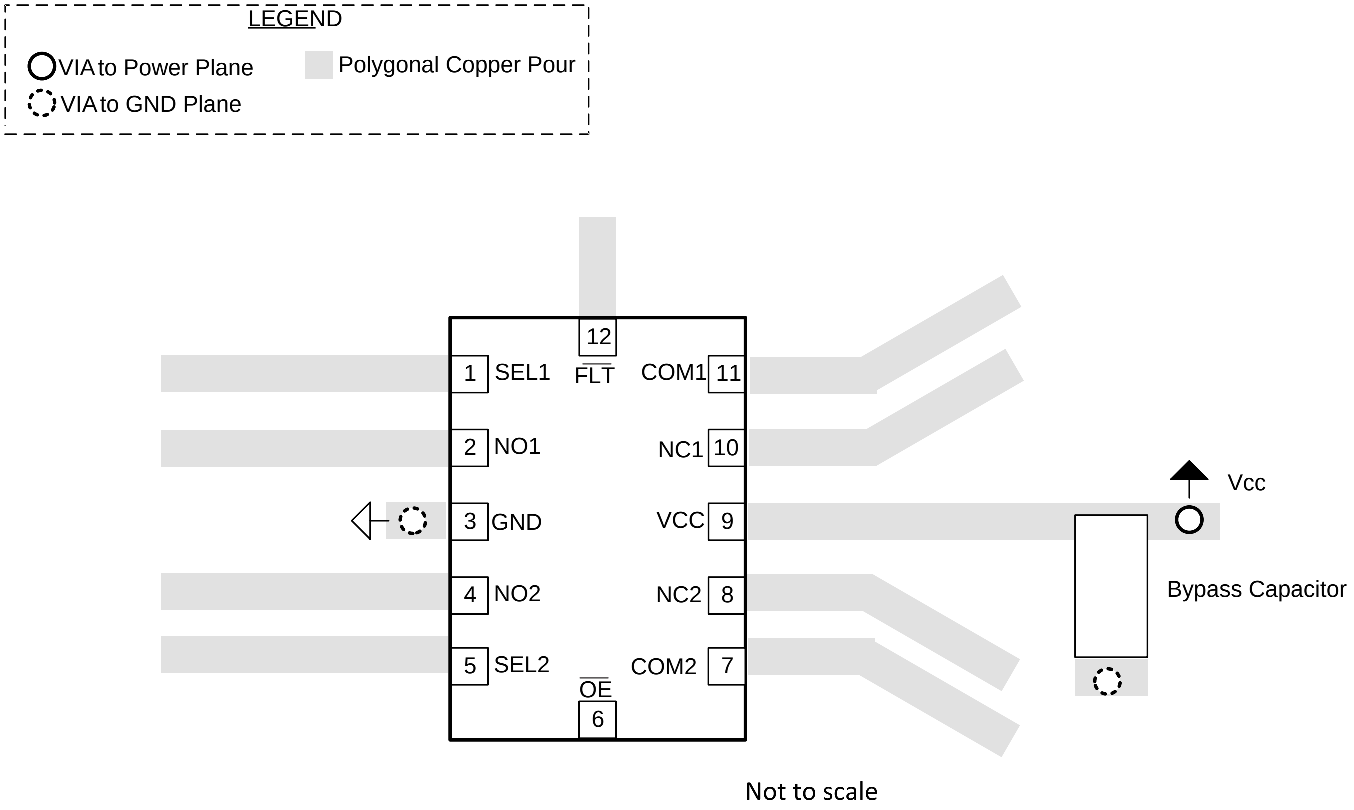


Figure 16. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *High-Speed Layout Guidelines Application Report*
- *High-Speed Interface Layout Guidelines*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX1072DGSR	ACTIVE	VSSOP	DGS	10	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX1072DGSR	PREVIEW	VSSOP	DGS	10	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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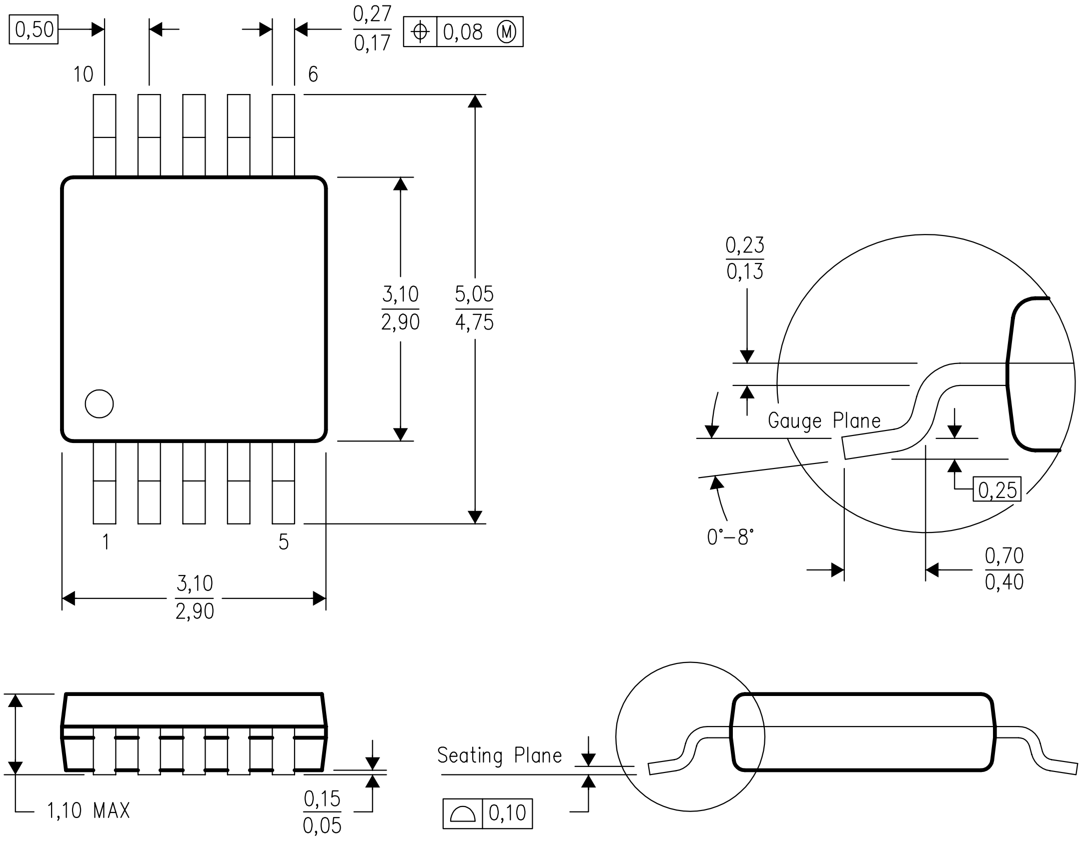
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation BA.

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