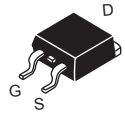
CEP13N10/CEB13N10

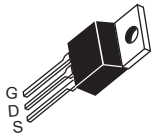
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

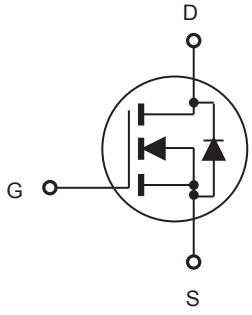
- 100V, 12.8A, $R_{DS(ON)}$ = 180mΩ @V_{GS} = 10V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 package.



CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	12.8	A
Drain Current-Pulsed [a]	I_{DM}	50	A
Maximum Power Dissipation @ T_C = 25°C	P_D	65	W
- Derate above 25°C		0.43	W/°C
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.3	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6A		140	180	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D = 6A		5		S
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		295		pF
Output Capacitance	C_{oss}			85		pF
Reverse Transfer Capacitance	C_{rss}			35		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 80, I_D = 12.8A, V_{GS} = 10V, R_{GEN} = 9.1Ω		10	20	ns
Turn-On Rise Time	t_r			8	16	ns
Turn-Off Delay Time	$t_{d(off)}$			17	35	ns
Turn-Off Fall Time	t_f			8	16	ns
Total Gate Charge	Q_g	V_{DS} = 80V, I_D = 12.8A, V_{GS} = 10V		12	16	nC
Gate-Source Charge	Q_{gs}			3.3		nC
Gate-Drain Charge	Q_{gd}			5.3		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				12.8	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 12.8A			1.5	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

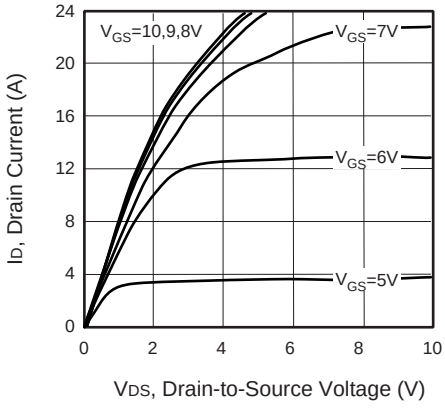


Figure 1. Output Characteristics

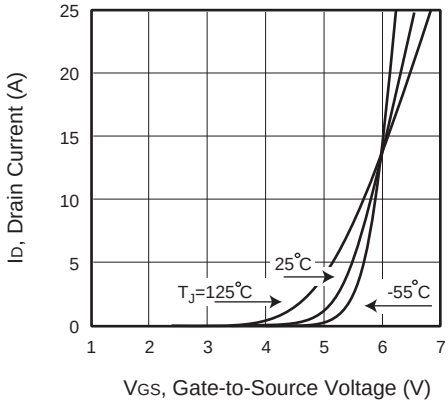


Figure 2. Transfer Characteristics

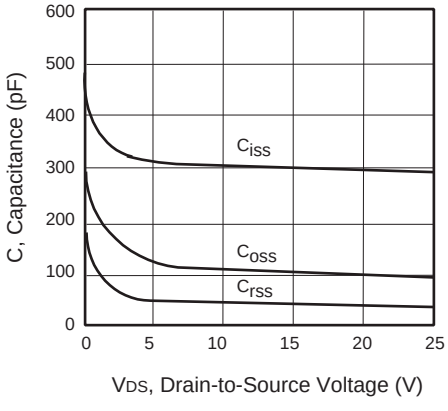


Figure 3. Capacitance

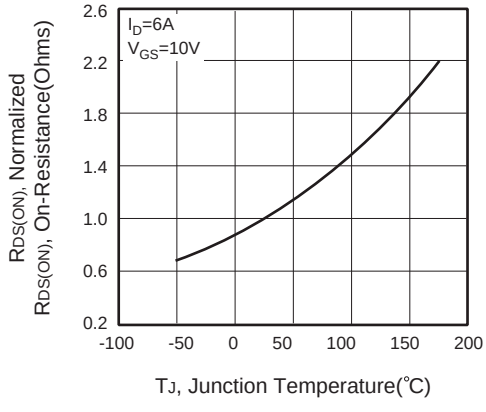


Figure 4. On-Resistance Variation with Temperature

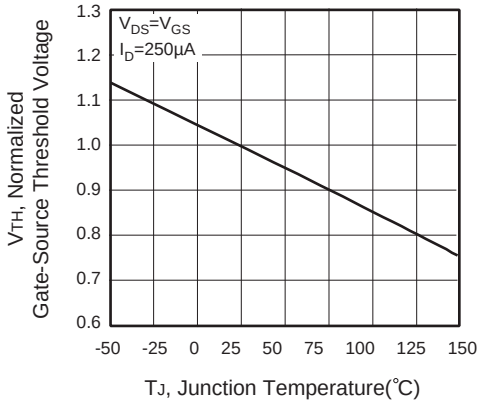


Figure 5. Gate Threshold Variation with Temperature

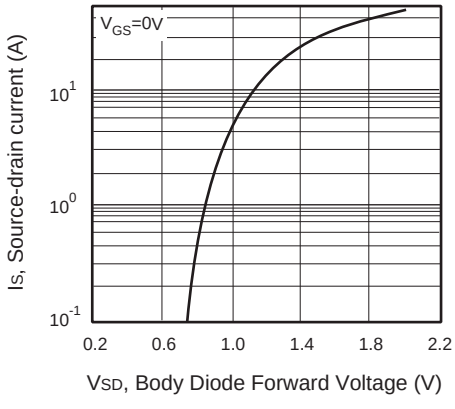


Figure 6. Body Diode Forward Voltage Variation with Source Current

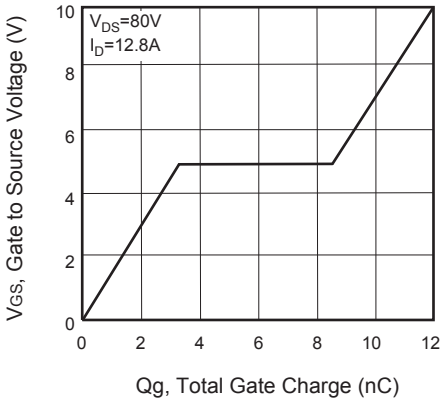


Figure 7. Gate Charge

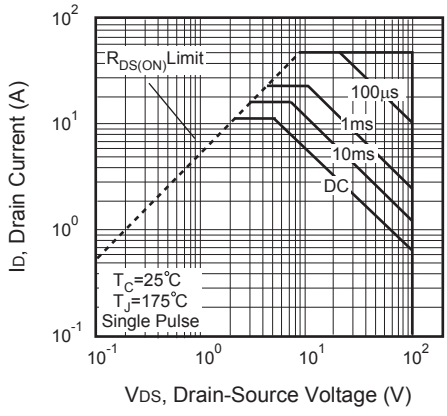


Figure 8. Maximum Safe Operating Area

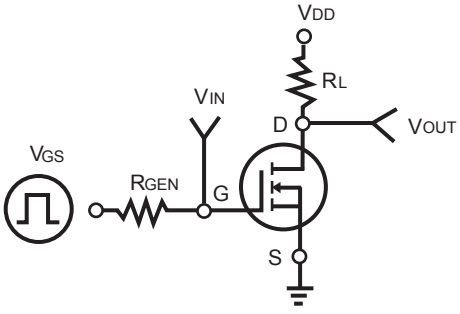


Figure 9. Switching Test Circuit

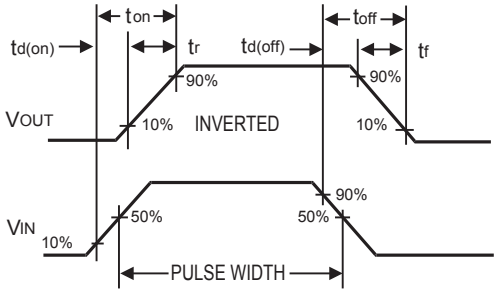


Figure 10. Switching Waveforms

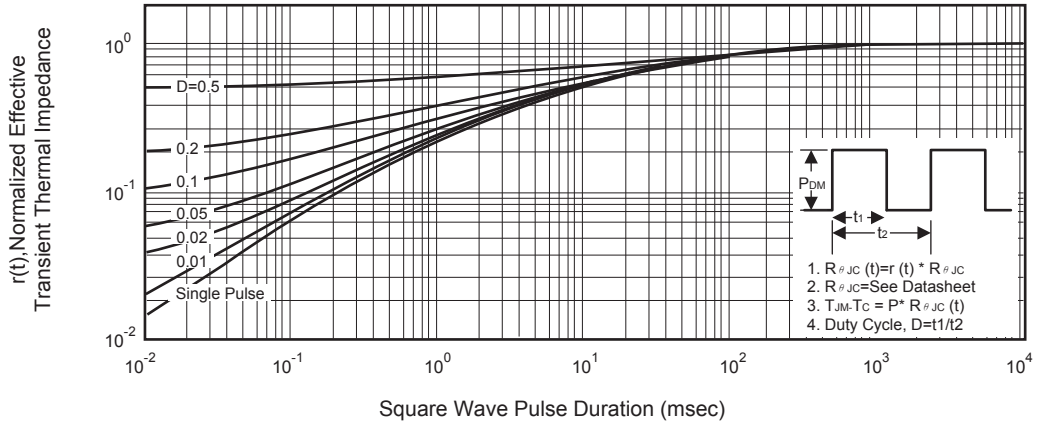


Figure 11. Normalized Thermal Transient Impedance Curve