LOGIC DEVICES INCORPORATED

L2340
Digital Synthesizer

FEATURES

- Digital Waveform Synthesis at 50 MHz
- 24-Bit Polar Phase Angle Accuracy
- User-selectable Waveform Synthesis, Frequency Modulation, or Phase Modulation.
- Amplitude Input for Amplitude Modulation and Gain Adjustment.
- Replaces TRW/Raytheon/Fairchild TMC2340A
- 120-pin PQFP

DESCRIPTION

The **L2340** is a digital synthesizer that performs waveform synthesis, modulation, and demodulation.

The L2340 automatically generates quadrature matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format with15-bit amplitude and 32-bit phase inputs.

Output waveforms can be phase or frequency modulated. Digital output frequencies are restricted to the Nyquist limit.

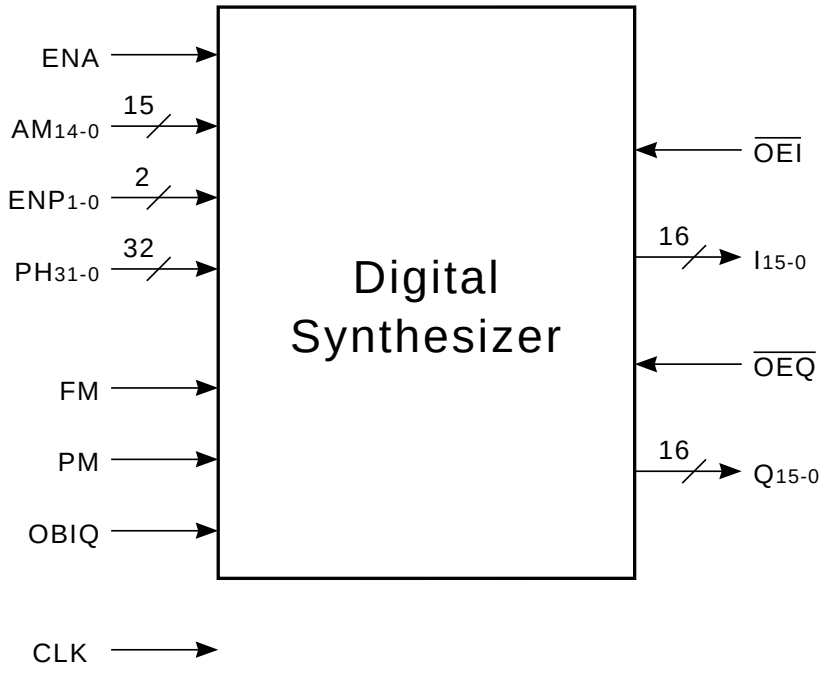
Functional Description

The L2340 converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) coordinates. The user selects the numeric format. A valid transformed result is seen at the output after 22 clock cycles and will continue upon every clock cycle thereafter.

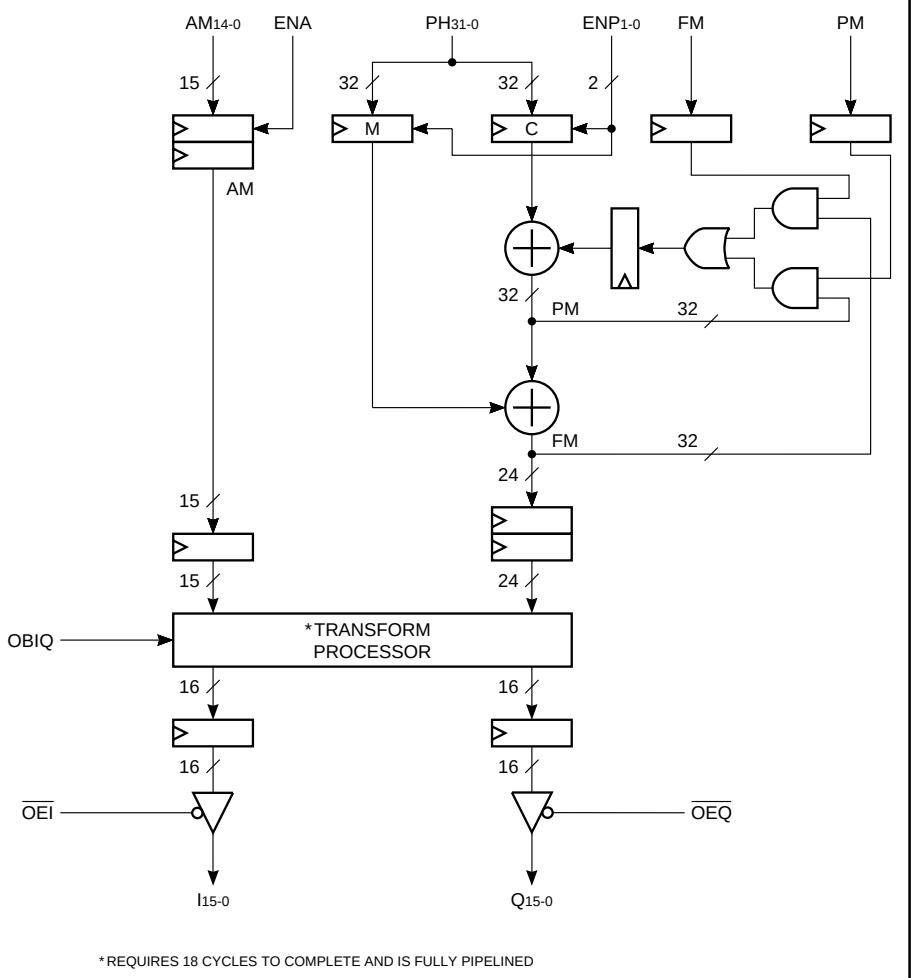
15-bit amplitude and 32-bit phase data are input into the L2340 to produce an output of 16-bit rectangular data. The user may select the data format to either 16-bit offset binary or 15-bit unsigned magnitude format. High accuracy phase increment values with minimal accumulation error is accomplished by use of a 32-bit phase accumulator.

The phase accumulator structure supports frequency or phase modulation and is selected by ENP_{1-0} and accumulator controls FM and PM.

L2340 Block Diagram



L2340 Functional Block Diagram



*REQUIRES 18 CYCLES TO COMPLETE AND IS FULLY PIPELINED

SIGNAL DEFINITIONS

Power

Vcc and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

AM14-0 — Amplitude Modulation Data Input

AM14-0 is the 15-bit Amplitude Modulation Data input port. AM14-0 is latched on the rising edge of CLK.

PH31-0 — Phase Angle Data Input

PH31-0 is the 32-bit Phase Angle Data input port. Input phase accumulators are loaded through this port into registers enabled by ENP1-0. PH31-0 is latched on the rising edge of CLK.

Outputs

I15-0 — x-coordinate Data Output

I15-0 is the 16-bit Cartesian x-coordinate Data output port. When $\overline{OEI}$ is HIGH, I15-0 is forced into the high-impedance state. I15 is forced HIGH if OBIQ is LOW.

Q15-0 — y-coordinate Data Output

Q15-0 is the 16-bit Cartesian y-coordinate Data output port. When $\overline{OEQ}$ is HIGH, Q15-0 is forced into the high-impedance state. Q15 is forced HIGH if OBIQ is LOW.

Controls

ENA — Amplitude Modulation Data Input Enable

When ENA is HIGH, AM is latched into the input register on the rising edge of clock. When ENA is LOW, the value stored in the register is unchanged.

ENP1-0 — Phase Modulation Data Input Control

ENP1-0 is the 2-bit Phase Modulation Data Input Control that determines one of the four modes shown in Table 1. 'M' is the Modulation Register and 'C' is the Carrier Register as shown in the Functional Block Diagram.

Table 1. Register Operation

ENP1-0	Configuration
0 0	No registers enabled, current data held
0 1	M register input enabled, C data held
1 0	C register input enabled, M data held
1 1	M register = 0, C register input enabled

Table 2. Accumulator Control

FM	PM	Configuration
0	0	No accumulation (normal operation)
0	1	PM accumulator path enabled
1	0	FM accumulator path enabled
1	1	Logical OR of PM and FM (Nonsensical)

FM, PM — Frequency Modulation, Phase Modulation Control

FM and PM is the 2-bit Frequency Modulation/Phase Modulation Control that determines one of the four modes shown in Table 2. When full-scale is exceeded, the accumulator will roll over correctly allowing continuous phase accumulation through 2π radians.

OBIQ — Data Input/Output Format Select

When OBIQ is HIGH, offset binary format is selected. When OBIQ is LOW, unsigned format is selected.

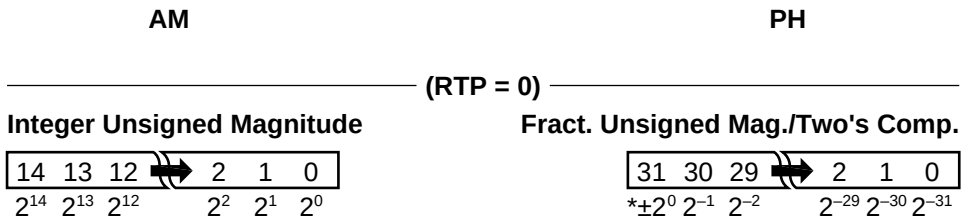
$\overline{OEI}$ — x-coordinate Data Output Enable

When $\overline{OEI}$ is LOW, I_{15-0} is enabled for data output. When $\overline{OEI}$ is HIGH, I_{15-0} is placed in a high-impedance state.

$\overline{OEQ}$ — y-coordinate Data Output Enable

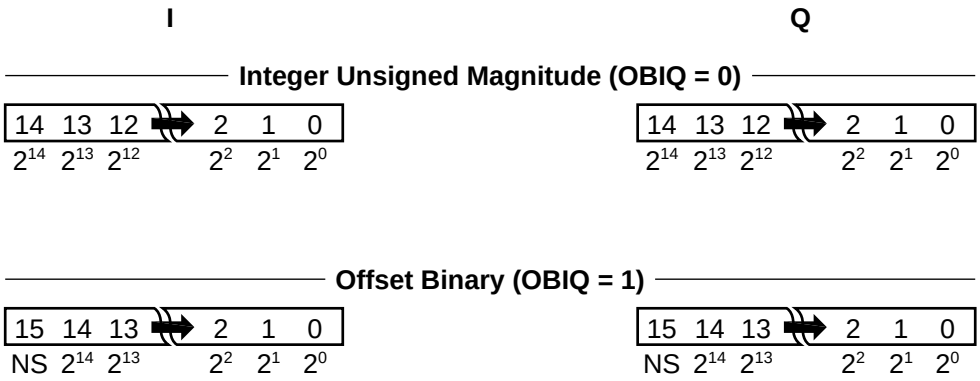
When $\overline{OEQ}$ is LOW, Q_{15-0} is enabled for data output. When $\overline{OEQ}$ is HIGH, Q_{15-0} is placed in a high-impedance state.

FIGURE 1A. INPUT FORMATS



*±2^0 denotes two's complement sign or highest magnitude bit. Since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as ±π.

FIGURE 1B. OUTPUT FORMATS



NS denotes negative sign. (i.e. '1' negates the number)

Circle Test

When performing a coordinate transformation, inaccuracies are introduced by a combination of quantization and approximation errors. The accuracy of a coordinate transformer is dependent on the word length used for the input variables, the word length used for internal calculations, as well as the number of iterations or steps performed. Truncation errors are due to the finite word length and approximation errors are due to the finite number of iterations. For example, in the case of performing a polar-to-rectangular transformation, the accuracy of the rotation will be determined by how closely the input rotation angle was approximated by the summation of sub-rotation angles.

In this study, we compare how accurately a coordinate transformer with a 16-bit internal processor versus a 24-bit internal processor can calculate all the coordinates of a circle. By setting the radius to 7FFFH, θ is incremented using the accumulator of the L2340 in steps of 0000 4000H until all the points of a full circle are calculated into rectangular coordinates.

The resulting rectangular coordinates were plotted and graphed. A graphical representation of the resulting vectors for both 16-bit and 24-bit internal processors are compared at 45°. Theoretically, a perfect circle is the desired output but when the resulting vectors from a coordinate transformer with 16-bit internal processor are graphed and displayed as shown in Figure 2, we see significant errors due to the inherent properties of a digital synthesizer. In comparison, the 24-bit internal processor proves to be significantly more accurate than a 16-bit internal processor due to minimization of truncation errors. In many applications, this margin of error will introduce noise when performing waveform sythesis, modulation, and demodulation.

Data values for Figure 2 and Figure 3 are shown in Table 3. By looking at these values, we observe the step resolution on a 16-bit internal processor is not 1 unit in the x and y. In most cases, the minimum step resolution is 2 units in the x and y. On the other hand, step resolution on a 24-bit internal processor is 1 unit in the x and y thus resulting in greater accuracy.

The minimum theoretical angle resolution that could be produced is 0.00175° when x = 7FFFH and y = 1H. A 16-bit internal processor can produce a minimum angle resolution of only 0.00549° and will not be able to properly calculate the theoretical minimum angle resolution. On the other hand, a 24-bit internal processor can produce a minimum angle resolution of 0.00002° and could therefore properly calculate the theoretical minimum angle resolution.

FIGURE 2. CIRCLE TEST RESULT NEAR 45° (16-BIT INTERNAL PROCESSOR)

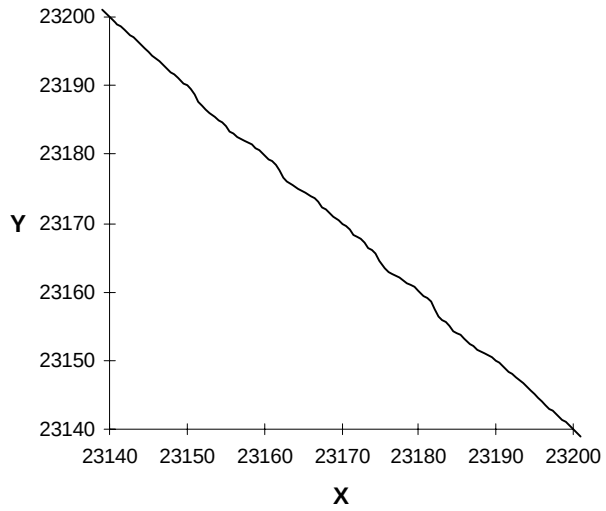


FIGURE 3. CIRCLE TEST RESULT NEAR 45° (24-BIT INTERNAL PROCESSOR)

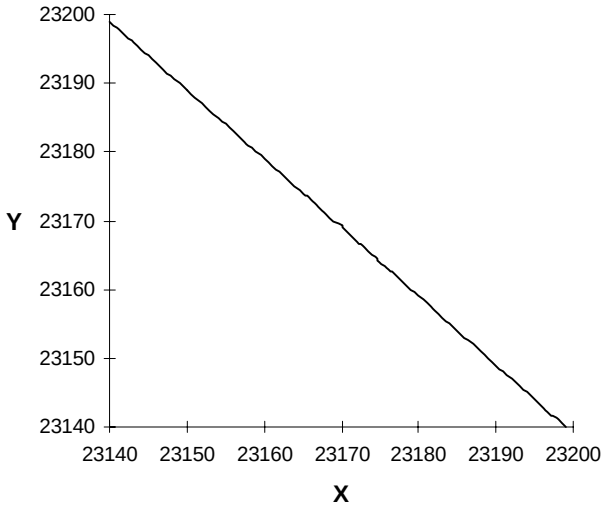


TABLE 3. RESULTANT DATA VALUES OF CIRCLE TEST NEAR 45°

16-bit Internal Processor				24-bit Internal Processor			
x	x (HEX)	y	y (HEX)	x	x (HEX)	y	y (HEX)
23201	5AA1	23139	5A63	23199	5A9F	23140	5A64
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23198	5A9E	23141	5A65
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23199	5A9F	23141	5A65	23197	5A9D	23142	5A66
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23196	5A9C	23143	5A67
23197	5A9D	23143	5A67	23195	5A9B	23144	5A68
23197	5A9D	23143	5A67	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23194	5A9A	23145	5A69
23195	5A9B	23145	5A69	23193	5A99	23146	5A6A
23195	5A9B	23145	5A69	23192	5A98	23147	5A6B
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	03148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23191	5A97	23148	5A6C
23192	5A98	23148	5A6C	23190	5A96	23149	5A6D
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23189	5A95	23150	5A6E
23190	5A96	23150	5A6E	23188	5A94	23151	5A6F
23187	5A93	23152	5A70	23187	5A93	23152	5A70
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23187	5A93	23152	5A70	23186	5A92	23153	5A71
23185	5A91	23154	5A72	23185	5A91	23154	5A72
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23185	5A91	23154	5A72	23184	5A90	23155	5A73
23183	5A8F	23156	5A74	23183	5A8F	23156	5A74

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			95	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			5	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

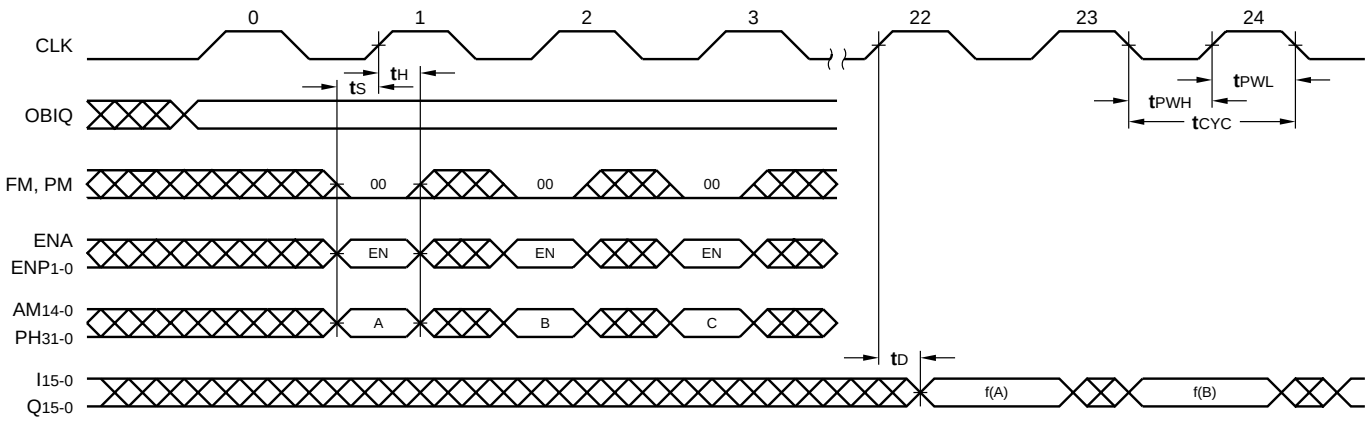
		L2340–					
		50*		25*		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	10		8		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	12		7		6	
t_H	Input Hold Time	1		0		1	
t_D	Output Delay		22		18		16
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		13		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

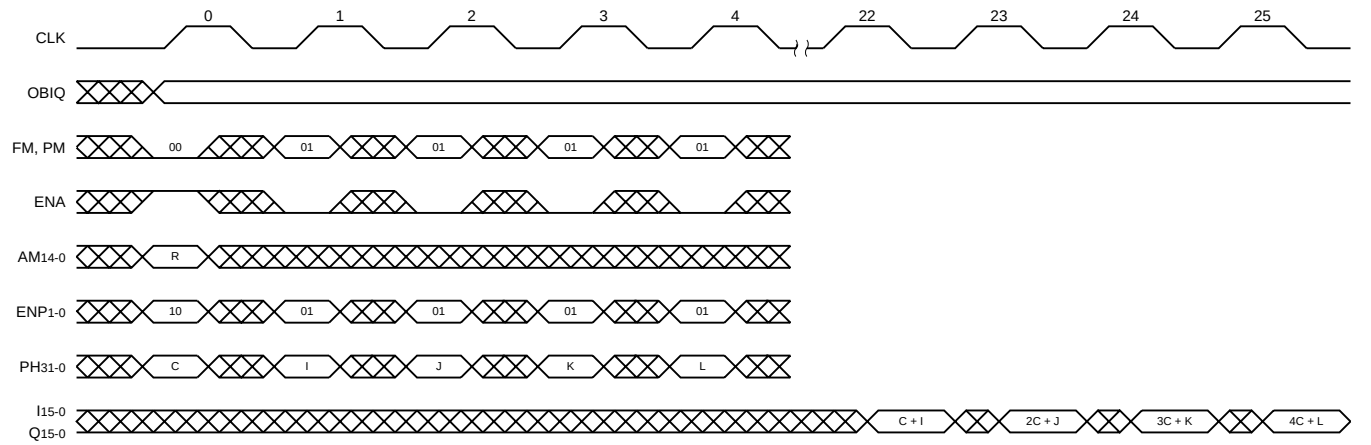
		L2340–					
		50*		25*		20*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20	
t_{PWL}	Clock Pulse Width Low	11		9		7	
t_{PWH}	Clock Pulse Width High	8		7		6	
t_S	Input Setup Time	13		7		6	
t_H	Input Hold Time	2		2		1	
t_D	Output Delay		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		14		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		14		13

***DISCONTINUED SPEED GRADE**

SWITCHING WAVEFORMS: NO ACCUMULATION



SWITCHING WAVEFORMS: PHASE MODULATION



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

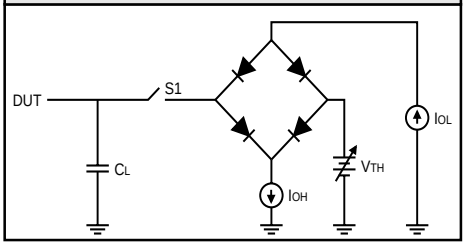
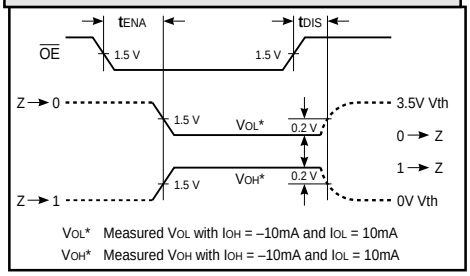
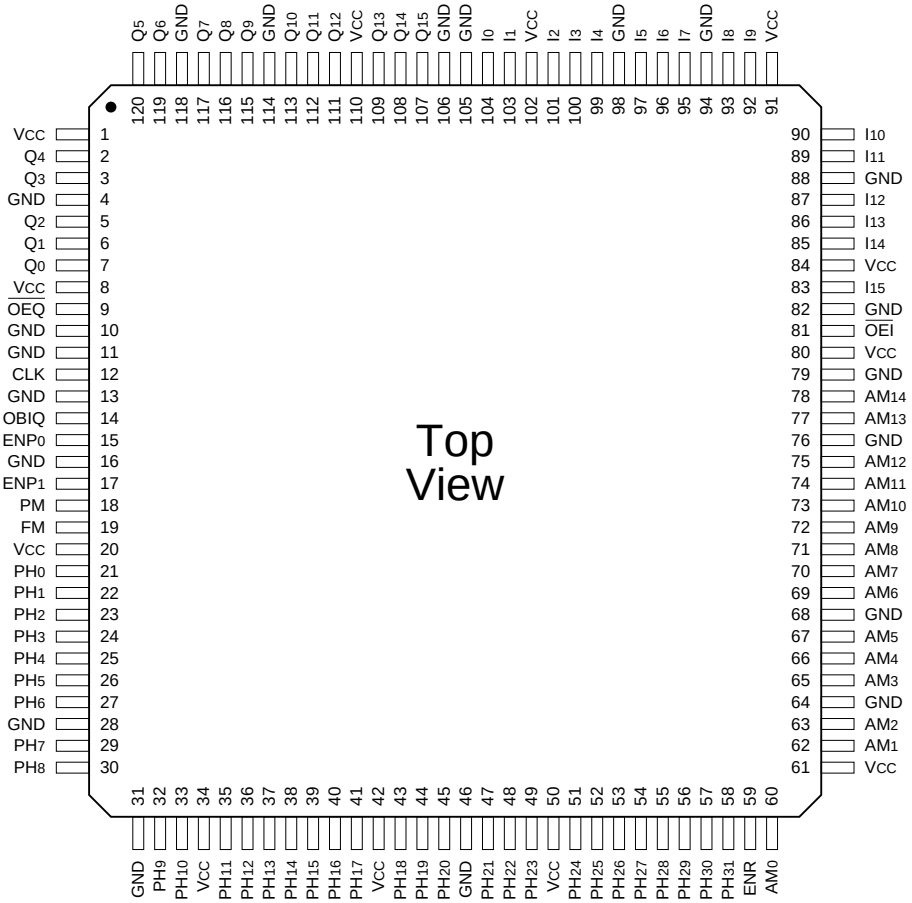


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

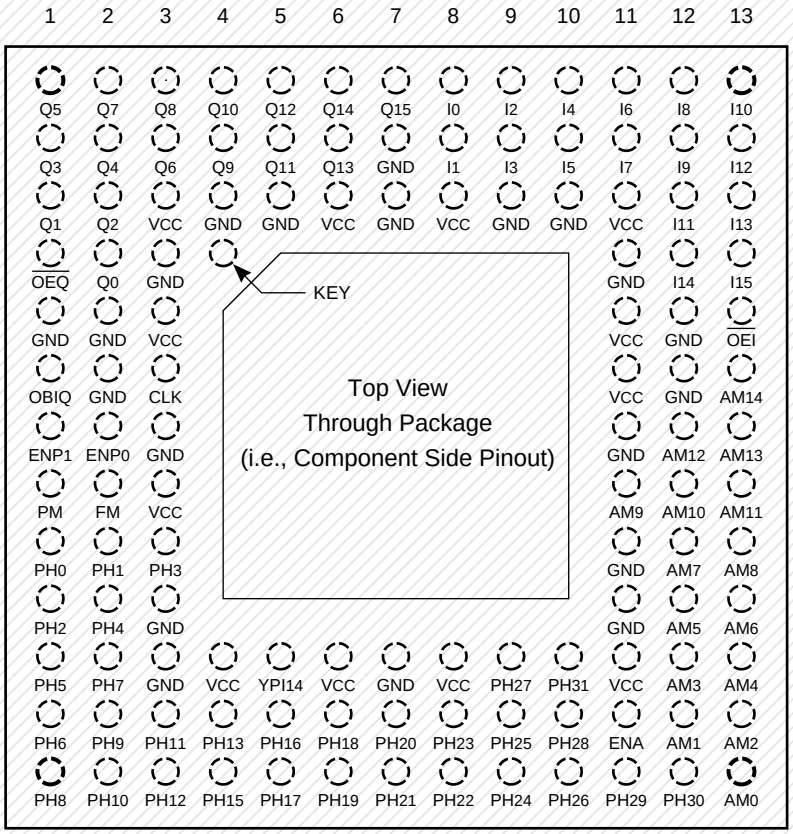
120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
20 ns	L2340QC20

ORDERING INFORMATION

120-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — Commercial Screening
	–55°C to +125°C — Commercial Screening
	–55°C to +125°C — MIL-STD-883 Compliant