High Efficiency DC/DC Power Module

VPN12AD1E-FU BOOST 1.5A

FEATURES:

- High Power Density Power Module
- Maximum Load: 1.5A
- Input Voltage Range from 5.5V to 30V
- Output Voltage Range from 20V to 45V
- 95% Peak Efficiency
- Protections (OTP, OVP Non-latching)
- Input Voltage UVLO
- Internal Soft Start
- Switching Frequency, 350kHz
- Small size (15.0mm x 15.0mm x 8mm)
- Pb-free Available (RoHS compliant)
- MSL 3, 260ºC Reflow

APPLICATIONS:

- Automotive LED lighting
- Instrument Cluster
- ADAS, Infotainment, HUD

GENERAL DESCRIPTION:

The POL module is non-isolated dc-dc converter that can deliver up to 1.5A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and two voltage dividing resistor to perform properly.

Other features include remote enable function, internal soft-start, and wettable flank packaging available.

The low profile and compact size package (15mm × 15mm x 8mm) is suitable for automated assembly by standard surface mount equipment. The POL module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

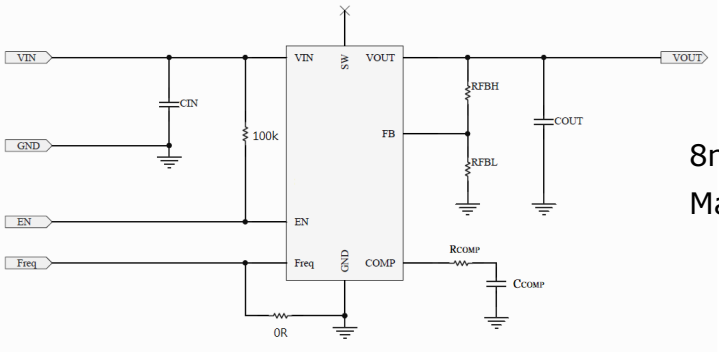


FIG.1 TYPICAL APPLICATION CIRCUIT

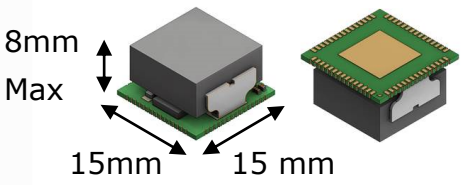


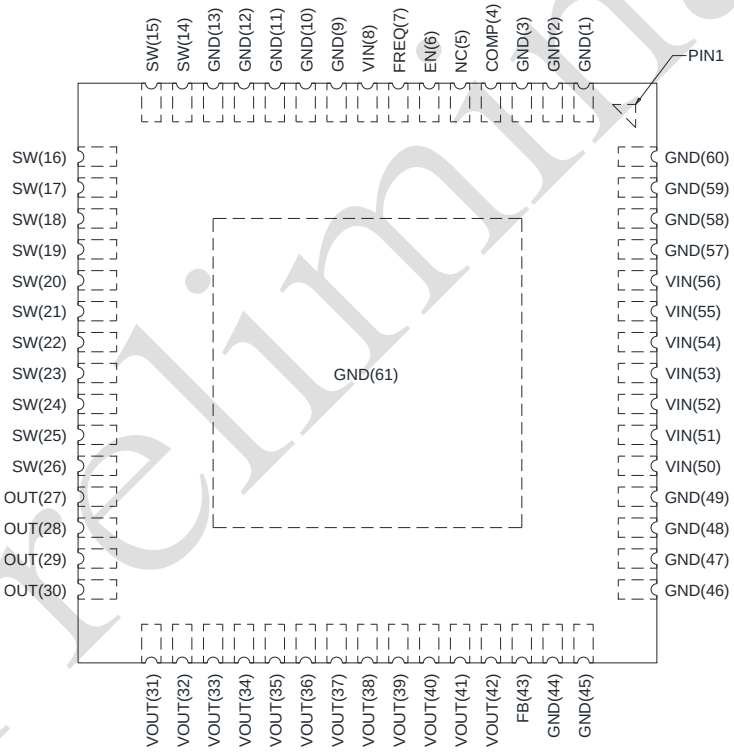
FIG.2 HIGH DENSITY POWER MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
VPN12AD1E-FU	-40 ~ +105	QFN	Level 3	-

Order Code	Packing	Quantity
VPN12AD1E-FU	Tape and reel	TBD

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
GND	1~3,9~13,44~49,56~60	**Ground;** Connect to system ground.
COMP	4	**Compensation Input;** Connect R and C network to improve the stability of the regulation loop.
NC	5	**Not Connected;**
EN	6	**Enable;** Apply logic high signal to enable device.
FS	7	**Frequency Select Input;** Connect to GND to set frequency, Define is 350kHz.
VIN	8,50~56	**Supply Input Voltage;** Power input pin.
SW	14~26	**Switch Output;** Switching node pin. Connect pins together at the PCB for thermal performance.
VOUT	27~42	**Output Voltage;** Power output pin.
FB	43	**Feedback;** Feedback input. Connect an external resistor divider from the output to GND to set the output voltage.

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures outside of warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-0.3	-	+45.0	V
EN to GND		-40	-	+45.0	V
FB to GND		-0.3	-	+5.5	V
FS to GND		-0.3	-	+5.5	V
COMP to GND		-0.3	-	+5.5	V
Tc		-	-	+135	℃
Tj		-40	-	+150	℃
Tstg		-40	-	+150	℃
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Charge Device Model (CDM)	-	-	500	V
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient.(Note1)	-	15.2	-	℃/W
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+9	-	+30	V
VOUT	Adjusted Output Voltage	+20.0	-	+45.0	V
Ta	Ambient Temperature	-40	-	+105	℃

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 75mm×58mm×1.6mm with 2 layers, 2 oz per layer. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm×1.6mm, 2 layers 2Oz .
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.
Conditions: T_A = 25 ºC, unless otherwise specified.
Vin=12V, Vout=40.0V, Cin=10uF/50V×2, Cout=10uF/50V×4

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
I_{IN}	Input supply bias current	Iout = 0A Vin = 12V, Vout = 40.0V	-	23	-	mA
I_S	Input supply current	Iout = 1.5A Vin = 12V, Vout = 40V	-	5.26	-	A
$V_{in(Off)}$	Input Under voltage Shutdown	VIN decreasing	3.75	-	-	V
$V_{in(On)}$	Input Voltage Startup	VIN increasing	-	-	4.75	V
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Vin=12V, Vout=40.0V	0.15	-	1.5	A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 9V to 16V Vout = 40.0V, Iout = 0.15A Vout = 40.0V, Iout = 1.5A	-	0.5	1	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0.15A to 1.5A Vin = 12.0V, Vout = 40.0V	-	0.5	1	%
$V_{OUT(AC)}$	Output ripple voltage	Iout = 1.5A Vin = 12.0V, Vout = 40.0V	-	260		mVp-p
Vo, set	Output voltage set point	TJ = 25°C, with 0.1% tolerance for external resistor used to set output voltage	-5.0	-	+5.0	%Vo,set
■ Boost Inductor Characteristics						
L_0	Inductance	DC Bias current at 0A	-	13	-	uH
L_{DCR}	Inductor DC resistance		-	23	-	mΩ
■ Control Characteristics						
V_{REF}	Reference voltage	TJ = -40~150°C	2.32	2.47	2.62	V
F_{OSC}	Oscillator frequency		300	350	400	kHz
V_{OV}	Over-voltage threshold level		-	110%	-	V_{FB}
■ EN Control						
V_{ENH}	Logic high Voltage	Module On	3	-	VIN	V
V_{ENL}	Logic low Voltage	Module Off	-	-	0.8	V
■ Fault Protection						
TP	Shutdown temperature		-	175	-	℃

TYPICAL PERFORMANCE CHARACTERISTICS: (40 VOUT)

Conditions: TA = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm×1.6mm, 2 layers 2Oz . The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Cin = 10uF/50V/1210x2, Cout = 10uF/50V/1210x4

The following figures provide the typical characteristic curves at 40Vout.

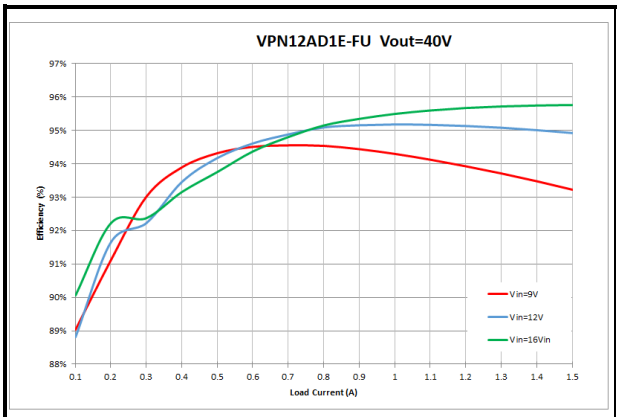


FIG.3 EFFICIENCY V.S. LOAD CURRENT

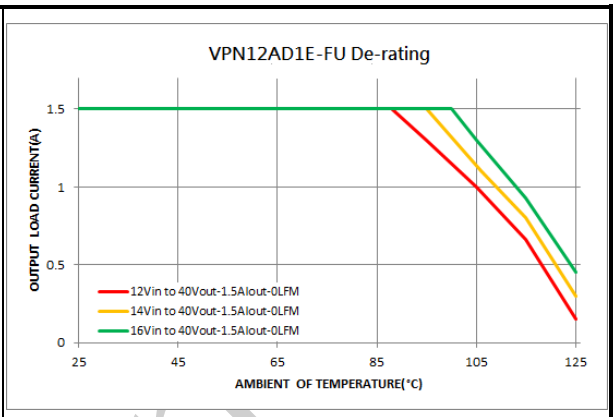


FIG.4 12VIN DE-RATING CURVE

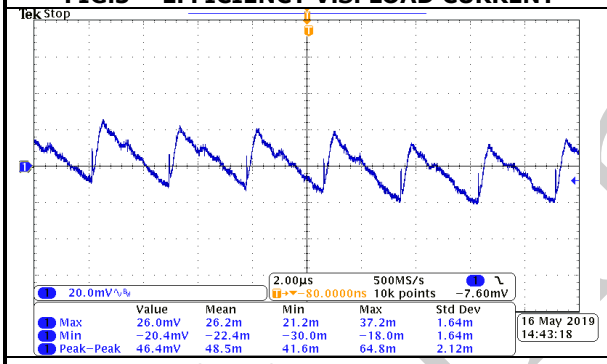


FIG.5 OUTPUT RIPPLE
(12VIN, 40VOUT, IOUT=0.15A)

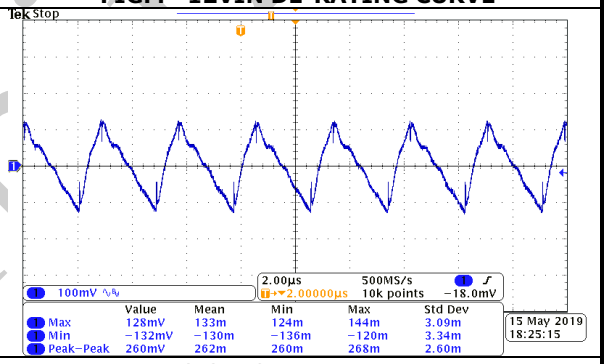


FIG.6 OUTPUT RIPPLE
(12VIN, 40VOUT, IOUT=1.5A)

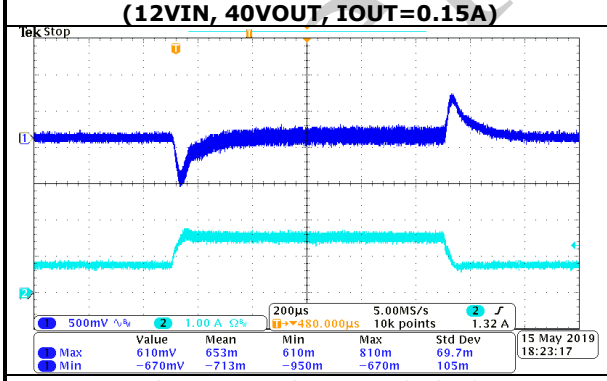


FIG.7 TRANSIENT RESPONSE
(12VIN, 40VOUT, 50% to 100% LOAD STEP)

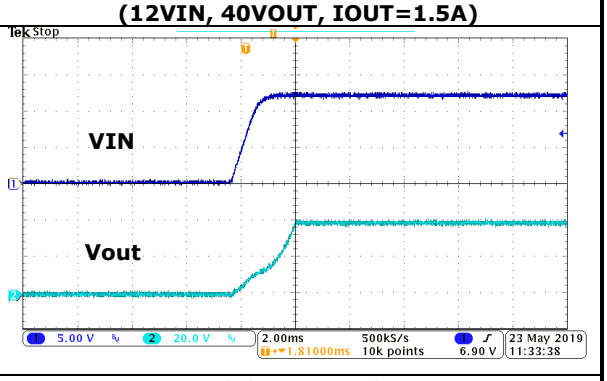


FIG.8 TURN-ON
(12VIN, 40VOUT, IOUT=1.5A)

APPLICATIONS INFORMATION: (Cont.)

Selecting the Input Capacitor:

The input requires a capacitor to supply the AC ripple current to the inductor, while limiting noise at the input source. Use a low-ESR capacitor with a value >6.8μF to minimize the Module noise. Ceramic capacitors are preferred, low-ESR electrolytic capacitors can also suffice. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the Module as possible. As an alternative, place a small, high-quality ceramic 0.1μF capacitor close to the Module and place the larger capacitor further away. If using the latter technique, electrolytic type capacitors for the larger capacitor. Place all ceramic capacitors close to the VPN12AD1E-FU.

Selecting the Output Capacitor:

The output capacitor maintains the DC output voltage. For best results, use low-ESR capacitors to minimize the output voltage ripple. The output capacitor's characteristics also affect regulatory control system's stability. For best results, use ceramic or low-ESR electrolytic capacitors. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and so the output voltage ripple is mostly independent of the ESR. The min. output capacitance is estimated as below formula, (Please also consider the bias voltage impacted the capacitance changing)

$$C_{OUT} \cong I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{V_{RIPPLE} \times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages, respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the value of the output capacitance.

$$V_{RIPPLE(ESR)} \cong \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}}$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor that satisfies the output ripple and load transient requirements of the design. 6.8μF-to-22μF ceramic capacitance is suitable for most applications. (Please also consider the bias voltage impacted the capacitance changing)

APPLICATIONS INFORMATION: (Cont.)

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 2.47V reference voltage. The output voltage can be programmed by the dividing resistor (R_{FBH} and R_{FBL}). The output voltage can be calculated by Equation 1, resistor choice may be referred TABLE 1.

$$VOUT(V) = 2.47 \times \left(1 + \frac{15.2k}{R_{FBL}}\right) \quad \text{(EQ.1)}$$

Vout	RFBH(Ohm)	RFBL (Ohm)
20V	15.2k	2.15k
30V	15.2k	1.37k
40V	15.2k	1k

TABLE 1 Resistor values for common output voltages

APPLICATIONS INFORMATION: (Cont.)

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

Figure 39 show the module application schematics for input voltage +12V.

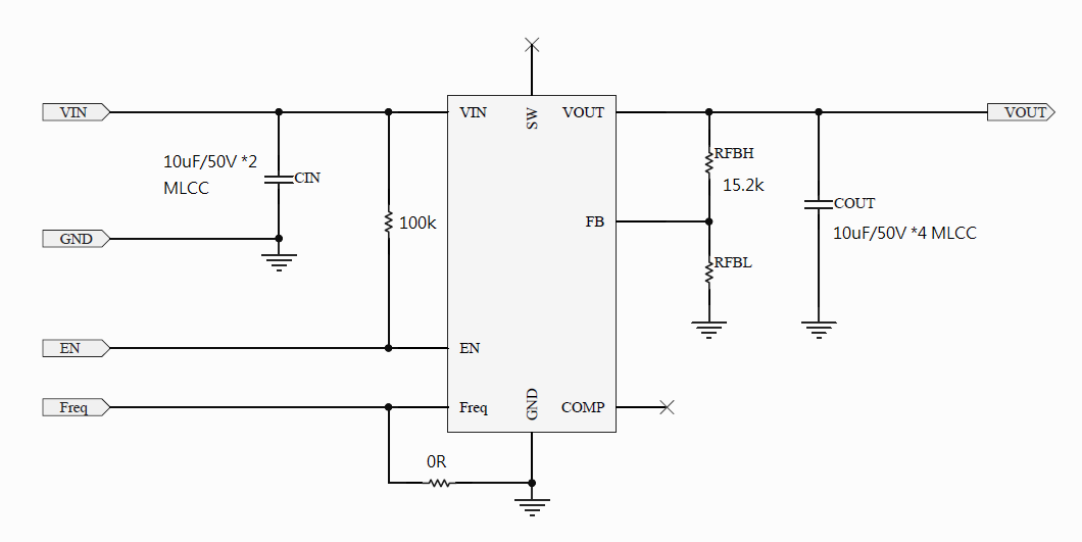


FIG.9 Reference Circuit for General Application

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 10.

1. The ground connection between pin 1~3, 9~13, 44~49, 56~60 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place ceramic capacitors between pin 50 ~ 56 (VIN), and pin 1~3, 57~60 (GND) for input side; and pin 27 ~ 42 (VOUT), and pin 44~49 (GND) for output side, as close to module as possible to minimize high frequency noise.
3. Keep the R_{FBH} and R_{FBL} connection trace to the module pin 43 (FB) shortly.
4. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. Bottom layer layout with Continuous ground plane for good EMI design.

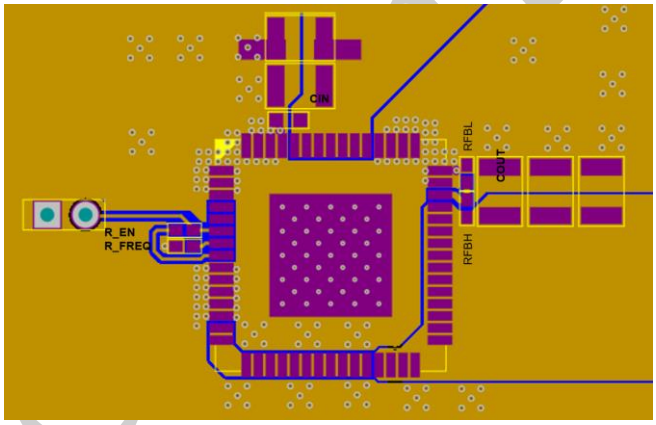


FIG.10 Recommendation TOP Layout

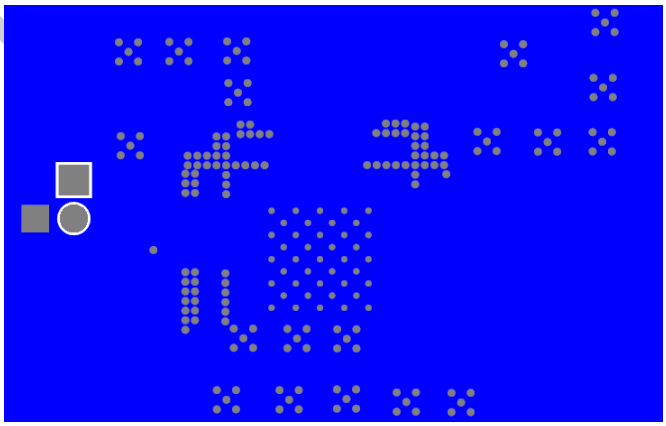
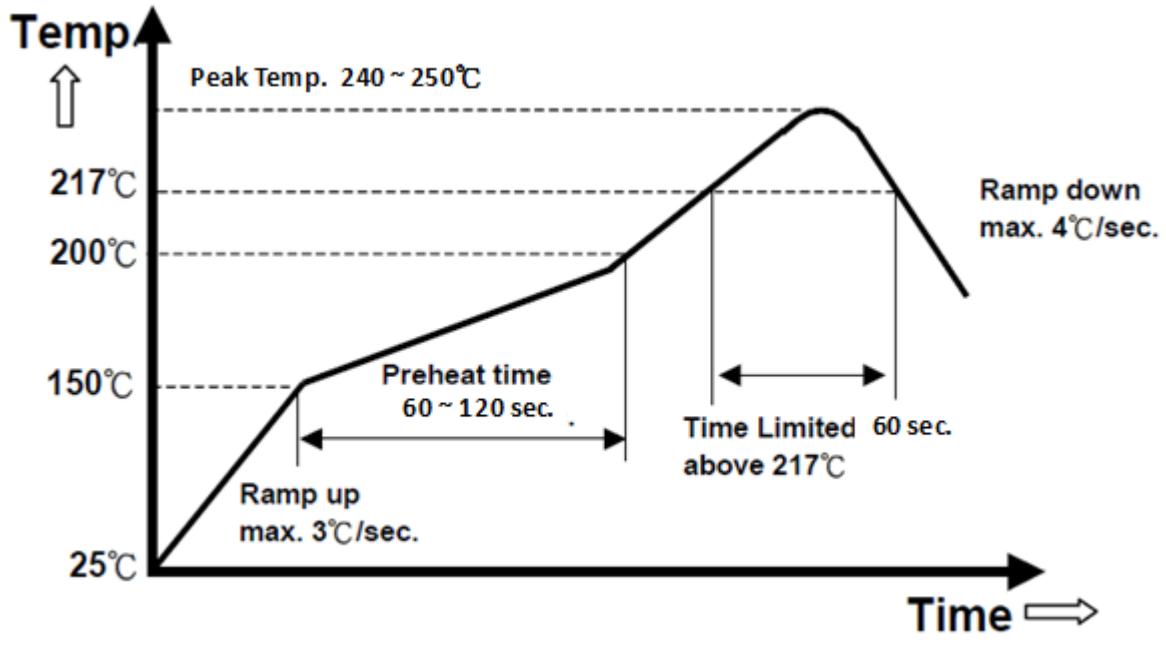


FIG.11 Recommendation Bottom Layout

REFLOW PARAMETERS:

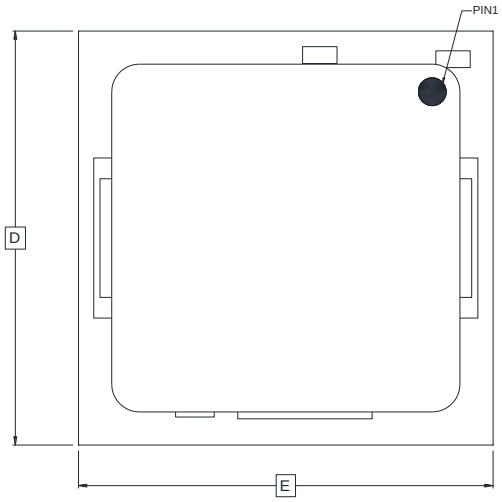
Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 56 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.



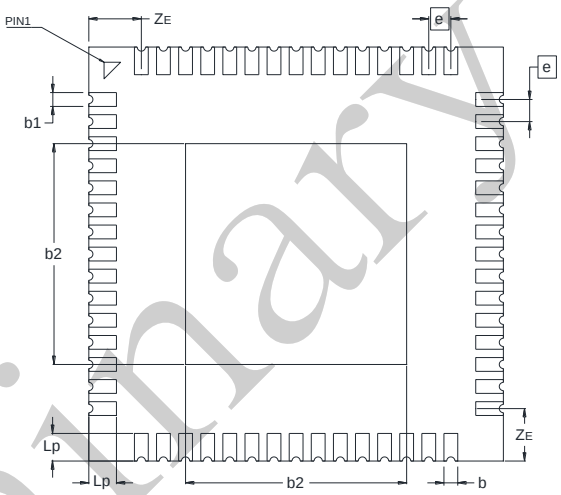
PACKAGE OUTLINE DRAWING:

Unit: mm

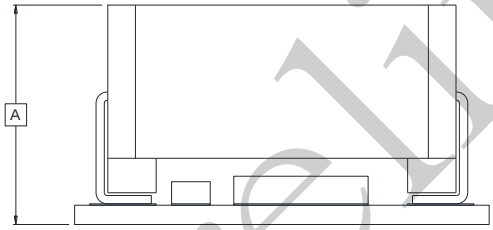
General Tolerances:±0.2mm



Top View



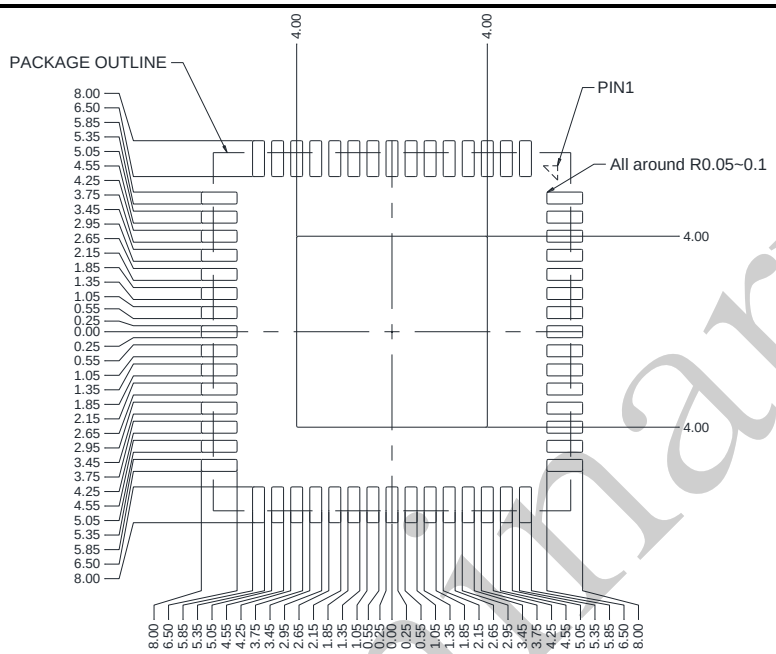
Bottom View



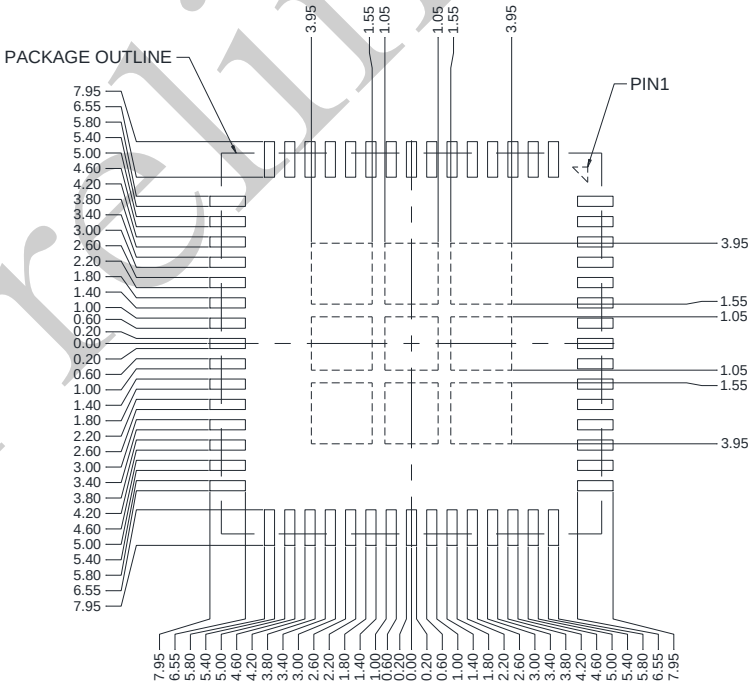
Side View

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	-	8.0
D	14.8	15	15.2
E	14.8	15	15.2
e	0.75	0.8	0.85
ZE	1.8	1.9	2.0
Lp	0.95	1.0	1.05
b1	0.45	0.5	0.55
b2	7.95	8.0	8.05

LAND PATTERN AND STENCIL PATTERN DRAWING:



TOP VIEW
TYPICAL RECOMMENDED LAND PATTERN



TOP VIEW
STENCIL PATTERN WITH SQUARE PADS