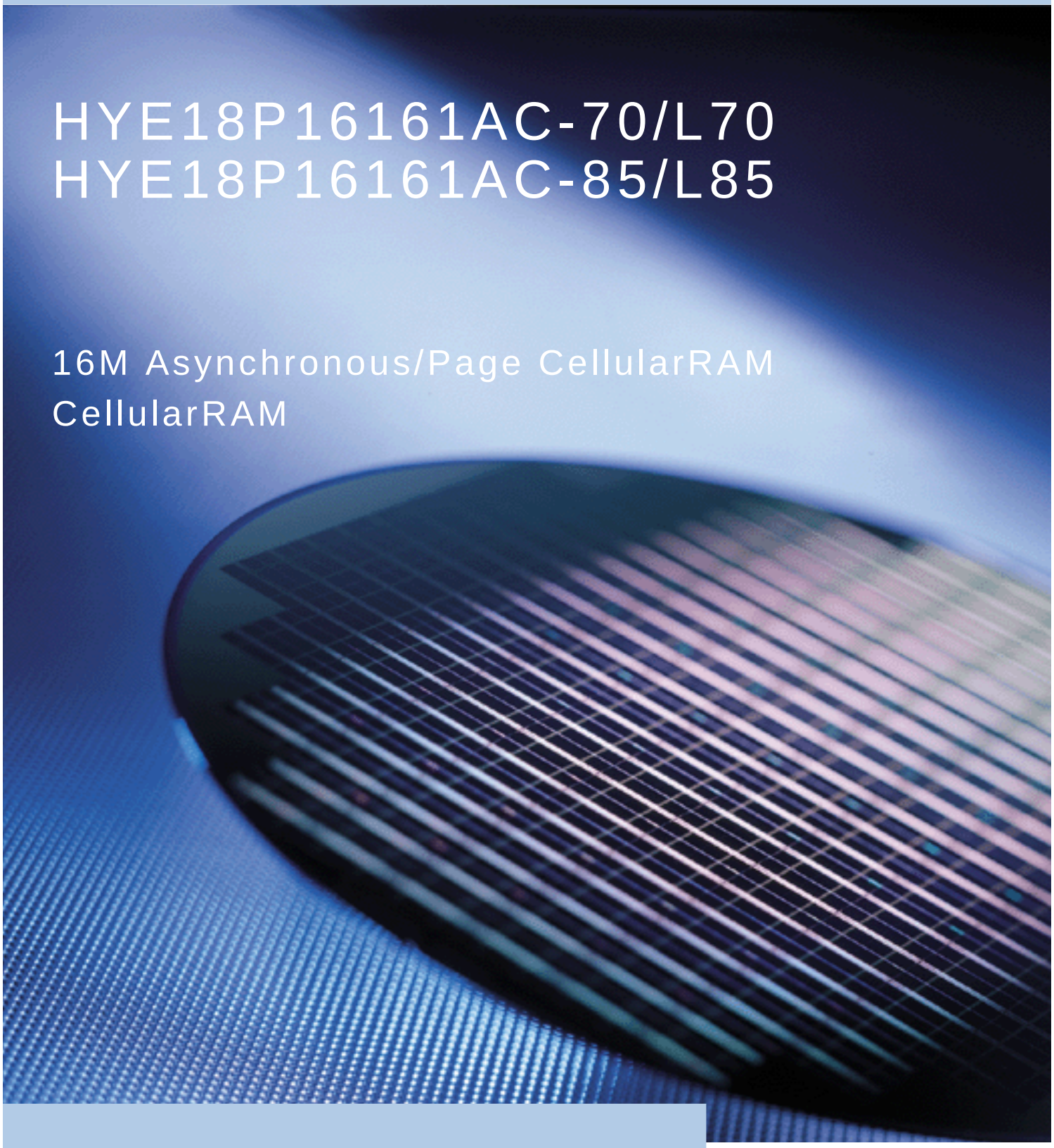
Data Sheet, V2.0, December 2003

HYE18P16161AC-70/L70
HYE18P16161AC-85/L85

16M Asynchronous/Page CellularRAM
CellularRAM



Memory Products

Never stop thinking.

Edition 2003-12-16

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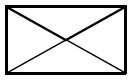
Previous Version: 1.9 (Target data sheet)

Page	Subjects (major changes since last revision)
all	2nd bin of Icc2 added. Marking for low-power part puts “L” in the place of “-”
all	tLZ, tBLZ, tOLZ are adjusted

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1 Overview . . . 8
1.1 Features . . . 8
1.2 General Description . . . 9
1.3 HYE18P16161AC(-/L)70/85 Ball Configuration . . . 10
1.4 HYE18P16161AC(-/L)70/85 Ball Definition and Description . . . 11
1.5 Functional Block Diagram . . . 12
1.6 Commands . . . 13

2 Functional Description . . . 14
2.1 Power-Up and Initialization . . . 14
2.2 Access To The Control Register Map . . . 15
2.3 Refresh Control Register . . . 16
2.3.1 Partial Array Self Refresh (PASR) . . . 17
2.3.2 Deep Power Down Mode . . . 18
2.3.3 Temperature Compensated Self Refresh (TCSR) . . . 18
2.3.4 Power Saving Potential in Standby When Applying PASR, TCSR or DPD . . . 18
2.3.5 Page Mode Enable/Disable . . . 19
2.4 Asynchronous Read . . . 20
2.4.1 Page Read Mode . . . 21
2.5 Asynchronous Write . . . 23
2.6 Deep Power Down Mode Entry/ Exit . . . 26
2.7 General AC Input/Output Reference Waveform . . . 26

3 Electrical Characteristics . . . 27
3.1 Absolute Maximum Ratings . . . 27
3.2 Recommended Power & DC Operation Ratings . . . 27
3.3 Output Test Conditions . . . 28
3.4 Pin Capacitances . . . 28

4 Package Outlines . . . 29

5 Appendix A: Low-Frequency Mode . . . 30
5.1 Asynchronous Access . . . 30

6 Appendix B: S/W Register Entry Mode (“4-cycle method”) . . . 31

Figure 1 CellularRAM - Interface Configuration Options. 9
Figure 2 Standard Ballout - HYE18P16161AC(-/L)70/85 10
Figure 3 Functional Block Diagram. 12
Figure 4 Power Up Sequence. 14
Figure 5 Refresh Control Registers 15
Figure 6 Control Register Write Access Protocol 15
Figure 7 PASR Programming Scheme 17
Figure 8 PASR Configuration Example. 18
Figure 9 Asynchronous Read - Address Controlled ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and/or $\overline{LB}$ = V_{IL}, ZZ = V_{IH}) 20
Figure 10 Asynchronous Read ($\overline{WE}$ = V_{IH}, ZZ = V_{IH}) 20
Figure 11 Asynchronous Page Read Mode (ZZ = V_{IH}) 21
Figure 12 Asynchronous Write - $\overline{WE}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, ZZ = V_{IH}). 23
Figure 13 Asynchronous Write - $\overline{CS1}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, ZZ = V_{IH}) 23
Figure 14 Asynchronous Write - $\overline{UB}$, $\overline{LB}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, ZZ = V_{IH}) 24
Figure 15 Asynchronous Write to Control Register ($\overline{OE}$ = V_{IH} or V_{IL}) 24
Figure 16 Deep Power Down Entry/ Exit 26
Figure 17 Output Test Circuit 28
Figure 18 P-VFBGA-48 (Plastic Very Thin Fine Pitch Ball Grid Array Package) 29
Figure 19 Low Frequency Mode 30
Figure 20 S/W Register Entry timing (Address input = FFFFFh) 31
Figure 21 RCR Mapping in S/W Register Entry 32

Table 1 Product Selection 8
Table 2 Ball Description - HYE18P16161AC(-/L)70/85 11
Table 3 Asynchronous Command Table 13
Table 4 Description of Commands 13
Table 5 Standby Currents When Applying PASR, TCSR or DPD 18
Table 6 Timing Parameters - Asynchronous Read 22
Table 7 Timing Parameters - Asynchronous Write 25
Table 8 DPD/ ZZ Timing Table 26
Table 9 Absolute Maximum Ratings 27
Table 10 Recommended DC Operating Conditions 27
Table 11 DC Characteristics 27
Table 13 Pin Capacitances 28
Table 12 Operating Characteristics 28

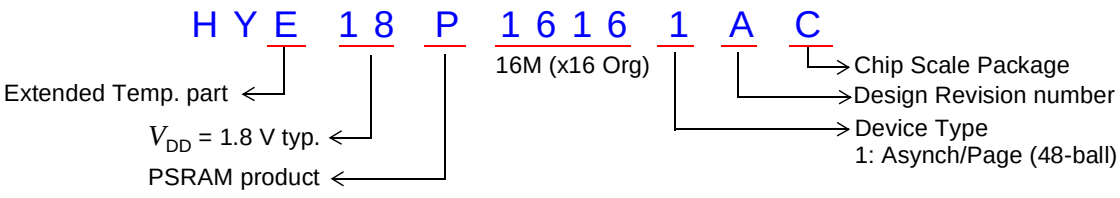
1 Overview

1.1 Features

- High density (1T1C-cell) Synchronous 16-Mbit Pseudo-Static RAM
- Designed for cell phone applications (CellularRAM)
- Functional-compatible to conventional low power asynchronous SRAM devices
- Organization 1M × 16
- Refresh-free operation
- 1.8 V single power supply (V_{DD} and V_{DDQ})
- Support of 2.5V and 3.0V I/O voltage options (V_{DDQ})
- Low power optimized design
  - $I_{STANDBY}$ = 70 µA for L-part and 100 µA for standard part (16M), data retention mode
  - I_{DPD} = < 25 µA (16M), non-data retention mode
- Low power features (partly adopted from the JEDEC standardized low power SDRAM specifications)
  - Temperature Compensated Self-Refresh (TCSR)
  - Partial Array Self-Refresh (PASR)
  - Deep Power Down Mode (DPD)
- 70 ns random access cycle time, 20 ns page mode (read only) cycle time
- Byte read/write control by $\overline{UB}$/$\overline{LB}$
- Wireless operating temperature range from -25 °C to +85 °C
- P-VFBGA-48 chip-scale package (8 × 6 ball grid)

Table 1 Product Selection

HYE18P16161AC	-70	-85	L70	L85
Min. Random Cycle time (tRC)	70ns	85ns	70ns	85ns
Min. Page Read Cycle time (tPC)	20ns	25ns	20ns	25ns
Operating current (Icc1)	20mA	17mA	20mA	17mA
Stand-by current (Icc2)	100uA		70uA	
Ordering Info			(Contact Factory)	



1.2 General Description

The 16M Asynchronous/Page CellularRAM (CellularRAM) is is the competitive alternative to today's SRAM based solutions in wireless applications, such as cellular phones. With its high density 1T1C-cell concept and highly optimized low power design, the CellularRAM is the advanced economic solution for the growing memory demand in baseband IC designs. SRAM-pin compatibility, refresh-free operation and extreme low power design makes a drop-in replacement in legacy systems an easy procedure.

Low power feature of Partial Array Self Refresh (PASR) allows the user to dynamically scale the active (=refreshed) memory to his needs and to adapt the refresh rate to the actual system environment. That is no power penalty is paid in case only portions of the total available memory capacity is used (e.g. 8Mb out of 16Mb).

The CellularRAM is available in two package options, in the SRAM compatible FBGA 48-ball package and with an enhanced feature set in a FBGA 54-ball package. For the advanced 54-ball device please refer to the corresponding data sheet (**HYE18P16160AC)**.

The CelllularRAM can be powered from a single 1.8V power supply feeding the core and the output drivers. Feeding the I/Os with a separate voltage supply the CelllularRAM can be easily adapted to systems operating in an I/O voltage range from 1.8V to 3.0V. The chip is fabricated in Infineon Technologies advanced 0.14µm low power process technology.

The configuration of interfacing CellularRAM is illustrated in **Figure 1**. Data byte control ($\overline{UB}$, $\overline{LB}$) is featured in all modes and provides dedicated lower and upper byte access.

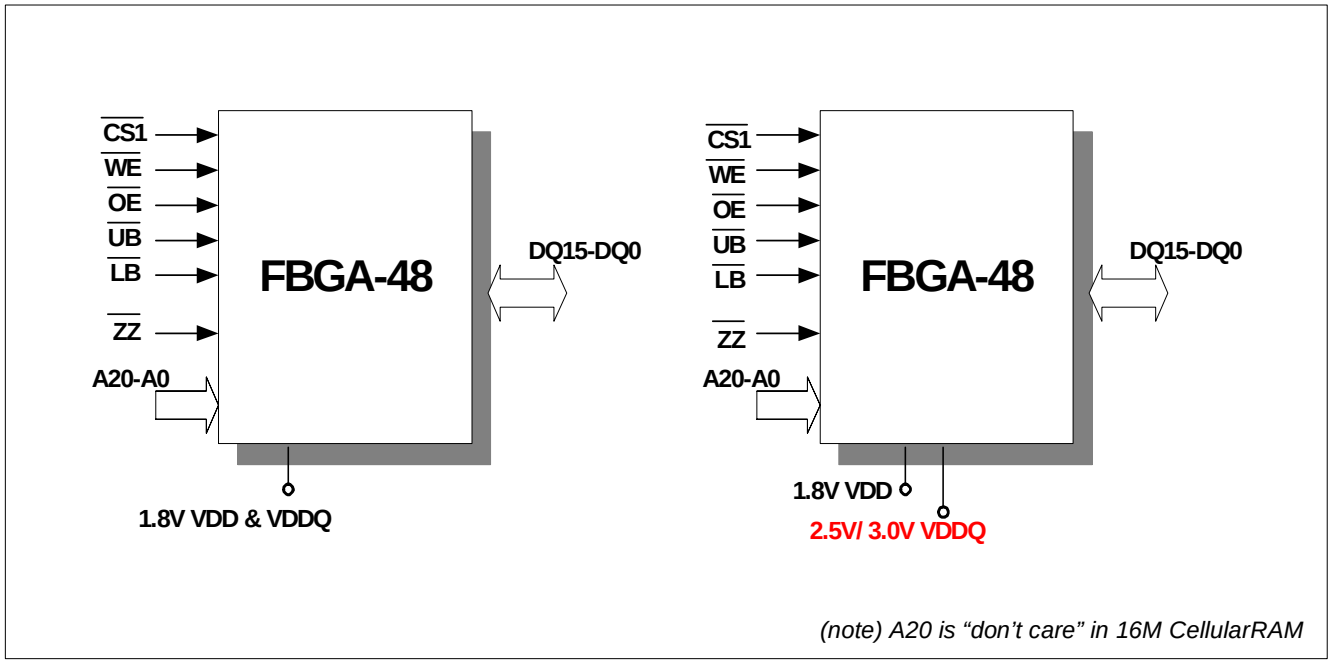


Figure 1 CellularRAM - Interface Configuration Options

The CellularRAM comes in a P-VFBGA-48 package.

1.3 HYE18P16161AC(-/L)70/85 Ball Configuration

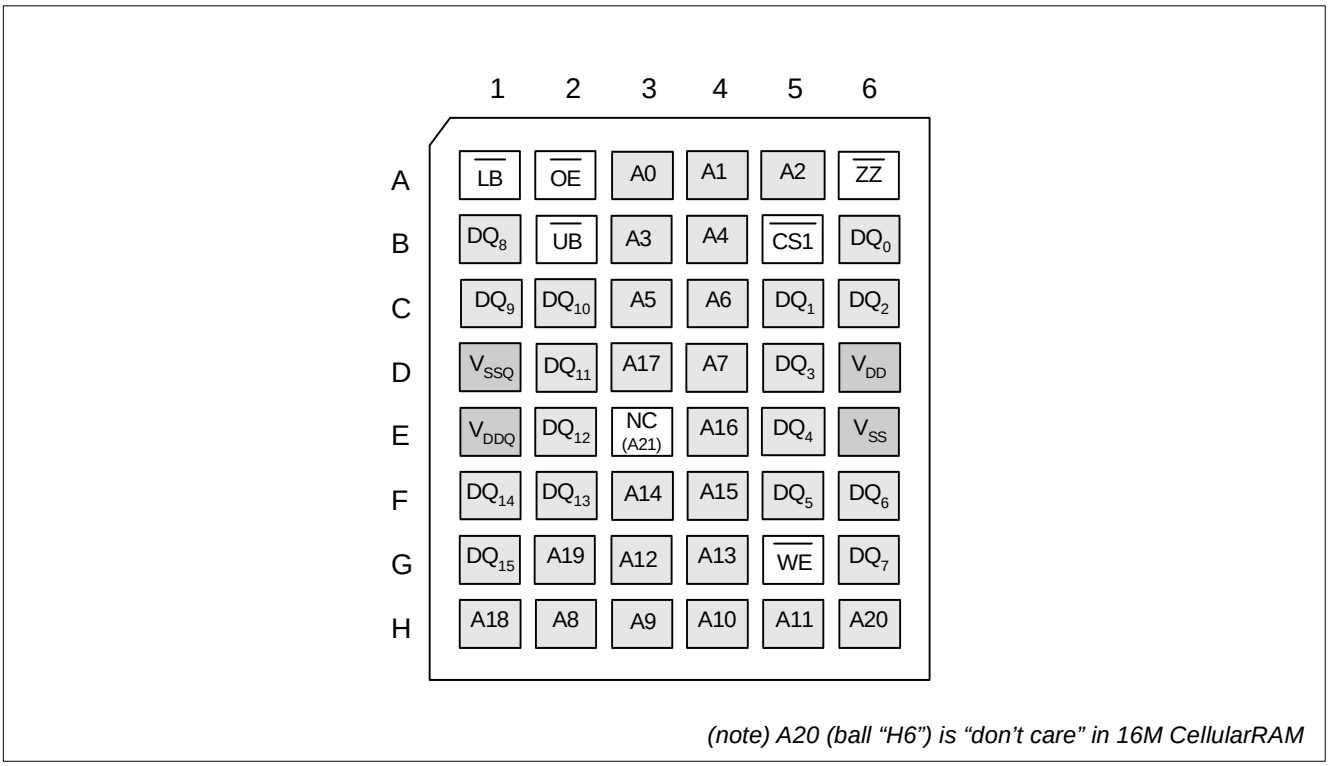


Figure 2 Standard Ballout - HYE18P16161AC(-/L)70/85

*Note: **Figure 2** shows top view*

1.4 HYE18P16161AC(-/L)70/85 Ball Definition and Description

Table 2 Ball Description - HYE18P16161AC(-/L)70/85

Ball	Type	Detailed Function
$\overline{CS1}$	Input	**Chip Select** $\overline{CS1}$ enables the command decoder when low and disables it when high. When the command decoder is disabled new commands are ignored, addresses are don't care and outputs are forced to high-Z. Internal operations, however, continue. For the details please refer to the command tables in **Chapter 1.6**.
$\overline{OE}$	Input	**Output Enable** $\overline{OE}$ controls DQ output driver. $\overline{OE}$ low drives DQ, $\overline{OE}$ high sets DQ to high-Z.
$\overline{WE}$	Input	**Write Enable** $\overline{WE}$ set to low while $\overline{CS}$ is low initiates a write command.
$\overline{UB}$, $\overline{LB}$	Input	**Upper/Lower Byte Enable** $\overline{UB}$ enables the upper byte DQ15-8 (resp. $\overline{LB}$ DQ7 … 0) during read/write operations. $\overline{UB}$ ($\overline{LB}$) deassertion prevents the upper (lower) byte from being driven during read or being written.
$\overline{ZZ}$	Input	**Deep Power Down Enable/ Set Control Register** Strapping $\overline{ZZ}$ to low for more than 10µs the device is put to deep power down mode. If a write access is initiated instantly (<500ns) after $\overline{ZZ}$ has been asserted to low access to the refresh configuration register is given. By applying the SET CONTROL REGISTER (SCR) command (see **Table 3**) the address bus is then loaded into the refresh control register.
A <19:0>	Input	**Address Inputs** During a Control Register Set operation, the address inputs define the register settings.
DQ <15:0>	I/O	**Data Input/Output** The DQ signals $\overline{0}$ to $\overline{15}$ form the 16-bit data bus.
$1 \times V_{DD}$ $1 \times V_{SS}$	Power Supply	**Power Supply, Core** Power and Ground for the internal logic.
$1 \times V_{DDQ}$ $1 \times V_{SSQ}$	Power Supply	**Power Supply, I/O Buffer** Isolated Power and Ground for the output buffers to provide improved noise immunity.
2 × NC	–	**No Connect** Please do not connect. Reserved for future use, i.e. H6: A20, E3: A21, see ballout in **Figure 2** on **Page 10**.

1.5 Functional Block Diagram

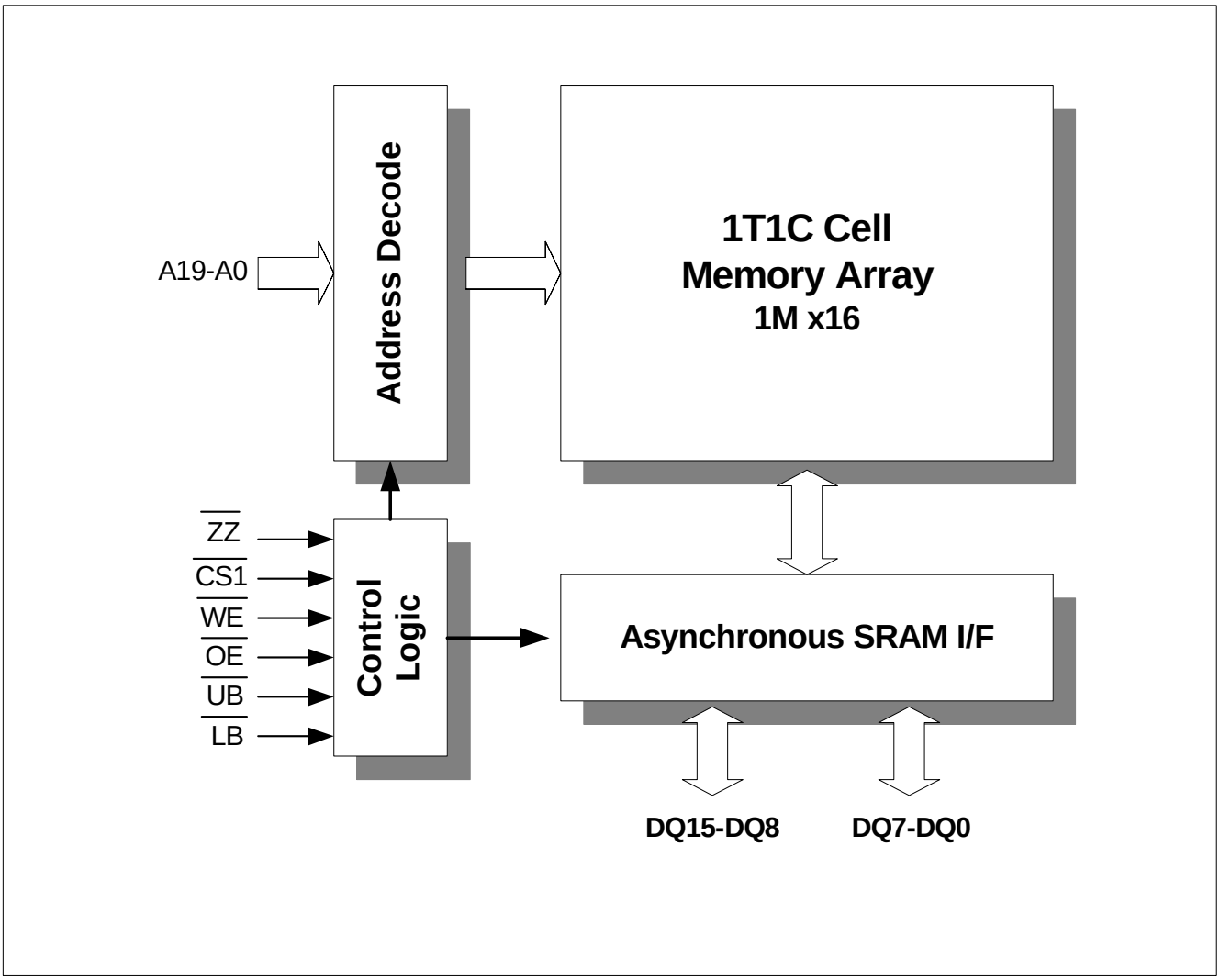


Figure 3 Functional Block Diagram

1.6 Commands

All commands are of asynchronous nature. The supported control signal combinations are listed in the table below.

c

Table 3 Asynchronous Command Table

Operation Mode	Power Mode	$\overline{CS1}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$/$\overline{LB}$	$\overline{ZZ}$	A19	A18 - A0	DQ15:0
READ	Active	L	H	L	L[1)]	H	V	ADR	DOUT
WRITE	Active	L	L	X[2)]	L[1)]	H	V	ADR	DIN
SET CONTROL REGISTER	Active	L	L	X[2)]	X	L	L	RCR DIN	X
NO OPERATION	Standby~Active[3)]	L	H	H	X	H	X	X	High-Z
DESELECT	Standby	H	X	X	X	X	X	X	High-Z
DPD	Deep Power Down	H	X	X	X	L	X	X	High-Z

1) **Table 3** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0).

2) During a write access invoked by $\overline{WE}$ set to low the $\overline{OE}$ signal is ignored.

3) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. Toggling address results in active power mode. Also, NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 4 Description of Commands

Mode	Description
READ	The READ command is used to perform an asynchronous read cycle. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is output.
WRITE	The WRITE command is used to perform an asynchronous write cycle. The data is latched on the rising edge of either $\overline{CS}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, whichever comes first. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is latched into the CellularRAM.
SET CONTROL REGISTER	The control registers are loaded via the address inputs A15 - A0 performing an asynchronous write access. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS1}$ = 0). Operations already in progress are not affected. Power consumption of this command mode varies by address change and initiating condition.
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 µA. Wake-up from DPD also requires 150 µs to get ready for normal operation.

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

2 Functional Description

2.1 Power-Up and Initialization

The power-up and initialization sequence guarantees that the device is preconditioned to the user's specific needs. Like conventional DRAMs, the CellularRAM must be powered up and initialized in a predefined manner. V_{DD} and V_{DDQ} must be applied at the same time to the specified voltage while the input signals are held in "DESELECT" state ($\overline{CS1}$ = High).

After power on, an initial pause of 150 µs is required prior to the control register access or normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

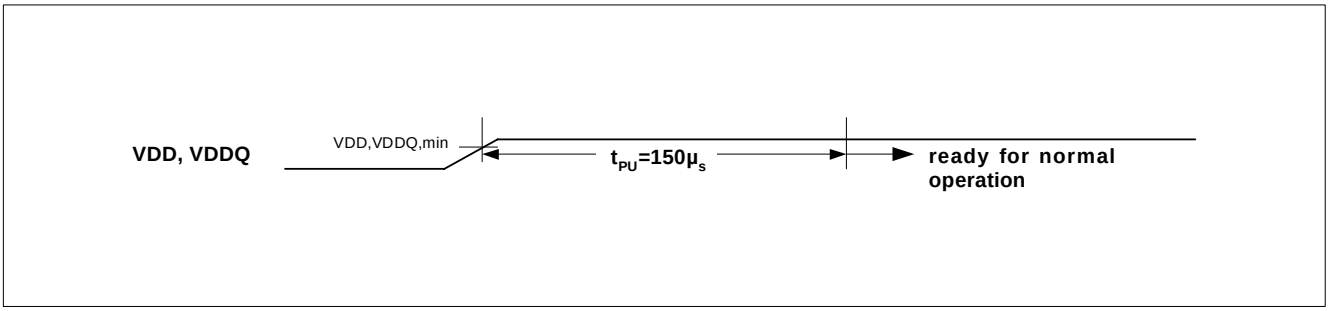


Figure 4 Power Up Sequence

2.2 Access To The Control Register Map

[Disclaimer]
A20 input shown in timing diagrams is not used in 16Mbit CellularRAM. Should be “don’t care”.

Write-only access to the refresh control register is enabled by applying the SCR command and asserting the $\overline{ZZ}$-pin to low. **Figure 5** shows the mapping of the address bus lines to the the refresh control register bits, whereas in Figure 6 the access timing is illustrated.

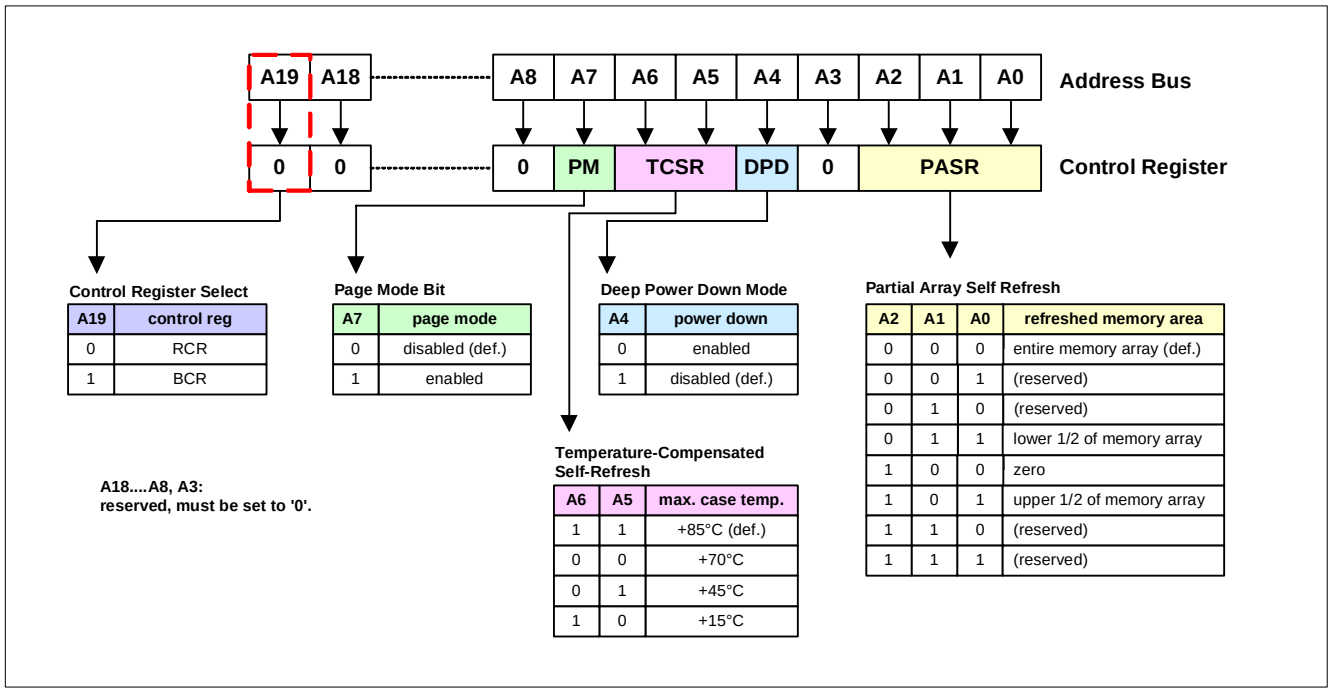


Figure 5 Refresh Control Registers

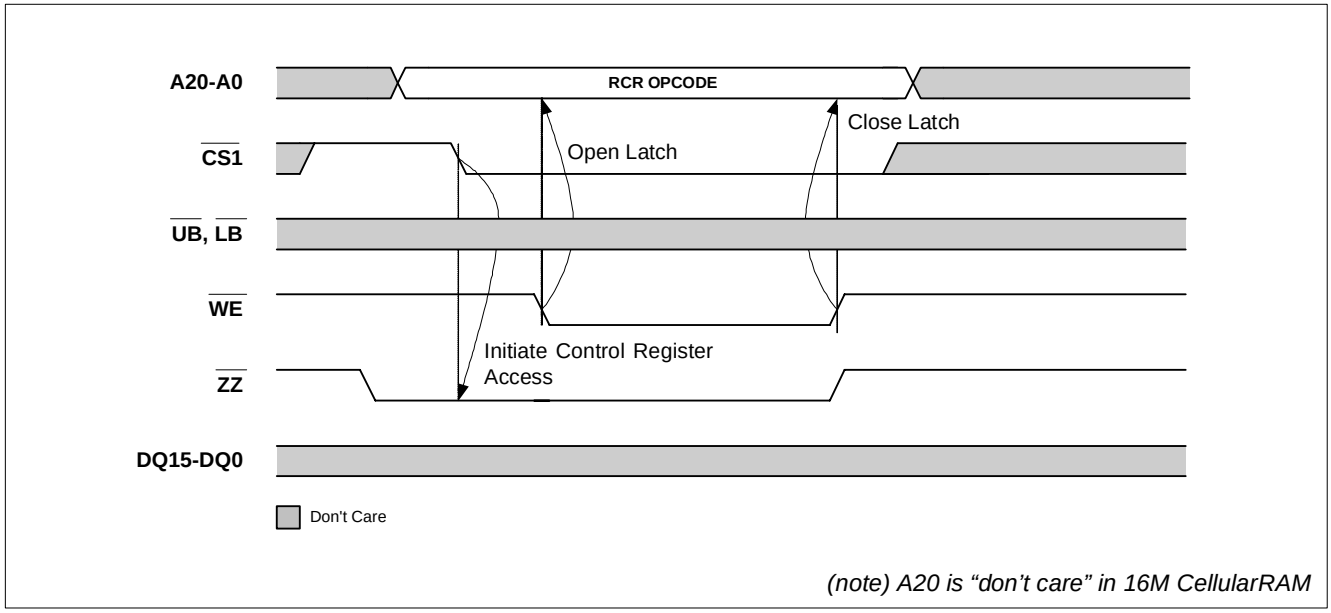


Figure 6 Control Register Write Access Protocol

2.3 Refresh Control Register

The Refresh Control Register (RCR) allows to save stand-by power additionally by making use of the Temperature-Compensated Self Refresh (TCSR), Partial-Array Self Refresh (PASR) and Deep Power Down (DPD) features. The Refresh Control Register is programmed via the Control Register Set command and retains the stored information until it is reprogrammed or the device loses power.

Please note that the RCR contents can only be set or changed when the CellularRAM is in idle state.

RCR
Refresh Control Register **($\overline{ZZ}$, A19 = 00_B)**

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RS	**0**											**PM**	**TCSR**		**DPD**	**0**	**PASR**		

Field	Bits	Type[1)]	Description
RS	19	w	**Register Select** 0 set to 0 to select this RCR.
PM	7	w	**Page Mode Enable/Disable** In asynchronous operation mode the user has the option to toggle A0 - A3 in a random way at higher rate (20 ns vs. 70 ns) to lower access times of subsequent reads with 16-word boundary. In synchronous mode this option has no effect. The max. page length is 16 words. Please note that as soon as page mode is enabled the $\overline{CS1}$ low time restriction applies. This means that the $\overline{CS1}$ signal must not be kept low longer than t_{CSL} = 10 µs. Please refer to **Figure 11**. 0 page mode disabled (default) 1 page mode enabled
TCSR	[6:5]	w	**Temperature Compensated Self Refresh** The 2-bit wide TCSR field features four different temperature ranges to adjust the refresh period to the actual case temperature. Since DRAM technology requires higher refresh rates at higher temperature this is a second method to lower power consumption in case of low or medium temperatures. 11 +85 °C (default) 00 +70 °C 01 +45 °C 10 +15 °C
DPD	4	w	**Deep Power Down Enable/Disable** The DPD control bit puts the CellularRAM device in an extreme low power mode cutting current consumption to less than 25 µA. Stored memory data is not retained in this mode, while the settings of control register, RCR is stored during DPD. 0 DPD enabled 1 DPD disabled (default)

Field	Bits	Type[1)]	Description
PASR	[2:0]	w	**Partial Array Self Refresh** The 3-bit PASR field is used to specify the active memory array. The active memory array will be kept periodically refreshed whereas the disabled parts will be excluded from refresh and previously stored data will get lost. The normal operation still can be executed in disabled array, but stored data is not guaranteed. This way the customer can dynamically adapt the memory capacity in steps of 8 Mbit to one's need without paying a power penalty. Please refer to **Figure 7**. 000 entire memory array (default) 011 lower 1/2 of the memory array (8 Mb) 100 zero 101 upper 1/2 of the memory array (8 Mb) All others; reserved (16Mb)
Res	[18:8], 3	w	**Reserved** must be set to '0'

1) w: write-only access

2.3.1 Partial Array Self Refresh (PASR)

By applying PASR the user can dynamically customize the memory capacity to one's actual needs in normal operation mode and standby mode. With the activation of PASR there is no longer a power penalty paid for the larger CellularRAM memory capacity in case only e.g. 8 Mbits are used by the host system.

Bit2 down to bit0 specify the active memory array and its location (starting from bottom or top). The memory parts not used are powered down immediately after the mode register has been programmed. Advice for the proper register setting including the address ranges is given in **Figure 7**.

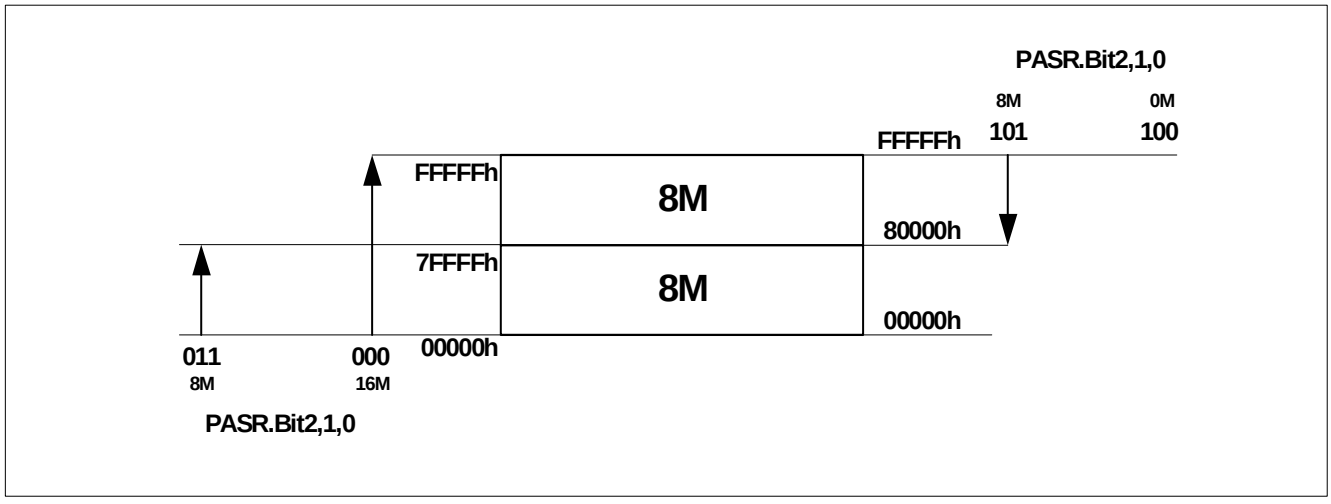


Figure 7 PASR Programming Scheme

PASR is activated, i.e. the memory parts not used are powered down, after $\overline{ZZ}$ has been held low for more than 10µs. In PASR state no READ or WRITE commands are recognized. To resume WRITE or READ operations, the device must exit PASR by taking $\overline{ZZ}$ to high level voltage again.

Pre-condition to enter PASR on $\overline{ZZ}$ low is that the Deep Power Down mode has been disabled before via RCR.Bit4= 1.

Figure 8 shows an exemplary PASR configuration where it is assumed that the application uses max. 8 Mbit out of 16 Mbit.

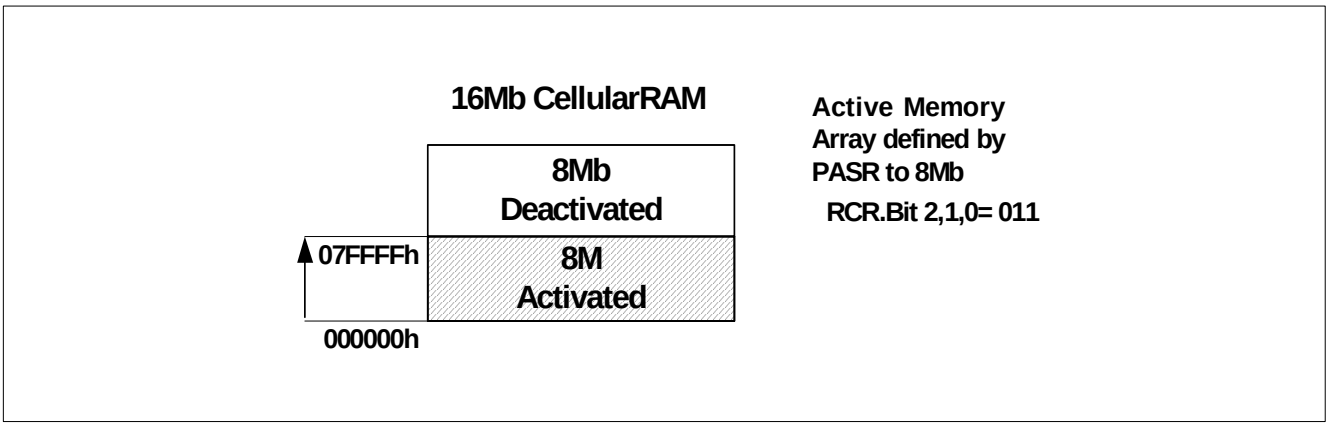


Figure 8 PASR Configuration Example

2.3.2 Deep Power Down Mode

To put the device in deep power down mode, it is required to comply with 2-steps. At first, the DPD mode bit must be set to be enabled in the Refresh Configuration Register. When DPD entry is really required, $\overline{ZZ}$ pin must be asserted to low for longer than 10µs. Between these 2 steps, any normal operations are permitted. Once the device enters into this extreme low power mode, current consumption is cut down to less than 25µA.

All internal voltage generators inside the CelllularRAM are switched off and the internal self-refresh is stopped. This means that all stored information will be lost in any time. The device will remain in DPD mode as long as $\overline{ZZ}$ is held low.To exit the Deep Power Down mode, it is needed to simply bring $\overline{ZZ}$ to high voltage level. A guard time of at least 150µs has to be met where no commands beside DESELECT must be applied to re-enter standby or idle mode. (see **Figure 16**).

2.3.3 Temperature Compensated Self Refresh (TCSR)

The 2-bit wide TCSR field features four different temperature ranges to adjust the refresh period to the actual case temperature. DRAM technology requires higher refresh rates at higher temperature. At low temperature the refresh rate can be reduced, which reduces as well the standby current of the chip. This feature can be used in addition to PAR to lower power consumption in case of low or medium temperatures. Please refer to **Table 5**.

2.3.4 Power Saving Potential in Standby When Applying PASR, TCSR or DPD

Table 5 demonstrates the currents in standby mode when PASR, TCSR or DPD is applied.

Table 5 Standby Currents When Applying PASR, TCSR or DPD

Operation Mode	Power Mode	PASR	Bit Controlled	Wake-Up Phase	Active Array	Standby [µA]			
NO OPERATION/ DESELECT	STANDBY	TCSR	RCR.Bit6-5	–	–	85°	70°	45°	15°
		PASR	RCR.Bit2-0	–	Full 1/2 0	70(100) 60(80) 50(60)	65(90) 60(75) 50(60)	55(70) 53(65) 50(60)	50(60) 50(60) 50(60)
DPD	DEEP POWER DOWN	DPD	RCR.Bit4	~150 µs	0	25.0			

2.3.5 Page Mode Enable/Disable

In asynchronous operation mode, the user has the option to enable page mode to toggle A0 - A3 in random way at higher cycle rate (20 ns vs. 70 ns) to lower access times of subsequent reads within 16-word boundary. Write operation is not supported in the manner of page mode access. In synchronous mode, this option has no effect. The max. page length is 16 words, so which A0 - A3 is regarded as page-mode address. If the access needs to cross the boundary of 16-word (any difference in A18 - A4), then it should start over new random access cycle, which is the same as asynchronous read operation.

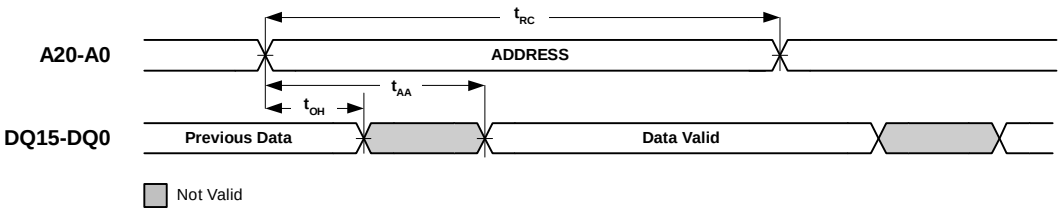
Please note that as soon as page mode is enabled the $\overline{CS1}$ low time restriction applies. This means that the $\overline{CS1}$ signal must not kept low longer than t_{CSL} = 10 µs. Please refer to **Figure 11**.

2.4 Asynchronous Read

[Disclaimer]
A20 input shown in timing diagrams is not used in 16Mbit CellularRAM. Should be “don’t care”.

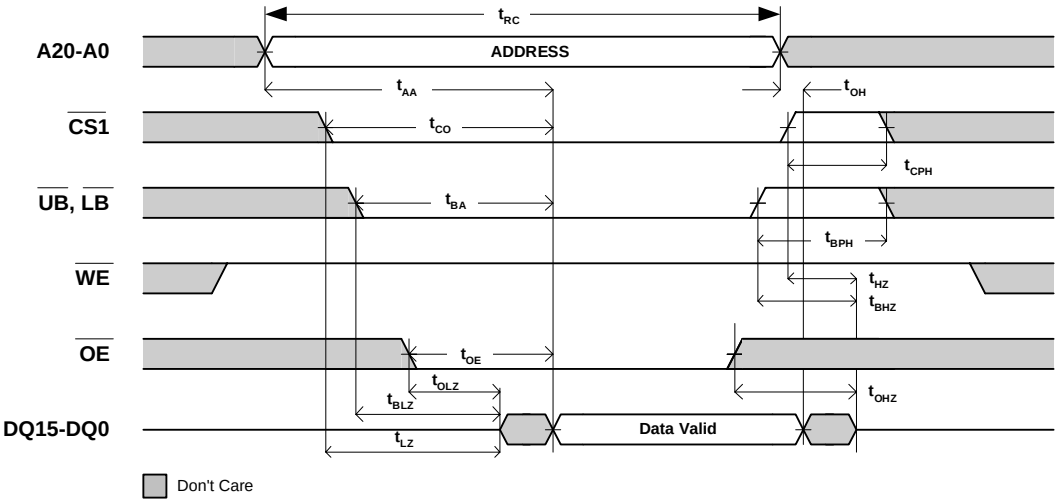
The CellularRAM applies the standard asynchronous SRAM protocol to perform read and write accesses.

Reading from the device in asynchronous mode is accomplished by asserting the Chip Select ($\overline{CS1}$) and Output Enable ($\overline{OE}$) signals to low while forcing Write Enable ($\overline{WE}$) to high. If the Upper Byte ($\overline{UB}$) control line is set active low then the upper word of the addressed data is driven on the output lines, DQ15 to DQ8. If the Lower Byte ($\overline{LB}$) control line is set active low then the lower word of the addressed data is driven on the output lines, DQ7 to DQ0.



(note) A20 is “don’t care” in 16M CellularRAM

Figure 9 Asynchronous Read - Address Controlled ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, $\overline{UB}$ and/or $\overline{LB}$ = V_{IL}, $\overline{ZZ}$ = V_{IH})



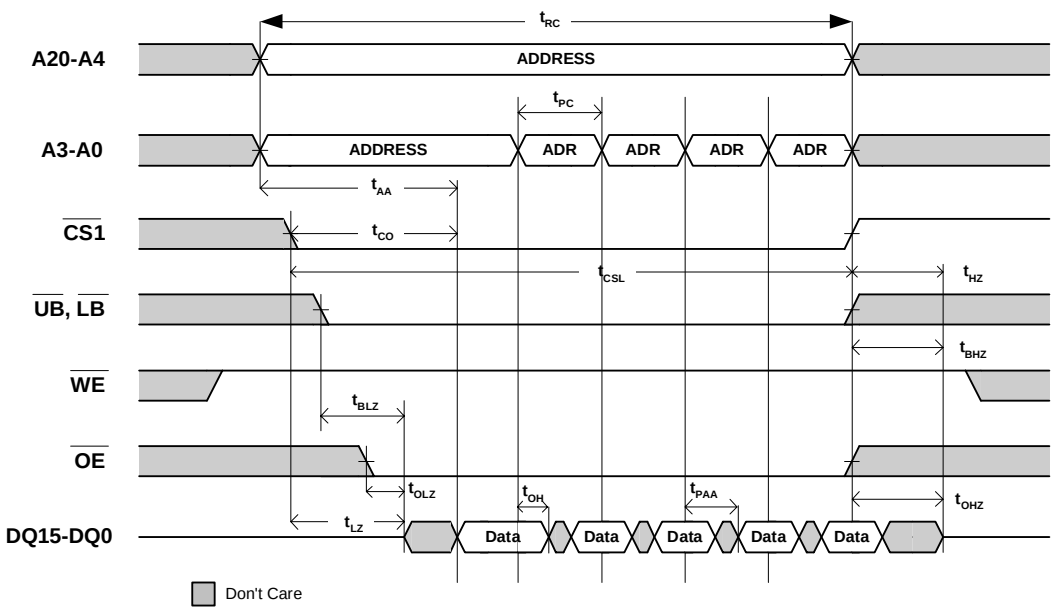
(note) A20 is “don’t care” in 16M CellularRAM

Figure 10 Asynchronous Read ($\overline{WE}$ = V_{IH}, $\overline{ZZ}$ = V_{IH})

2.4.1 Page Read Mode

If activated by RCR.Bit7 page mode allows to toggle the four lower address bits (A3 to A0) to perform subsequent random read accesses (max. 16-words by A3 - A0) at much faster speed than 1st read access. Page mode operation supports only read access in CellularRAM. As soon as page mode is activated, $\overline{CS1}$ low time restriction (t_{CSL}) applies. In case of $\overline{CS1}$ staying low longer than t_{CSL} limit, then it is alternative way to toggle non-page address (A18 - A4) no later than $t_{CSL,max}$. Therefore the usage of page mode is only recommended in systems which can respect this limitation.

Please see also application note on **Page 30**.



(note) A20 is "don't care" in 16M CellularRAM

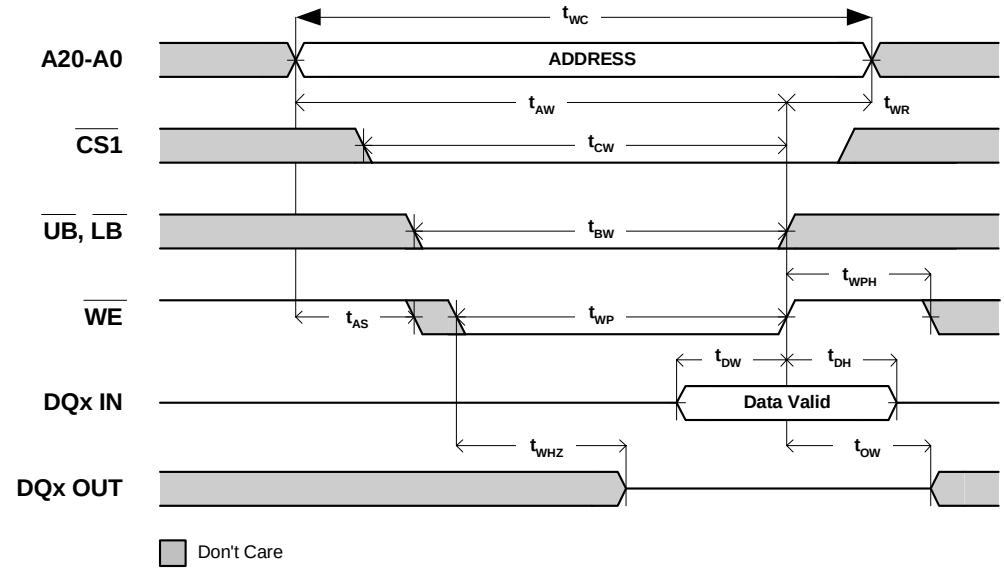
Figure 11 Asynchronous Page Read Mode ($\overline{ZZ}$ = V_{IH})

Table 6 Timing Parameters - Asynchronous Read

Parameter	Symbol	70		85		Unit	Notes
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	70	–	85	–	ns	–
Address access time	t_{AA}	–	70	–	85	ns	–
Page address cycle time	t_{PC}	20	–	25	–	ns	–
Page address access time	t_{PAA}	–	20	–	25	ns	–
Output hold from address change	t_{OH}	5	–	6	–	ns	–
Chip select access time	t_{CO}	–	70	–	85	ns	–
$\overline{UB}$, $\overline{LB}$ access time	t_{BA}	–	70	–	85	ns	–
$\overline{OE}$ to valid output data	t_{OE}	–	20	–	25	ns	–
Chip select pulse width low time	t_{CSL}	–	10	–	10	µs	–
Chip select to output active	t_{LZ}	6	–	6	–	ns	–
Chip select disable to high-Z output	t_{HZ}	–	8	–	8	ns	–
$\overline{UB}$, $\overline{LB}$ enable to output active	t_{BLZ}	6	–	6	–	ns	–
$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	–	8	–	8	ns	–
Output enable to output active	t_{OLZ}	3	–	3	–	ns	–
Output disable to high-Z output	t_{OHZ}	–	6	–	8	ns	–
$\overline{CS1}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–

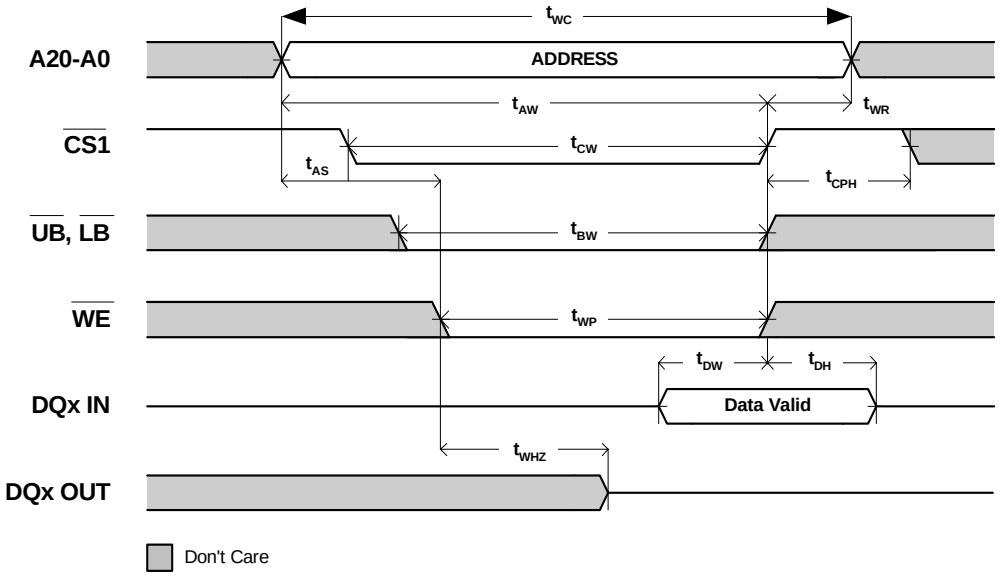
2.5 Asynchronous Write

Writing to the device in asynchronous mode is accomplished by asserting the Chip Select ($\overline{CS1}$) and Write Enable ($\overline{WE}$) signals to low. If the Upper Byte ($\overline{UB}$) control line is set active low then the upper word (DQ15 to DQ8) of the data bus is written to the specified memory location. If the Lower Byte ($\overline{LB}$) control line is set active low then the lower word (DQ7 to DQ0) of the data bus is written to the specified memory location. Write operation takes place when either one or both $\overline{UB}$ and $\overline{LB}$ is asserted low. The data is latched by the rising edge of either $\overline{CS1}$, $\overline{WE}$, or $\overline{UB}$/$\overline{LB}$ whichever signal comes first.



(note) A20 is "don't care" in 16M CellularRAM

Figure 12 Asynchronous Write - $\overline{WE}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, $\overline{ZZ}$ = V_{IH})



(note) A20 is "don't care" in 16M CellularRAM

Figure 13 Asynchronous Write - $\overline{CS1}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, $\overline{ZZ}$ = V_{IH})

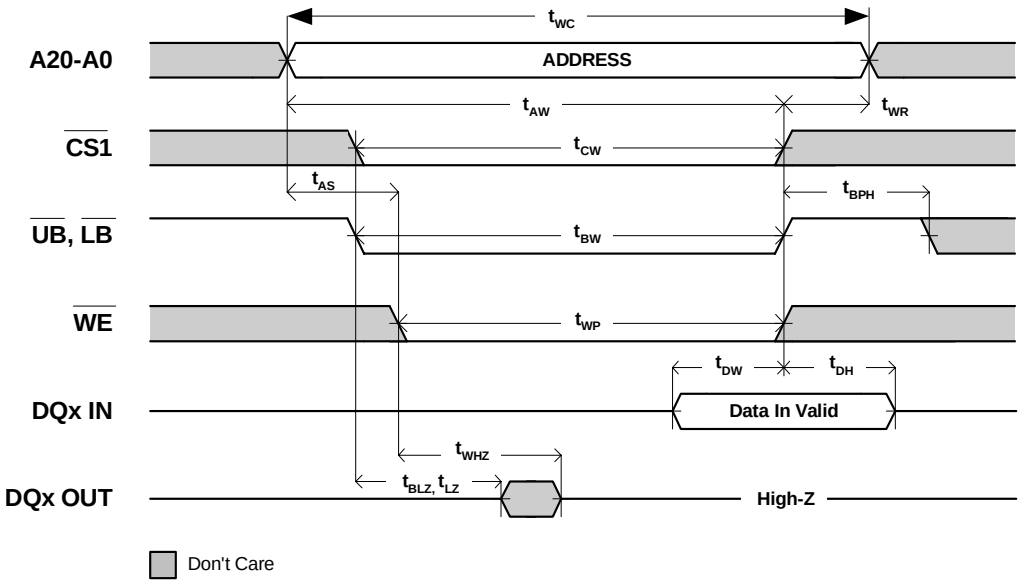


Figure 14 Asynchronous Write - $\overline{UB}$, $\overline{LB}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, $\overline{ZZ}$ = V_{IH})

The programming of control register in asynchronous mode is performed in the similar manner as asynchronous write except $\overline{ZZ}$ being held low during the operation. Note that $\overline{ZZ}$ has to meet set-up time (t_{ZZWE}) and hold time (t_{WEZZ})of valid state (= Low) in reference to $\overline{WE}$ falling and rising edge, respectively. $\overline{CS1}$ should toggle at the end of the operation to get ready for following access.

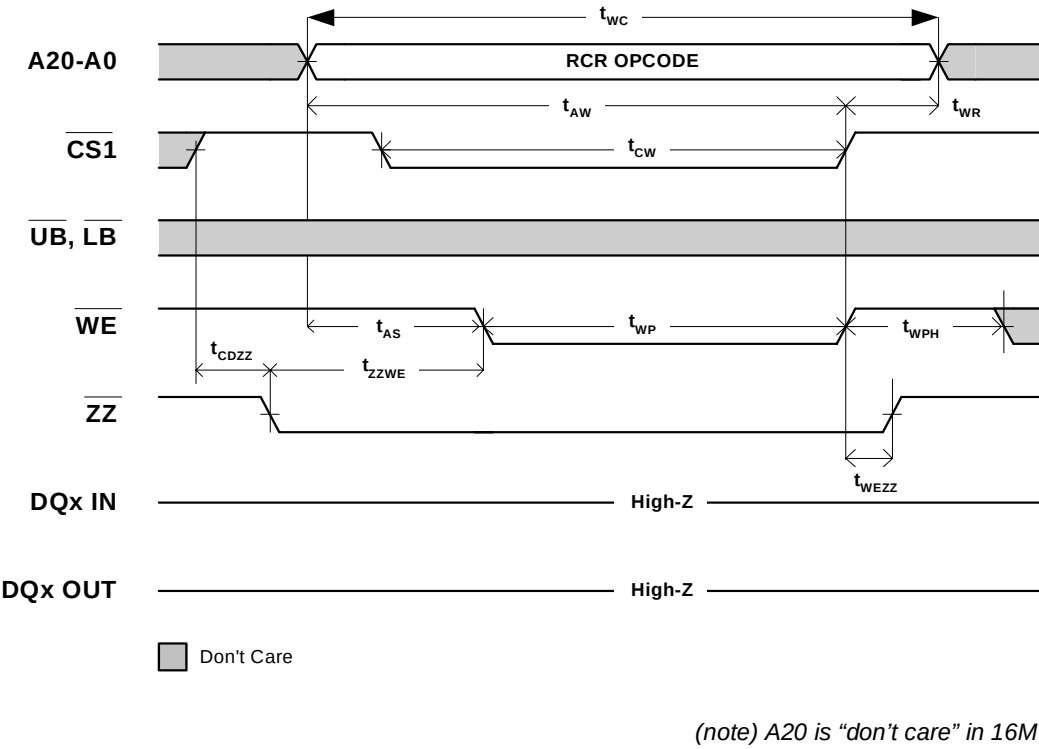


Figure 15 Asynchronous Write to Control Register ($\overline{OE}$ = V_{IH} or V_{IL})

Table 7 Timing Parameters - Asynchronous Write

Parameter	Symbol	70		85		Unit	Notes
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	70	–	85	–	ns	–
Address set-up time to start of write	t_{AS}	0	–	0	–	ns	–
Address valid to end of write	t_{AW}	70	–	85	–	ns	–
Write recovery time	t_{WR}	0	–	0	–	ns	–
Chip select pulse width low time	t_{CSL}	–	10	–	10	µs	–
Chip select to end of write	t_{CW}	70	–	85	–	ns	–
Byte control valid to end of write	t_{BW}	70	–	85	–	ns	–
Write pulse width	t_{WP}	40	–	45	–	ns	–
Write pulse pause	t_{WPH}	10	–	15	–	ns	–
$\overline{CS}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–
Write to output disable	t_{WHZ}	–	8	–	10	ns	–
End of write to output enable	t_{OW}	3	–	3	–	ns	–
Write data setup time	t_{DW}	20	–	20	–	ns	–
Write data hold time	t_{DH}	0	–	0	–	ns	–
$\overline{CS1}$ high setup time to $\overline{ZZ}$ low	t_{CDZZ}	5	–	5	–	ns	–
$\overline{ZZ}$ active setup time to start of write	t_{ZZWE}	10	500	10	500	ns	–
$\overline{ZZ}$ active hold time from end of write	t_{WEZZ}	0	–	0	–	ns	–

2.6 Deep Power Down Mode Entry/ Exit

To put the device in deep power down mode, it is required to comply with 2-step operation. At first, the DPD mode bit (RCR.bit4) has be programmed to be enabled in the Refresh Configuration Register through SCR command. When DPD entry is really required, $\overline{ZZ}$ pin must be asserted to low for longer than 10µs while $\overline{CS1}$ sets to high as shown in Figure 15. Between these 2 steps, any normal operations are permitted. Once the device enters into this extreme low power mode, current consumption is cut down to less than 25µA.

Please note that 2 step operation for DPD entry is not designed to take place at a time when $\overline{ZZ}$ is held low. In case of back-to-back operation to perform 2 steps, it is required to meet $\overline{ZZ}$ precharge time (t_{ZPH}).

All internal voltage generators inside the CelllularRAM are switched off and the internal self-refresh is stopped. This means that all stored information will be lost in any time. The device will remain in DPD mode as long as $\overline{ZZ}$ is held low. To exit the Deep Power Down mode, it is needed to simply bring $\overline{ZZ}$ to high voltage level. A guard time of at least 150µs (t_R) has to be met where no commands beside DESELECT must be applied to re-enter standby or idle mode.

Figure 16 Deep Power Down Entry/ Exit

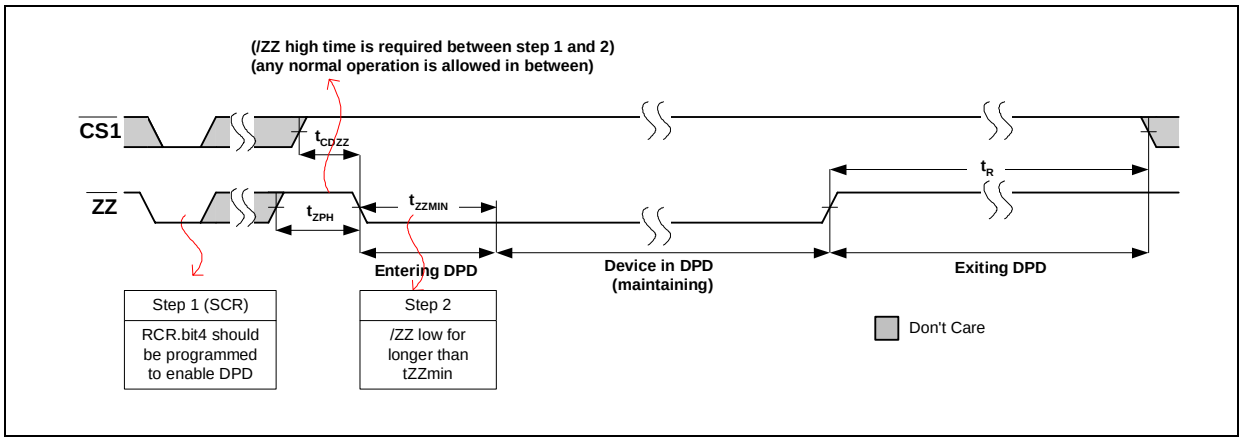


Table 8 DPD/ ZZ Timing Table

Parameter	Symbol	70 & 85		Unit	Notes
		Min.	Max.		
$\overline{CS1}$ high setup time to $\overline{ZZ}$ low	t_{CDZZ}	5	–	ns	–
$\overline{ZZ}$ precharge time	t_{ZPH}	5	–	ns	–
$\overline{ZZ}$ active for DPD entry	t_{ZZMIN}	10	–	µs	–
Recovery time from DPD exit	t_R	150	–	µs	–

2.7 General AC Input/Output Reference Waveform

The input timings refer to a midlevel of $V_{DDQ}/2$ while as output timings refer to midlevel $V_{DDQ}/2$. The rising and falling edges are 10 - 90% and < 2 ns.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operating temperature range	T_C	-25	+85	°C	–
Storage temperature range	T_{STG}	-55	+150	°C	–
Soldering peak temperature (10 s)	T_{Sold}	–	260	°C	–
Voltage of V_{DD} supply relative to V_{SS}	V_{DD}	-0.3	+2.45	V	–
Voltage of V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.3	+3.6	V	–
Voltage of any input relative to V_{SS}	V_{IN}	-0.3	+3.6	V	–
Power dissipation	P_D	–	180	mW	–
Short circuit output current	I_{OUT}	-50	+50	mA	–

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Recommended Power & DC Operation Ratings

All values are recommended operating conditions unless otherwise noted.

Table 10 Recommended DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Power supply voltage, core	V_{DD}	1.7	1.8	1.95	V	–
Power supply voltage, 1.8 V I/Os	V_{DDQ}	1.7	1.8	2.25	V	–
Power supply voltage, 2.5 V I/Os	V_{DDQ}	2.3	2.5	2.7	V	–
Power supply voltage, 3.0 V I/Os	V_{DDQ}	2.7	3.0	3.3	V	–
Input high voltage	V_{IH}	V_{DDQ} – 0.4	–	V_{DDQ} + 0.2	V	–
Input low voltage	V_{IL}	-0.2	–	0.4	V	–

Table 11 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Output high voltage (I_{OH} = -0.2 mA)	V_{OH}	$V_{DDQ} \times 0.8$	–	–	V	–
Output low voltage (I_{OL} = 0.2 mA)	V_{OL}	–	–	$V_{DDQ} \times 0.2$	V	–
Input leakage current	I_{LI}	–	–	1	µA	–
Output leakage current	I_{LO}	–	–	1	µA	–

Table 12 Operating Characteristics

Parameter	Symbol	70		85		Unit	Test Condition	Notes
		Min.	Max.	Min.	Max.			
Operating Current						mA	$V_{in} = V_{DD}$ or V_{SS}, Chip enabled, $I_{out} = 0$	1)
• Async read/write random @t_{RCmin}	I_{DD1}	–	20	–	17			
• Async read/write random @t_{RC} = 1 µs	I_{DD1L}	–	5	–	5			
• Async Page read	I_{DD1P}	–	15	–	12			
Stand-By Current : L-part (16M)	I_{DD2}	–	70	–	70	µA	$V_{in} = V_{DD}$ or V_{SS}, Chip deselected, (Full array)	–
Stand-By Current : Std. part (16M)		–	100	–	100	µA		
Deep Power Down Current (16M)	I_{DD3}	–	25	–	25	µA	$V_{in} = V_{DD}$ or V_{SS}	–

1) The specification assumes the output disabled.

3.3 Output Test Conditions

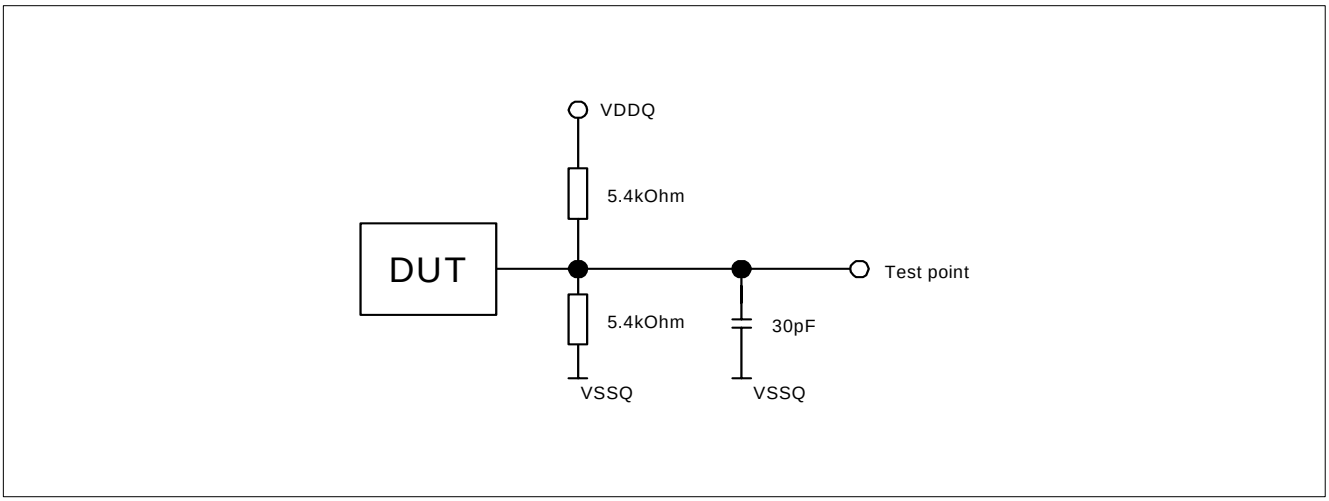


Figure 17 Output Test Circuit

Please refer to section **Section 2.7**.

3.4 Pin Capacitances

Table 13 Pin Capacitances

Pin	Limit Values		Unit	Condition
	Min.	Max.		
A19 - A0, $\overline{CS1}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, $\overline{ZZ}$	–	5.0	pF	T_A = +25 °C, freq. = 1 MHz, V_{pin} = 0 V, (sampled, not 100% tested)
DQ15 - DQ0	–	6.0	pF	

4 Package Outlines

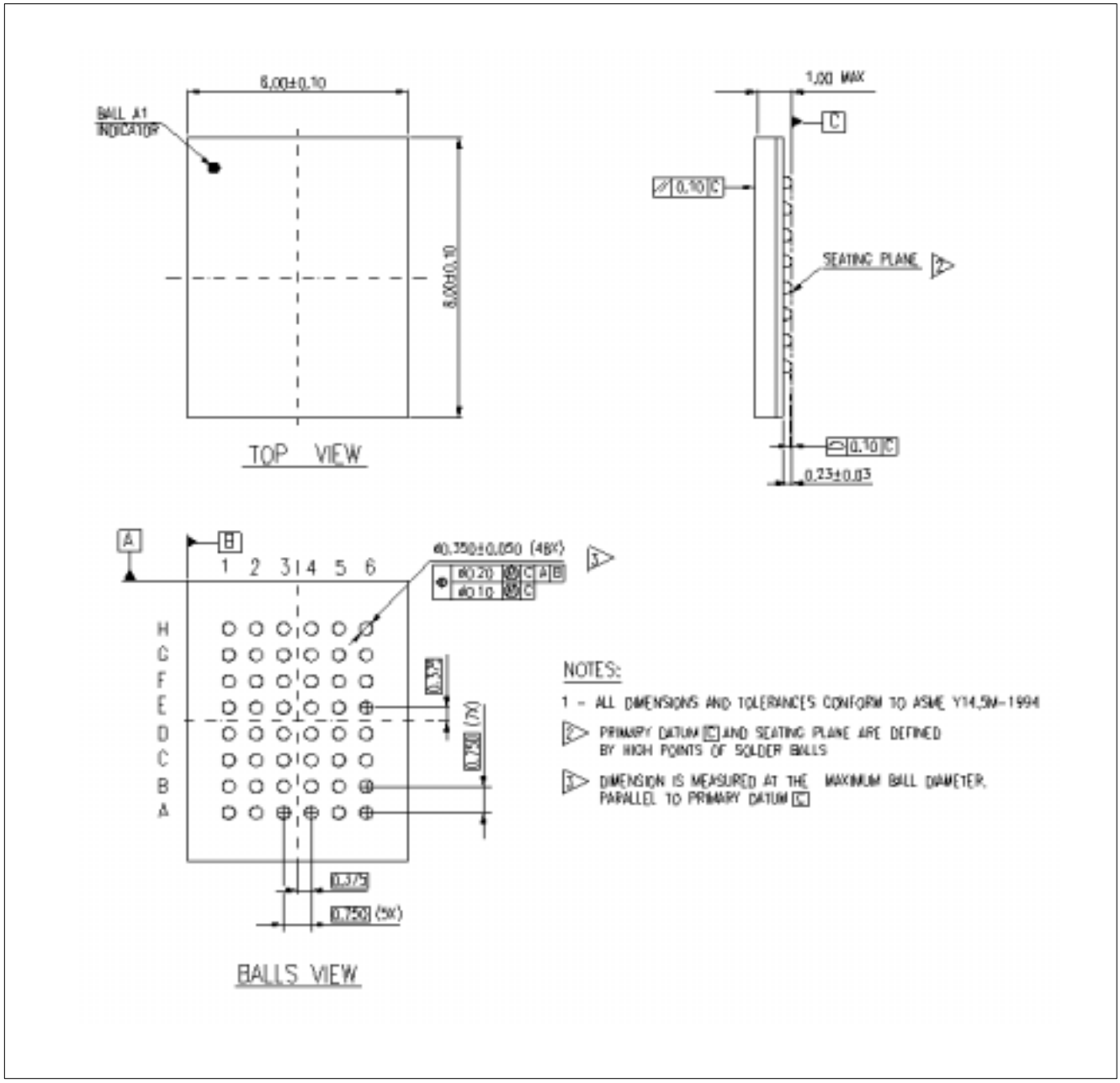


Figure 18 P-VFBGA-48 (Plastic Very Thin Fine Pitch Ball Grid Array Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

5 Appendix A: Low-Frequency Mode

5.1 Asynchronous Access

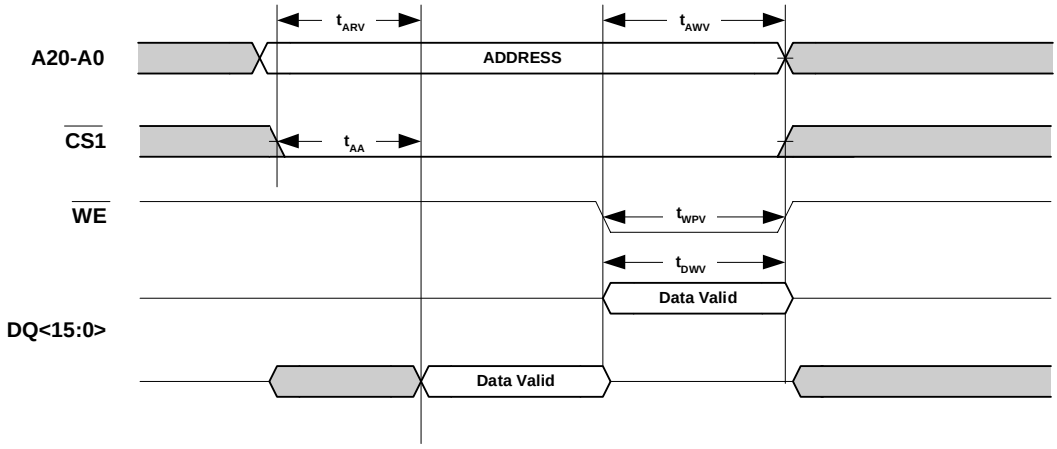
Depending on the random access frequency two cases are distinguished:

High Frequency Mode (≥ 100 kHz):

There are no t_{RC} max. time nor $\overline{CS1}/\overline{OE}$ max. low time restrictions during subsequent random read or write accesses.

Low Frequency Mode (< 100 kHz):

There are no t_{RC} max. time nor $\overline{CS1}/\overline{OE}$ max. low time restrictions if all control signals ($\overline{CS1}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}/\overline{LB}$) follow the modified timing as shown below, see attached timing diagram and timing table. There is no extra mode register setting necessary.



(note) A20 is "don't care" in 16M CellularRAM

Figure 19 Low Frequency Mode

Parameter	Symbol	70		85		Unit	Notes
		Min.	Max.	Min.	Max.		
Address stable time for read access	t_{ARV}	70	–	85	–	ns	–
Address stable overlap with write pulse	t_{AWV}	70	–	85	–	ns	–
Write pulse width	t_{WPV}	70	–	85	–	ns	–
Data to write time overlap	t_{DWV}	70	–	85	–	ns	–

6 Appendix B: S/W Register Entry Mode (“4-cycle method”)

Other than $\overline{ZZ}$-controlled SCR operation, CellularRAM supports software (S/W) method as an alternative to access the control registers. Since S/W register entry mode consists of 4 consecutive access cycles to top memory location (all addresses are “1”), it is often referred as “4-cycle method”. 4-cycles starts from 2 back-to-back read cycles (initializing command identification) followed by one write cycle (command identification completed and refresh control register is accessed), then final write cycle for configuring the RCR by the given input or read cycle to check the content of the register through DQ pins. It does function the configuration of control register bits like the way with dedicated pin, $\overline{ZZ}$ method, but there are a few differences from $\overline{ZZ}$-controlled method as follow;

- Register read mode (checking content) is supported with S/W register entry as well as register write (program).
- The mode bits for control register are supplied through DQ <15:0> instead of address pins in $\overline{ZZ}$-controlled. Though each register has 20-bits (A<19:0>) for 16M CellularRAM, only low 16-bit registers becomes valid during S/W method.
- The valid selection of refresh control register, RCR, is done with the state of DQ<15:0> given at 3rd cycle. (“00h”)
- Since S/W register entry asks for 4 complete access cycles in a row and the device is designed operating with internally regulated supply which is going to be discharged in deep power-down (DPD) mode, **DPD function is not supported** with this programming method.
- The method is realized by the device exactly when 2 consecutive read cycles to top memory location is followed by write cycle to the same location, so that any exceptional cycle combination - not only access mode, but also the number of cycles - will fail in invoking the register entry mode properly.

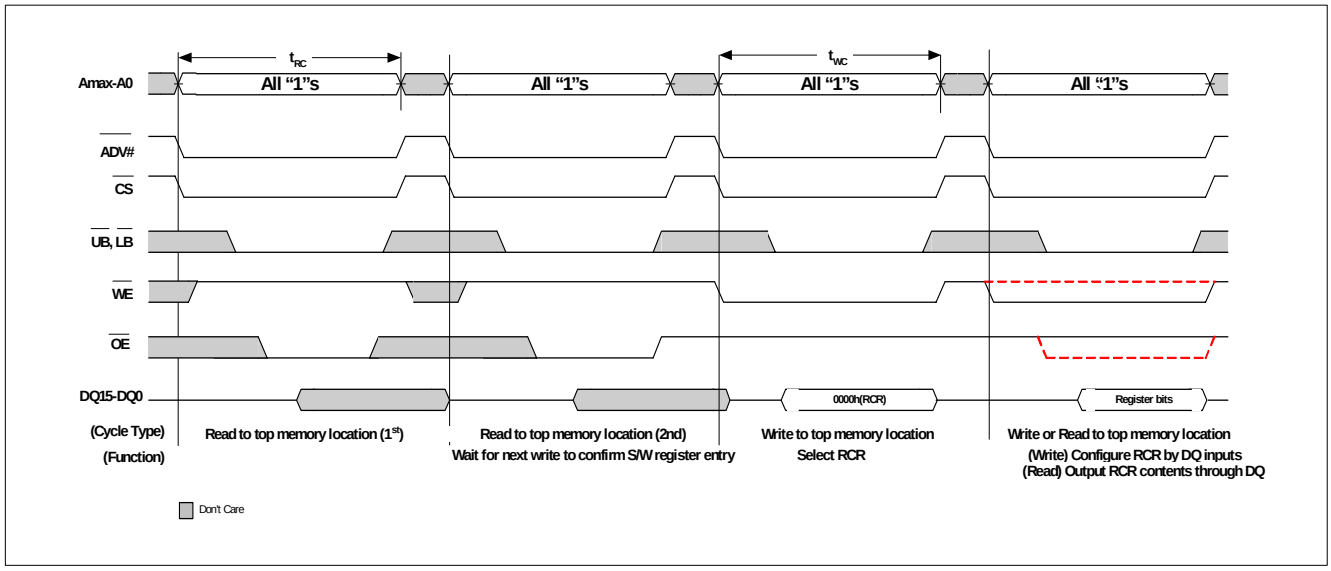


Figure 20 S/W Register Entry timing (Address input = FFFFFh)

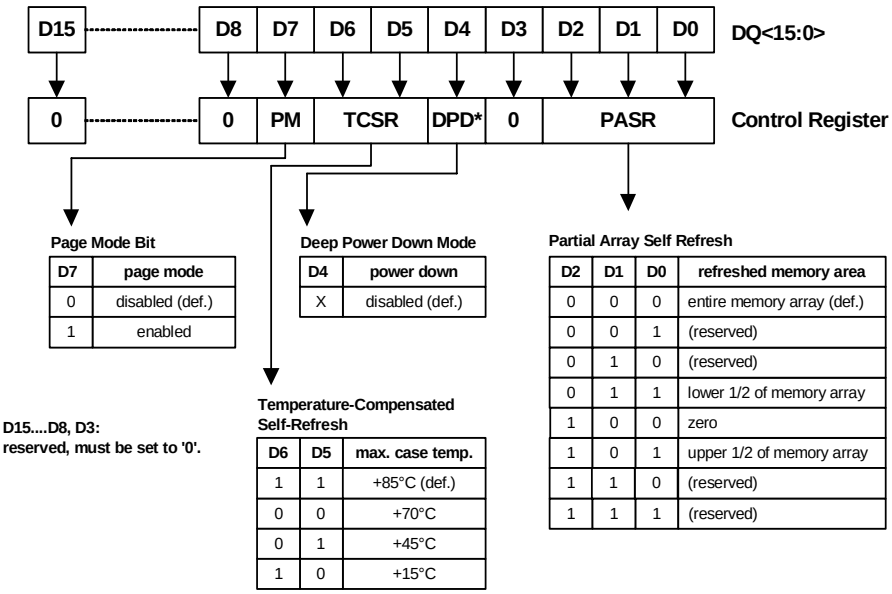


Figure 21 RCR Mapping in S/W Register Entry

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