FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27225-4E

ASSP For Power Management Applications

6-ch DC/DC Converter IC with Synchronous Rectifier for Voltage Step-up and Step-down

MB3883

■ DESCRIPTION

The MB3883 is a 6-channel step-up/step-down DC/DC converter IC using pulse width modulation (PWM) and synchronous rectification, designed for low voltage, high efficiency, and compact size. This IC is ideal for up conversion, down conversion, and up/down conversion (using a step-up/step-down Zeta system with free input and output settings).
The MB3883 can operate at low voltage levels, and has a wide supply voltage range from 1.7 V to 9 V.
The MB3883 is available in two packages, an LQFP-48P or a leadless BCC-48P formed with a contact electrode pad only.
This is an ideal power supply for high-performance portable devices such as digital still cameras.
This product is covered by US Patent Number 6,147,477.

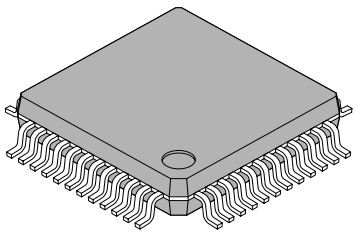
■ FEATURES

- Supports synchronous rectification (CH1, 2, 5)
- Supports for down-conversion and up/down Zeta conversion (CH1, 2)
  Supports for up-conversion (CH5)
- Supports up-conversion (CH3, 4, 6)
- Low start-up voltage : 1.7 V (CH6)

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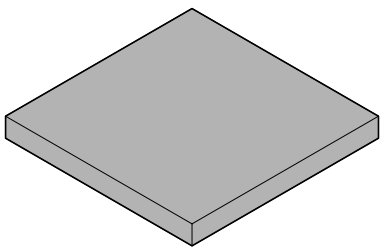
■ PACKAGES

48-pin plastic LQFP



(FPT-48P-M05)

48-pad plastic BCC



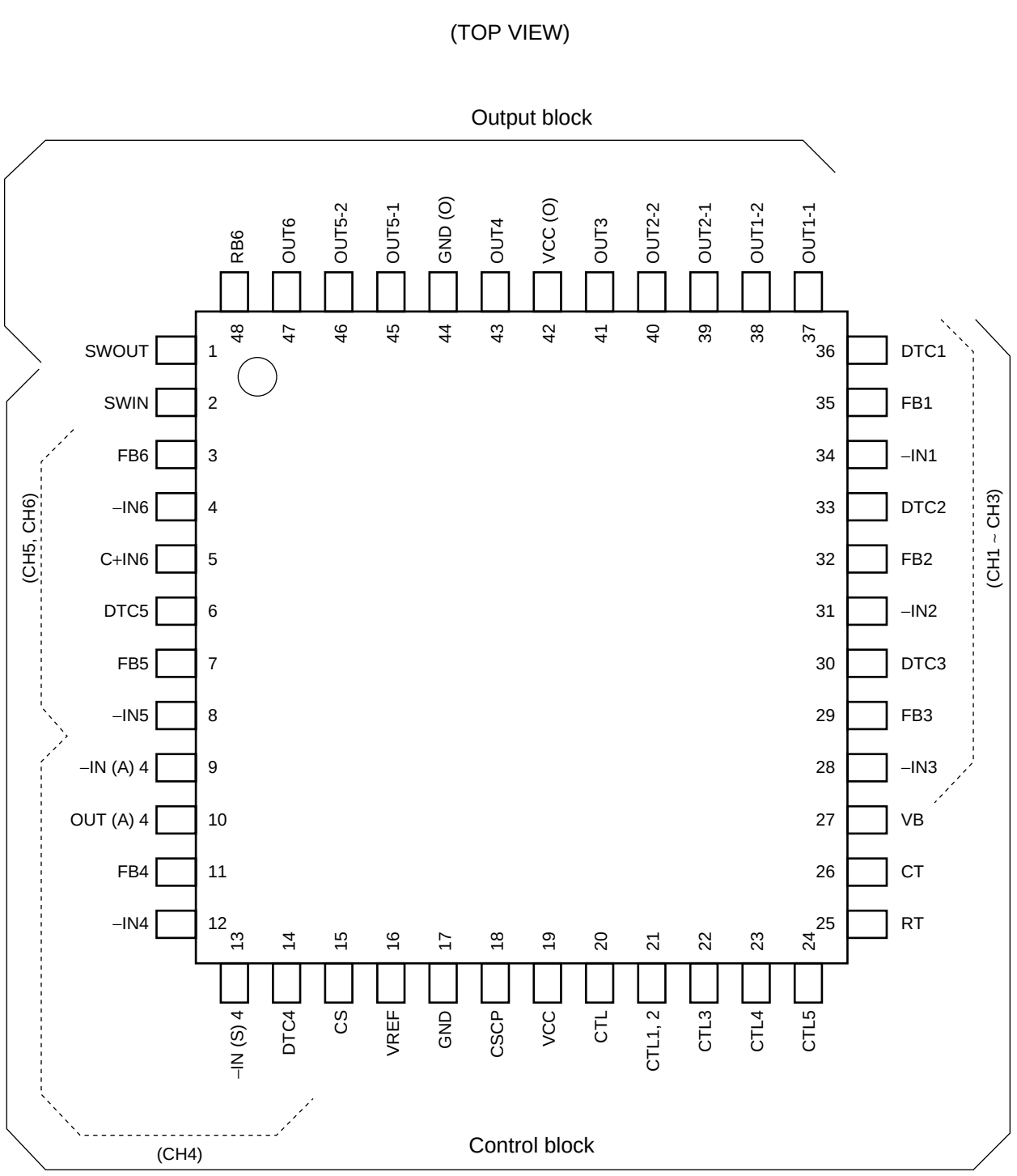
(LCC-48P-M02)

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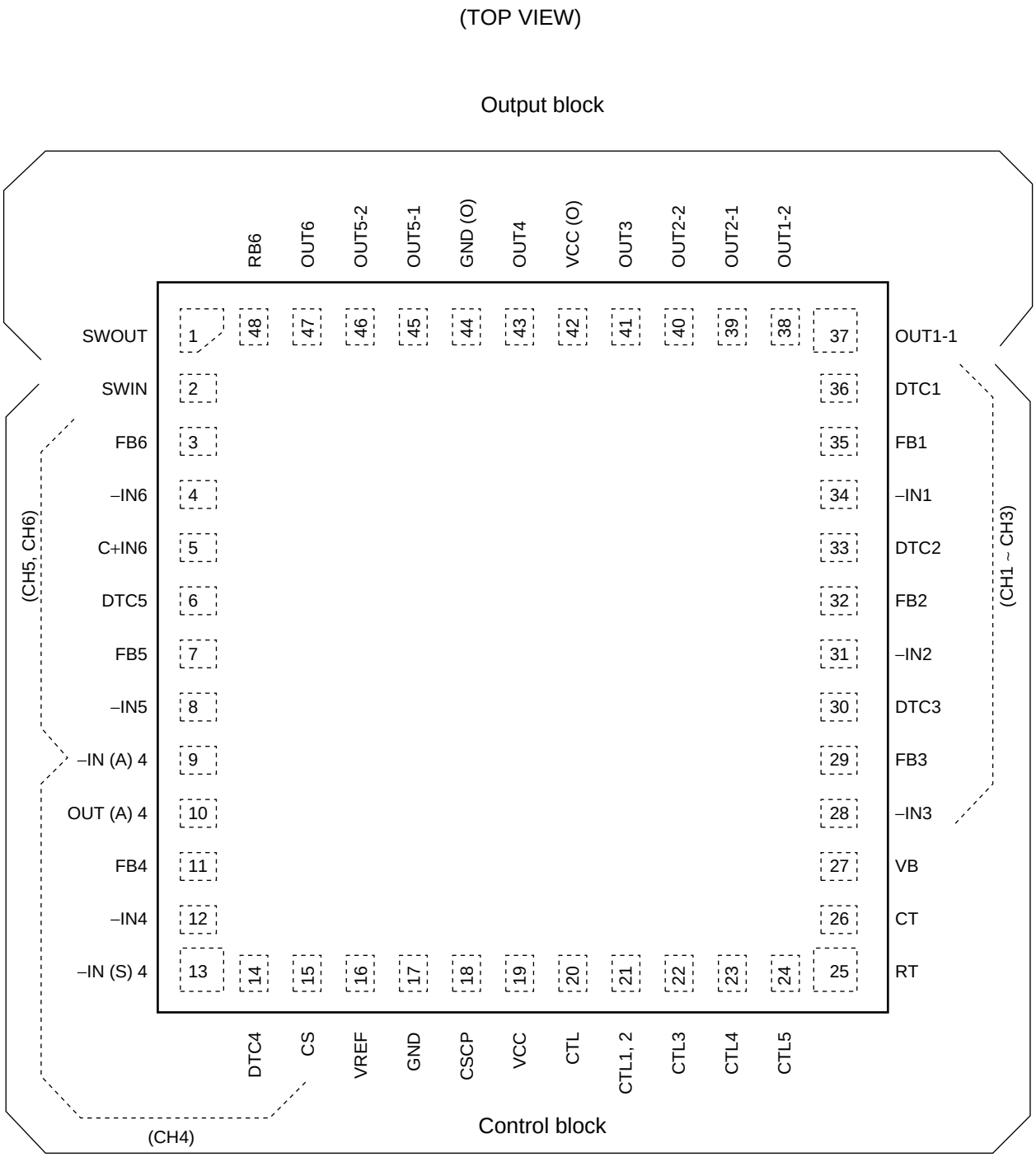
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- Power supply voltage range : 2.4 V to 9 V (CH6)
  : 3.6 V to 9 V (CH1 to CH5)
- Built-in high-precision reference voltage circuit : ±1 %
- Wide operating oscillator frequency range with high-frequency capability : 100 kHz to 1 MHz
- Error amplifier output for soft start (CH1 to CH6)
- Totem-pole type output switch control circuit

■ PIN ASSIGNMENTS



(FPT-48P-M05)


(TOP VIEW)
Output block
RB6
OUT6
OUT5-2
OUT5-1
GND (O)
OUT4
VCC (O)
OUT3
OUT2-2
OUT2-1
OUT1-2
SWOUT
SWIN
FB6
–IN6
C+IN6
DTC5
FB5
–IN5
–IN (A) 4
OUT (A) 4
FB4
–IN4
–IN (S) 4
OUT1-1
DTC1
FB1
–IN1
DTC2
FB2
–IN2
DTC3
FB3
–IN3
VB
CT
RT
(CH5, CH6)
(CH1 ~ CH3)
(CH4)
DTC4
CS
VREF
GND
CSCP
VCC
CTL
CTL1, 2
CTL3
CTL4
CTL5
Control block

(LCC-48P-M02)

■ PIN DESCRIPTION

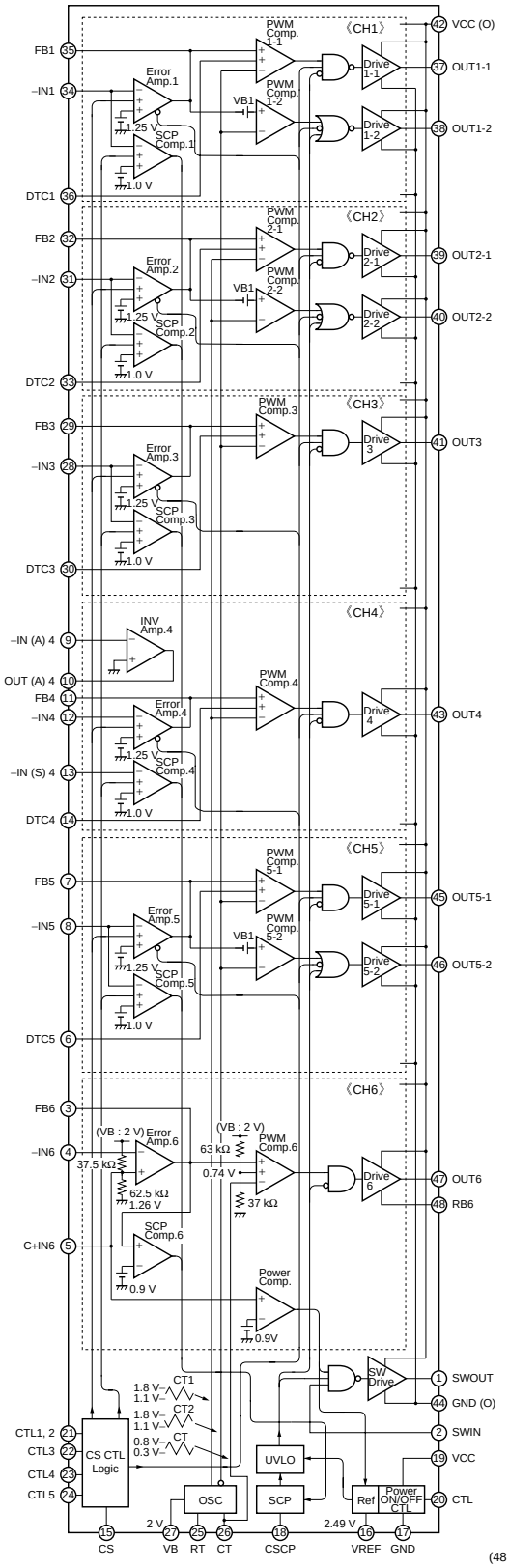
Pin No.		Symbol	I/O	Descriptions
CH1	35	FB1	O	Error amplifier output pin.
	34	–IN1	I	Error amplifier inverted input pin.
	36	DTC1	I	Dead time control pin.
	37	OUT1-1	O	Main side output pin.
	38	OUT1-2	O	Synchronous rectifier side output pin.
CH2	32	FB2	O	Error amplifier output pin.
	31	–IN2	I	Error amplifier inverted input pin.
	33	DTC2	I	Dead time control pin.
	39	OUT2-1	O	Main side output pin.
	40	OUT2-2	O	Synchronous rectifier side output pin.
CH3	29	FB3	O	Error amplifier output pin.
	28	–IN3	I	Error amplifier inverted input pin.
	30	DTC3	I	Dead time control pin.
	41	OUT3	O	Output pin.
CH4	11	FB4	O	Error amplifier output pin.
	12	–IN4	I	Error amplifier inverted input pin.
	14	DTC4	I	Dead time control pin.
	43	OUT4	O	Output pin.
	9	–IN (A) 4	I	Inverting amplifier input pin.
	10	OUT (A) 4	O	Inverting amplifier output pin.
	13	–IN (S) 4	I	Short detection comparator inverted input pin.
CH5	7	FB5	O	Error amplifier output pin.
	8	–IN5	I	Error amplifier inverted input pin.
	6	DTC5	I	Dead time control pin.
	45	OUT5-1	O	Main side output pin.
	46	OUT5-2	O	Synchronous rectifier side output pin.
CH6	3	FB6	O	Error amplifier output pin.
	4	–IN6	I	Error amplifier inverted input pin.
	5	C+IN6	I	Soft start capacitor connection pin.
	48	RB6	O	Output current setting resistor connection pin.
	47	OUT6	O	Output pin.

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Pin No.		Symbol	I/O	Descriptions
OSC	25	RT	—	Triangular wave frequency setting resistor connection pin.
	26	CT	—	Triangular wave frequency setting capacitor connection pin.
	27	VB	O	Triangular wave oscillator regulator output pin.
Control	1	SWOUT	O	Output switch control circuit output pin.
	2	SWIN	I	Output switch control circuit input pin.
	20	CTL	I	Power supply, CH6 control pin. “H” level : Power supply CH6 operating mode “L” level : Standby mode
	21	CTL1, 2	I	CH1, CH2 control pin. When CTL1, 2 pin = “H” level “H” level : CH1, CH2 operating mode “L” level : CH1, CH2 OFF mode
	22	CTL3	I	CH3 control pin. When CTL3 pin = “H” level “H” level : CH3 operating mode “L” level : CH3 OFF mode
	23	CTL4	I	CH4 control pin. When CTL4 pin = “H” level “H” level : CH4 operating mode “L” level : CH4 OFF mode
	24	CTL5	I	CH5 control pin. When CTL5 pin = “H” level “H” level : CH5 operating mode “L” level : CH5 OFF mode
	18	CSCP	—	Short protection circuit capacitor connection pin.
	15	CS	—	CH1to CH5 soft start circuit capacitor connection pin.
Power	19	VCC	—	Reference voltage and control circuit power supply pin.
	42	VCC (O)	—	Output circuit power supply pin.
	16	VREF	O	Reference voltage output pin.
	17	GND	—	Ground pin.
	44	GND (O)	—	Output circuit ground pin.

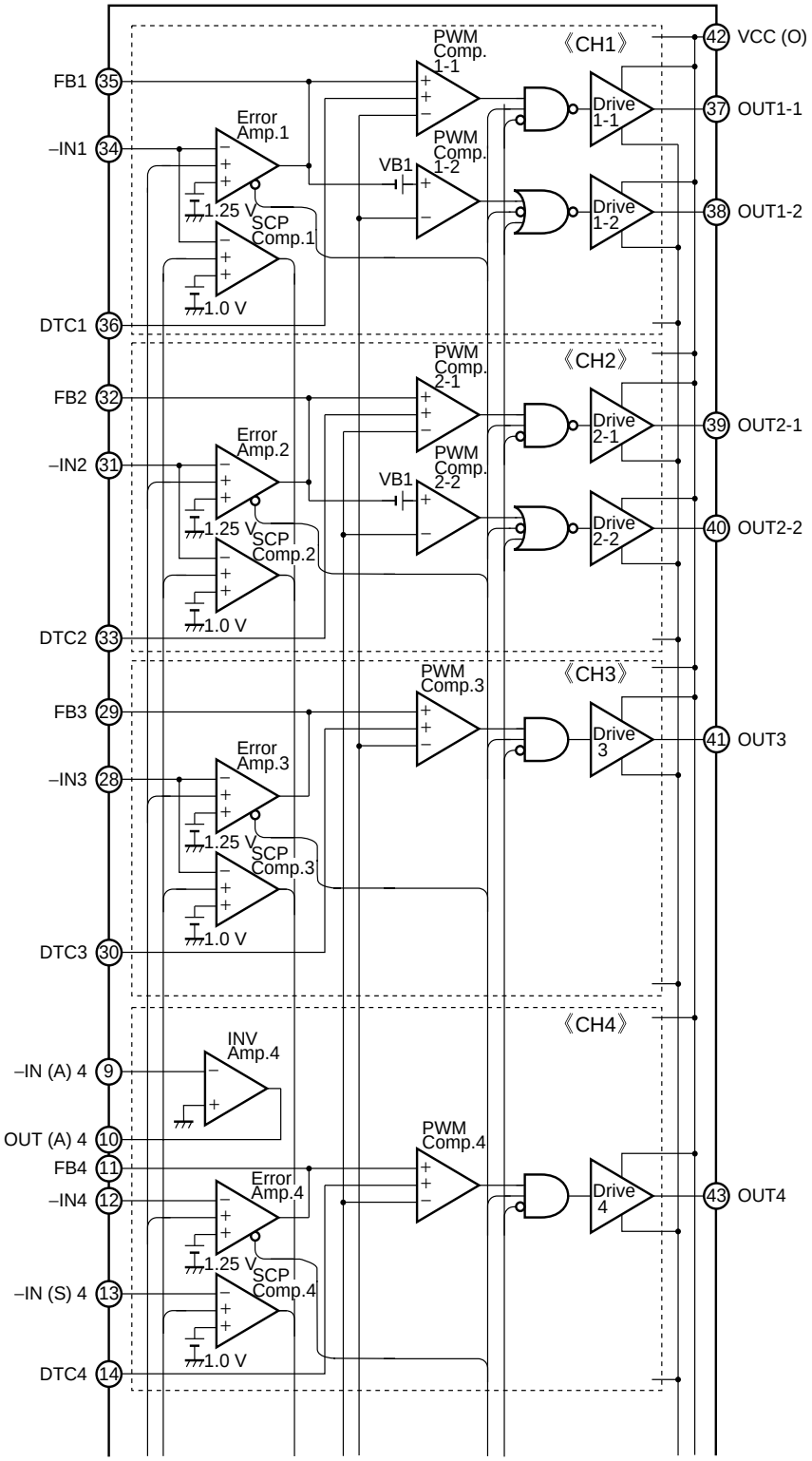
■ BLOCK DIAGRAM



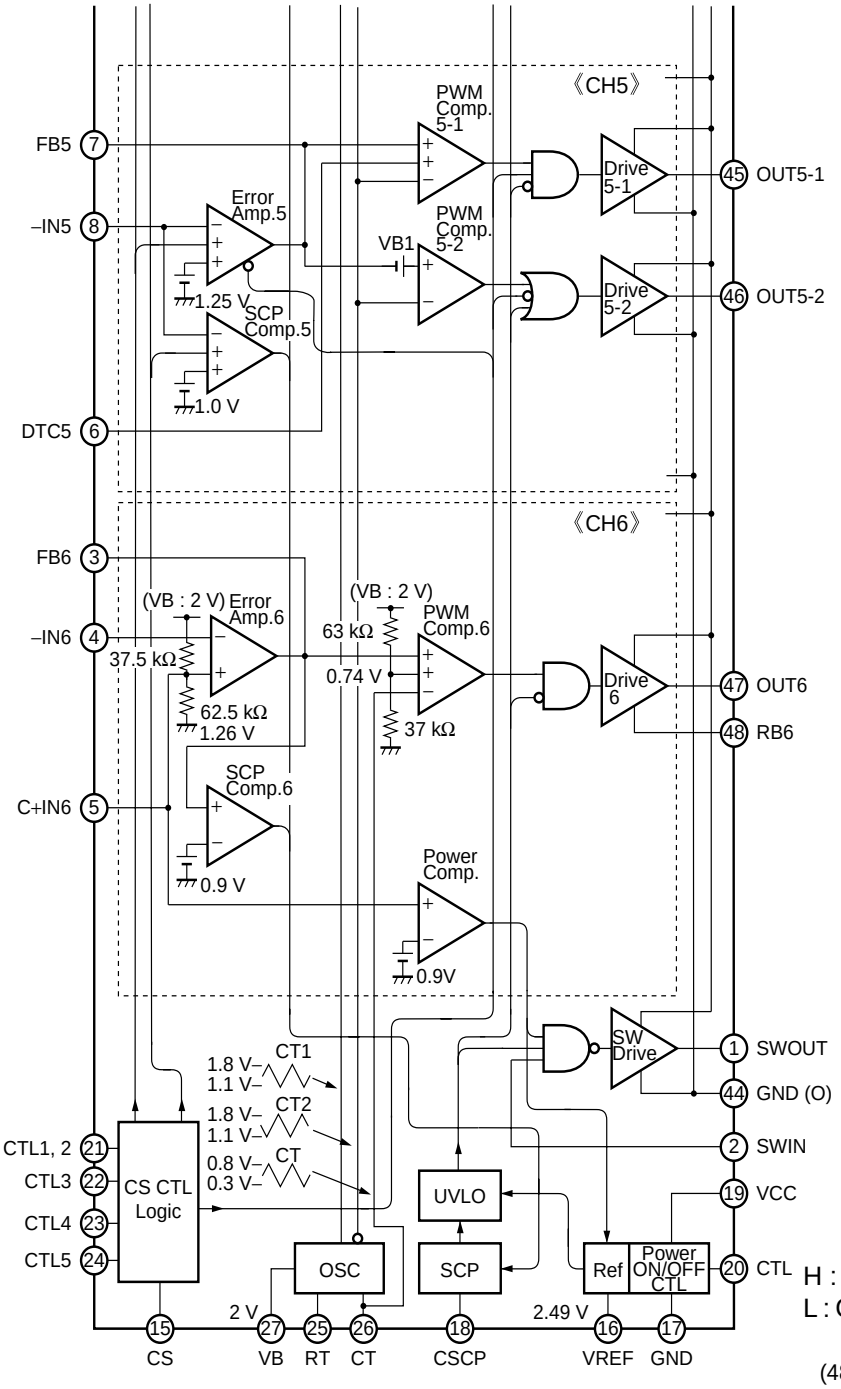
H : ON (Power/CH6)
L : OFF (Standby mode)

(48 Pin)

• Block diagram (Expansion 1/2)



• Block diagram (Expansion 2/2)



H : ON (Power/CH6)
L : OFF (Standby mode)

(48 Pin)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	—	—	10	V
	I_O	OUT pin	—	20	mA
Output current	I_O	OUT pin, Duty ≤ 5%	—	200	mA
Output peak current	P_D	Ta ≤ +25 °C (LQFP-48P)	—	860*	mW
Power dissipation		Ta ≤ +25 °C (BCC-48P)	—	710*	mW
Storage temperature	Tstg	—	−55	+125	°C

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Startup power supply voltage	V_{CC}	CH6	1.7	—	9	V
Power supply voltage	V_{CC}	CH6	2.4	5.0	9	V
		CH1 to CH5	3.6	5.0	9	V
Reference voltage output current	I_{OR}	VREF pin	–1	—	0	mA
VB pin output current	I_B	VB pin	–0.5	—	0	mA
Input voltage	V_{IN}	–IN1 to –IN5, –IN (A) 4, –IN (S) 4 pin	0	—	V_{CC} – 1.8	V
		–IN6 pin	0	—	V_{CC} – 0.9	V
Control input voltage	V_{CTL}	CTL pin	0	—	9	V
Output current	I_O	OUT pin (CH1 to CH5)	—	2	15	mA
		OUT pin (CH6)	1	2	15	mA
		SWOUT pin	—	1	4	mA
Output current setting resister	R_B	RB6 pin	2.4	24	51	kΩ
Oscillator frequency	f_{OSC}	—	100	500	1000	kHz
Timing capacitor	C_T	—	47	100	560	pF
Timing resistor	R_T	—	8.2	18	100	kΩ
Soft-start capacitor	C_S	CH1 to CH5	—	0.027	1.0	µF
	C_{+IN6}	CH6	—	0.47	1.0	µF
Short detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
VB pin capacitor	C_{VB}	—	0.082	0.18	—	µF
Operating ambient temperature	Ta	—	–30	25	85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC = 5 V)

Parameter			Symbol	Pin No.	Conditions	Value			Unit
						Min.	Typ.	Max.	
Reference voltage block [REF]		Reference voltage	V_{REF}	16	—	2.46	2.49	2.51	V
		Output voltage temperature stability	$\Delta V_{REF}/V_{REF}$	16	Ta = –30 °C to +85 °C	—	0.5*	—	%
		Input stability	Line	16	VCC = 3.6 V to 9 V	–10	—	10	mV
		Load stability	Load	16	VREF = 0 mA to –1 mA	–10	—	10	mV
		Short-circuit output current	I_{OS}	16	VREF = 2 V	–20	–5	–1	mA
Under voltage lockout protection circuit block [U.V.L.O]	CH1 to CH5	Threshold voltage	V_{TH}	37	VCC = ↗	2.6	2.8	3.0	V
		Hysteresis width	V_H	37	—	—	0.2	—	V
		Reset voltage	V_{RST}	37	VCC = ↘	1.20	1.30	1.40	V
	CH6	Threshold voltage	V_{TH}	47	VCC = ↗	1.35	1.5	1.65	V
Soft-start block [CS]		Input standby voltage	V_{STB}	15	—	—	50	100	mV
		Charge current	I_{CS}	15	—	–1.4	–1.0	–0.6	µA
Short circuit detection block [SCP]		Threshold voltage	V_{TH}	18	—	0.65	0.70	0.75	V
		Input standby voltage	V_{STB}	18	—	—	50	100	mV
		Input latch voltage	V_I	18	—	—	50	100	mV
		Input source current	I_{CSCP}	18	—	–1.4	–1.0	–0.6	µA
Triangular wave oscillator block [OSC]		Oscillator frequency	f_{OSC}	37, 38, 39, 40, 41, 43, 45, 46, 47	CT = 100 pF, RT = 18 kΩ VB = 2 V	450	500	550	kHz
		Frequency stability for voltage	Δf/fdv	37, 38, 39, 40, 41, 43, 45, 46, 47	VCC = 3.6 V to 9 V	—	1	10	%
		Frequency stability for temperature	Δf/fdt	37, 38, 39, 40, 41, 43, 45, 46, 47	Ta = –30 °C to +85 °C	—	1*	—	%

*: Standard design value.

(Continued)

(Ta = +25 °C, VCC = 5 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Error amplifier block (CH1 to CH5) [Error Amp.]	Threshold voltage	V_{TH}	35, 32, 29, 11, 7	FB = 1.45 V	1.23	1.25	1.27	V
	V_T temperature stability	$\Delta V_T/V_T$	35, 32, 29, 11, 7	Ta = –30 °C to +85 °C	—	0.5*	—	%
	Input bias current	I_B	34, 31, 28, 8	–IN = 0 V (CH1 to CH3, CH5)	–320	–80	—	nA
			12	–IN = 0 V (CH4)	–120	–30	—	nA
	Voltage gain	A_V	35, 32, 29, 11, 7	DC	60	100	—	dB
	Frequency bandwidth	BW	35, 32, 29, 11, 7	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	35, 32, 29, 11, 7	—	2.2	2.4	—	V
		V_{OL}	35, 32, 29, 11, 7	—	—	50	200	mV
	Output source current	I_{SOURCE}	35, 32, 29, 11, 7	FB = 1.45 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	35, 32, 29, 11, 7	FB = 1.45 V	70	140	—	µA
Error amplifier bolck (CH6) [Error Amp.]	Threshold voltage	V_{TH}	3	FB = 0.55 V	1.24	1.26	1.28	V
	V_T temperature stability	$\Delta V_T/V_T$	3	Ta = –30 °C to +85 °C	—	0.5*	—	%
	Input bias current	I_B	4	–IN = 0 V	–100	–20	—	nA
	Voltage gain	A_V	3	DC	60	75	—	dB
	Frequency bandwidth	BW	3	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	3	—	1.1	1.3	—	V
		V_{OL}	3	—	—	0	200	mV
	Output source current	I_{SOURCE}	3	FB = 0.55 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	3	FB = 0.55 V	60	120	—	µA
Inverting amplifier bolck (CH4) [Inv Amp.]	Input offset voltage	V_{IO}	10	OUT = 1.25 V	–10	0	10	mV
	Input bias current	I_B	9	–IN = 0 V	–120	–30	—	nA
	Voltage gain	A_V	10	DC	60	100	—	dB
	Frequency bandwidth	BW	10	A_V = 0 dB	—	1.0*	—	MHz
	Output voltage	V_{OH}	10	—	2.2	2.4	—	V
		V_{OL}	10	—	—	50	200	mV
	Output source current	I_{SOURCE}	10	OUT = 1.25 V	—	–2.0	–1.0	mA
	Output sink current	I_{SINK}	10	OUT = 1.25 V	70	140	—	µA

*: Standard design value.

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(Ta = +25 °C, VCC = 5 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Short detection comparator block (CH1 to CH5) [SCP Comp.]	Threshold voltage	V_{TH}	37, 38, 39, 40, 41, 43, 45, 46	CH1 to CH5	0.97	1.00	1.03	V
	Input bias current	I_B	34, 31, 28, 8	–IN = 0 V (CH1 to CH3, CH5)	–320	–80	—	nA
			13	–IN = 0 V (CH4)	–200	–50	—	nA
Short detection comparator block (CH6) [SCP Comp.]	Threshold voltage	V_{TH}	47	—	0.8	0.9	1.0	V
PWM Comp. block (CH1 to CH5) [PWM Comp.]	Threshold voltage	V_{T0}	37, 39, 41, 43, 45	Duty cycle = 0 %	1.0	1.1	—	V
		V_{T100}	37, 39, 41, 43, 45	Duty cycle = 100 %	—	1.8	1.9	V
	Input current	I_{DTC}	36, 33, 30, 14, 6	DTC = 0.4 V (CH1 to CH5)	–1.0	–0.3	—	µA
PWM Comp. block(CH6) [PWM Comp.]	Threshold voltage	V_{T0}	47	Duty cycle = 0 %	0.2	0.3	—	V
		V_{Tmax}	47	Duty cycle = Max.	—	0.74	0.84	V
	Maximum duty cycle	Dtr	47	CT = 100 pF, RT = 18 kΩ, RB = 24 kΩ	70	80	90	%
Output block (CH1, CH2, CH5) [Drive-1(Pch MOS)]	Output source current	I_{SOURCE}	37, 39, 45	Duty ≤ 5 %, OUT = 0 V	—	–130	–80	mA
	Output sink current	I_{SINK}	37, 39, 45	Duty ≤ 5 %, OUT = 5 V	65	100	—	mA
	Output ON resistor	R_{OH}	37, 39, 45	OUT = –15 mA	—	18	30	Ω
		R_{OL}	37, 39, 45	OUT = 15 mA	—	16	25	Ω
Output block (CH1 to CH5) [Drive-2(Nch MOS)]	Output source current	I_{SOURCE}	38, 40, 41, 43, 46	Duty ≤ 5 %, OUT = 0 V	—	–130	–80	mA
	Output sink current	I_{SINK}	38, 40, 41, 43, 46	Duty ≤ 5 %, OUT = 5 V	65	100	—	mA
	Output ON resistor	R_{OH}	38, 40, 41, 43, 46	OUT = –15 mA	—	18	30	Ω
		R_{OL}	38, 40, 41, 43, 46	OUT = 15 mA	—	16	25	Ω
Output block (CH6) [Drive]	Output source current	I_{SOURCE}	47	RB = 24 kΩ, OUT = 0.7 V	–2.6	–2.0	–1.4	mA
	Output sink current	I_{SINK}	47	Duty ≤ 5 %, OUT = 0.7 V	—	40	—	mA

*: Standard design value.

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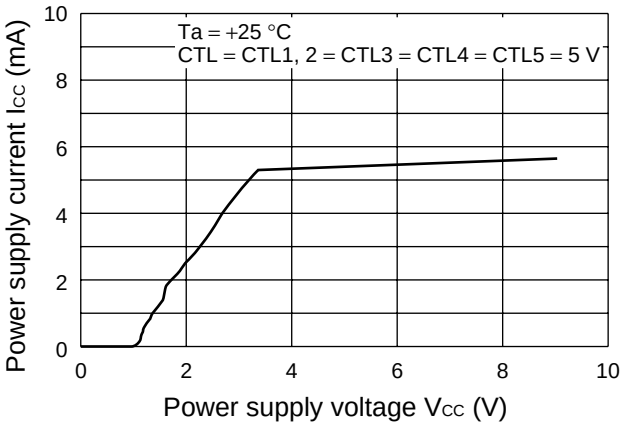
(Ta = +25 °C, VCC = 5 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Output switch control block (Drive-1 [SW])	SW input voltage	V_{IH}	5	SWOUT = “L” level	1.5	—	9	V
		V_{IL}	5	SWOUT = “H” level	0	—	0.5	V
	Input current	I_{SWIN}	5	SWIN = 5 V	—	100	200	µA
	Output source current	I_{SOURCE}	1	Duty ≤ 5 %, SWOUT = 0 V	—	–9	—	mA
	Output sink current	I_{SINK}	1	Duty ≤ 5 %, SWOUT = 5 V	—	17	—	mA
	Output ON resistor	R_{OH}	1	SWOUT = –4 mA	—	250	400	Ω
		R_{OL}	1	SWOUT = 4 mA	—	100	150	Ω
Control block (CTL, CTL1 to CTL5) [CTL]	CTL input voltage	V_{IH}	20, 21, 22, 23, 24	Active mode	1.5	—	9	V
		V_{IL}	20, 21, 22, 23, 24	Standby mode	0	—	0.5	V
	Input current	I_{CTL}	20, 21, 22, 23, 24	CTL = 5 V	—	100	200	µA
General	Standby current	I_{CCS}	19	CTL = 0 V	—	—	10	µA
		I_{CCS} (O)	42	CTL = 0 V	—	—	10	µA
	Power supply current	I_{CC}	19, 42	CTL = CTL1, 2 = CTL3 = CTL4 = CTL5 = 5 V	—	6	9	mA

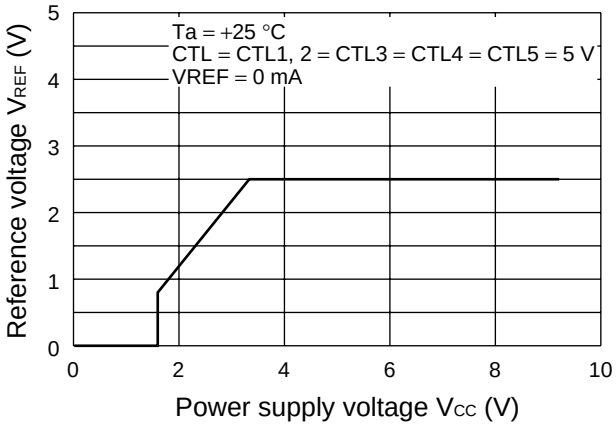
*: Standard design value.

■ TYPICAL CHARACTERISTICS

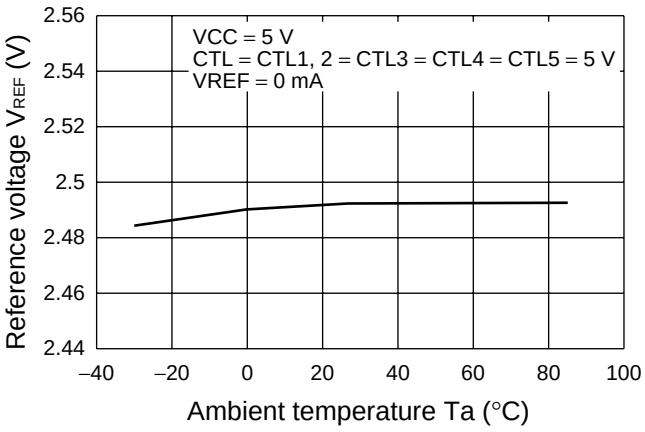
Power supply current vs. power supply voltage



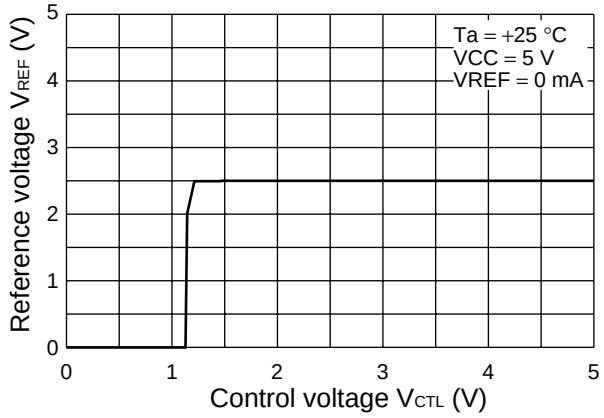
Reference voltage vs. power supply voltage



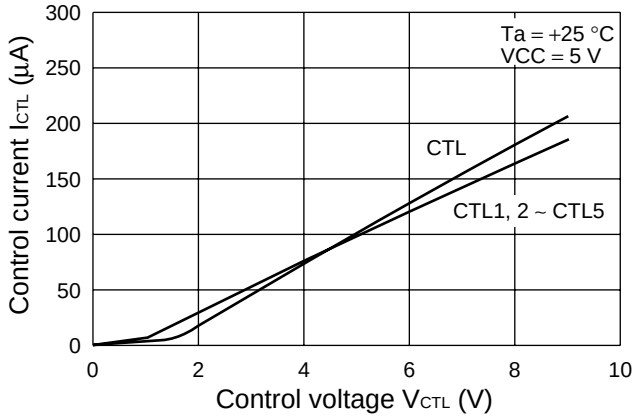
Reference voltage vs. ambient temperature



Reference voltage vs. control voltage

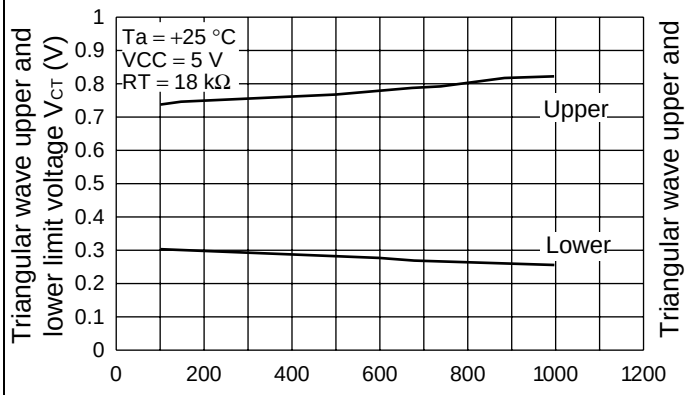


Control current vs. control voltage

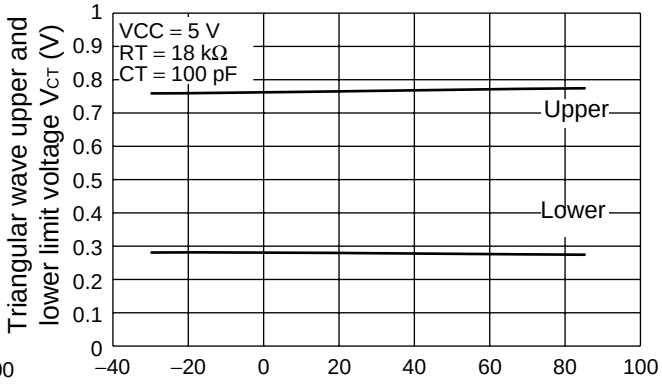


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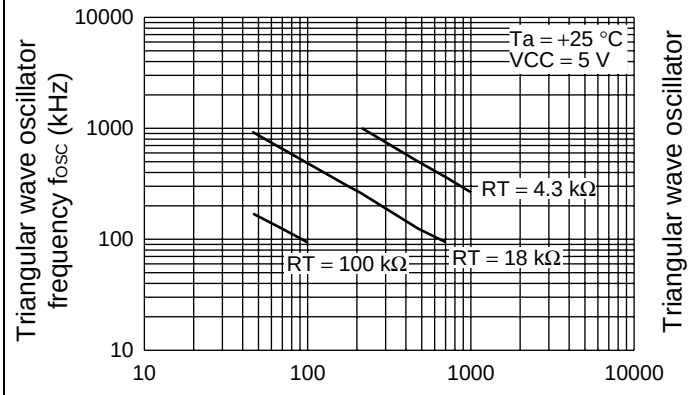
Triangular wave upper and lower limit voltage vs. triangular wave oscillator frequency



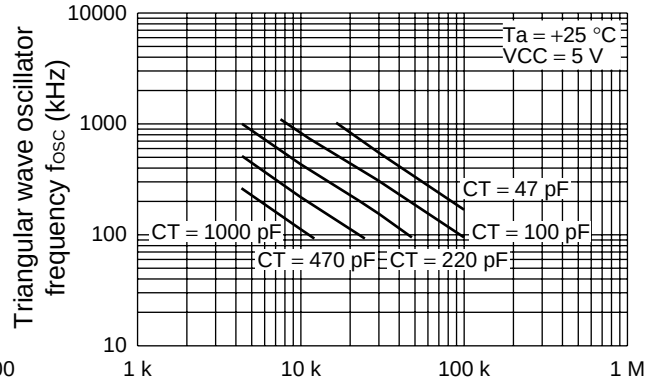
Triangular wave upper and lower limit voltage vs. ambient temperature



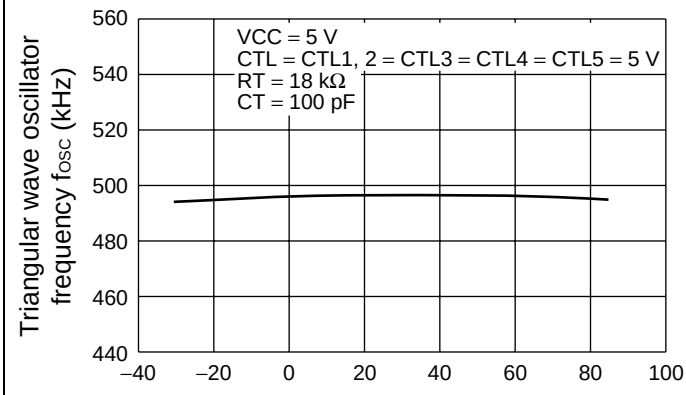
Triangular wave oscillator frequency vs. timing capacitor



Triangular wave oscillator frequency vs. timing resistor



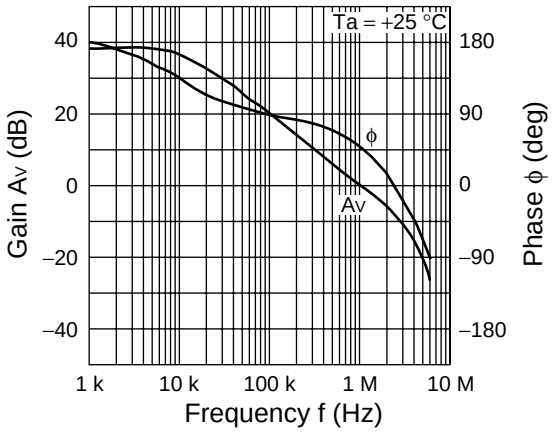
Triangular wave oscillator frequency vs. ambient temperature

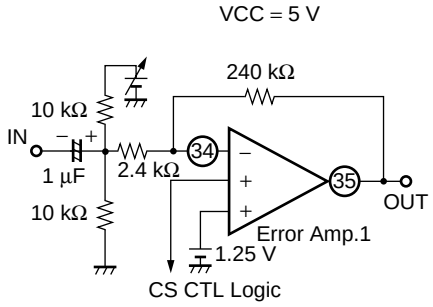


(Continued)

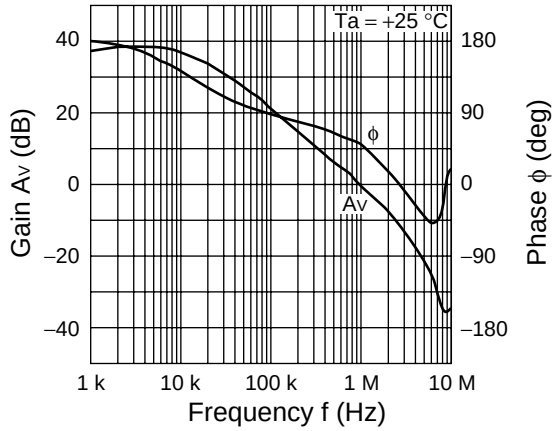
(Continued)

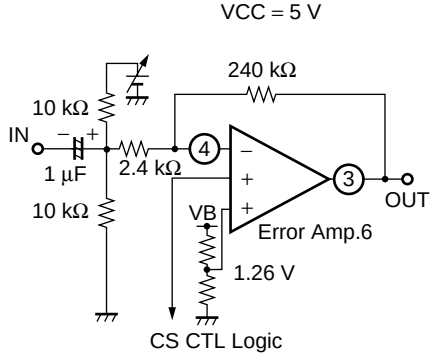
Error amplifier gain and phase vs. frequency (CH1)



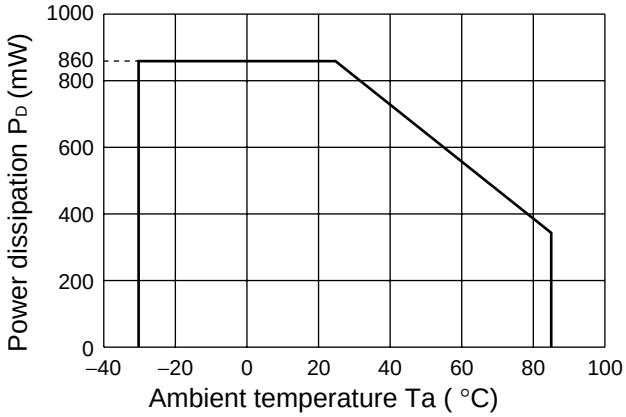


Error amplifier gain and phase vs. frequency (CH6)

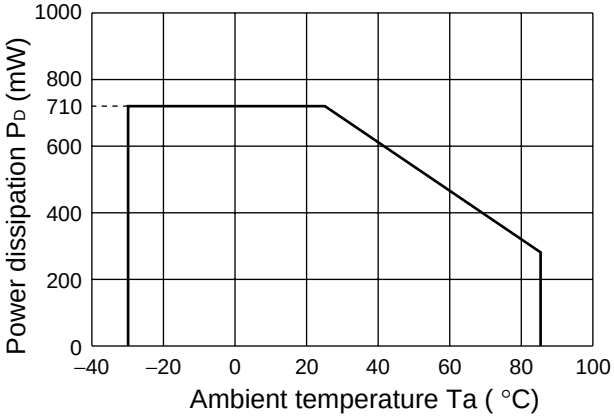




Power dissipation vs. ambient temperature (LQFP-48P)



Power dissipation vs. ambient temperature (BCC-48P)



■ FUNCTIONS

1. DC-DC Converter Functions

(1) Reference voltage block

The reference voltage circuit generates a temperature-compensated reference voltage (typically ≒ 2.49 V) from the voltage supplied from the power supply terminal (pin 19). The voltage is used as the reference voltage for the IC's internal circuitry.
The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 16).

(2) Triangular-wave oscillator block

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 26) and RT terminal (pin 25) to generate triangular oscillation waveform CT (amplitude of 0.3 V to 0.8 V), CT1 (amplitude 1.1 V to 1.8 V in phase with CT), or CT2 (amplitude 1.1 V to 1.8 V in inverse phase with CT).
CT1 and CT2 are input to the PWM comparator in the IC.

(3) Error amplifier (Error Amp.) block

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. It supports a wide range of in-phase input voltages from 0 V to "V_{CC} - 1.8 V" (channels 1 to 5), or 0 V to "Vcc-0.9 V"(channel6) allowing easy setting from the external power supply.
In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output pin to inverted input pin of the error amplifier, enabling stable phase compensation to the system.

(4) Inverting amplifier (Inv Amp.) block

The inverting amplifier detects the DC/DC converter output voltage (as a negative voltage) and outputs a control signal to the error amp.

(5) PWM comparator (PWM Comp.) block

The PWM comparator is a voltage-to-pulse width converter for controlling the output duty depending on the input voltage.

Channels 1, 2, and 5 main sides,channel 3,4, and 6 : The comparator keeps the output transistor on while the error amplifier output voltage and DTC voltageremain higher than the triangular wave voltage.

Channels 1, 2, and 5 synchronous rectification sides : The comparator keeps the output transistor on while the error amplifier output voltage remain lower than the triangular wave voltage.

(6) Output block

The output block on the main side and on the synchronous rectification side is both in the totem pole configuration, capable of driving an external P-channel MOS FET (channels 1, 2 main sides, channel 5 synchronous rectification side), NPN transistor (channel 6), and N-channel MOS FET (channels 3, 4, channel 5 main side, channels 1, 2 synchronous rectification sides).

2. Channel Control Function

Channels are turned on and off depending on the voltage levels at the CTL terminal (pin 20), CTL1, 2 terminal (pin 21), CTL3 terminal (pin 22), CTL4 terminal (pin 23), and CTL5 terminal (pin 24).

Channel On/Off Setting Conditions

Voltage level at CTL pin					Channel on/off state				
CTL	**CTL1, 2**	**CTL3**	**CTL4**	**CTL5**	**Power/CH6**	**CH1, CH2**	**CH3**	**CH4**	**CH5**
L	×	×	×	×	OFF (Standby state)				
H	L	L	L	L	ON	OFF	OFF	OFF	OFF
				H					ON
			H	L				ON	OFF
				H					ON
		H	L	L			ON	OFF	OFF
				H					ON
			H	L				ON	OFF
				H					ON
	H	L	L	L		ON	OFF	OFF	OFF
				H					ON
			H	L				ON	OFF
				H					ON
		H	L	L			ON	OFF	OFF
				H					ON
			H	L				ON	OFF
				H					ON

× : Undefined

3. Protective Functions

(1) Timer-latch short-circuit protection circuit

The short-circuit detection comparator in each channel detects the output voltage level and, if any channel output voltage falls below the short-circuit detection voltage, the timer circuits is actuated to start charging the external capacitor C_{SCP} connected to the CSCP terminal (pin 18).
When the capacitor voltage reaches about 0.70 V, the circuit is turned off the output transistor and sets the dead time to 100 %.
To reset the actuated protection circuit, turn the power supply on back. (See “SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.)

(2) Undervoltage lockout protection circuit

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the undervoltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 18) at the “L” level.
The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

(3) Output switch control circuit

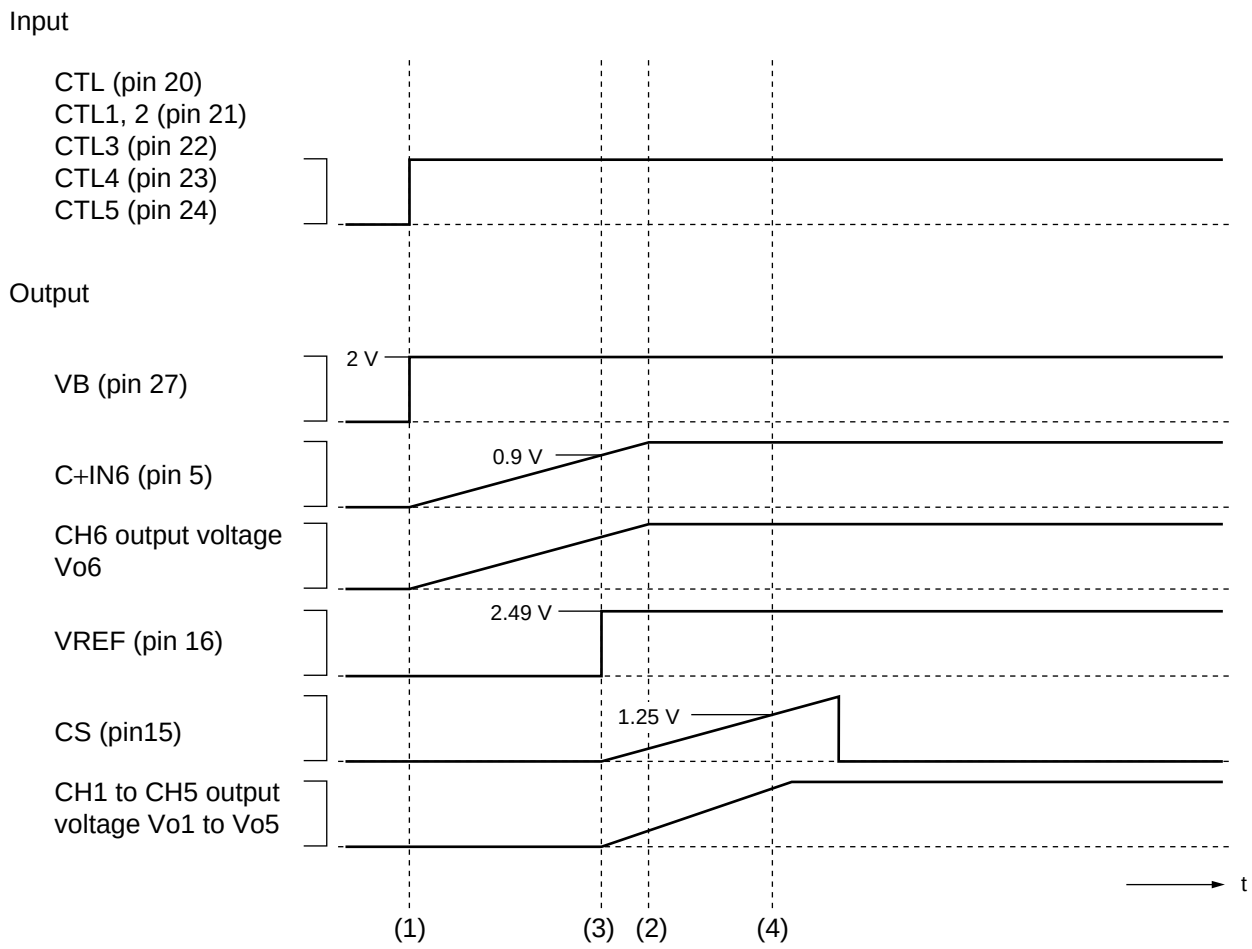
When the power is turned on, this circuit prevents reactive current flow to external step-up circuits on CH5 and CH6. When the SWIN terminal (pin 2) is a state at “H” level after releasing UVLO and the C+IN6 terminal (pin5) voltage goes above 0.9 V (Typ.), the SWOUT terminal (pin 1) becomes “L” level. External P-ch MOS FET is turned on at this time and the output voltage is generated.

4. Soft Start Operation

1. Description

- When the CTL, CTL1,2, CTL3, CTL4, and CTL5 terminals are driven high (“H” level) at the same time

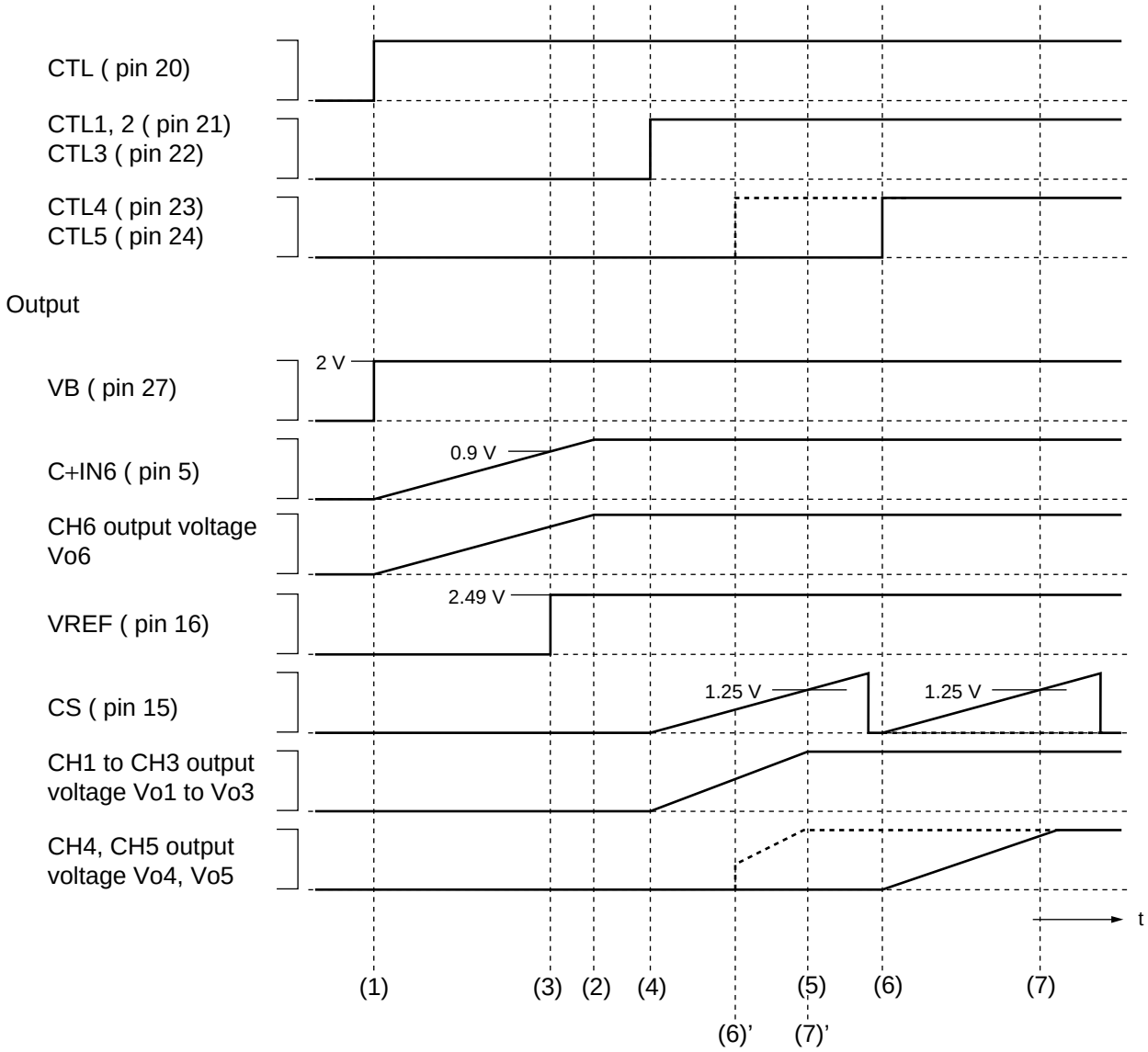
The capacitor (C+IN6) connected to the C+IN6 terminal (pin 5) starts charging. When the C+IN6 terminal voltage falls below 0.9 V (Typ.), the capacitor (Cs) connected to the CS terminal (pin 15) starts charging and the error amp. provides a soft start by comparing the CH1 to CH5 output voltage to the voltage at the CS terminal.



(1) to (2) : CH6 soft start interval
(3) to (4) : CH1 to CH5 soft start interval

- After a CH6 soft start, when the CTL1, 2, CTL3, CTL4, and CTL5 terminals are driven high

The capacitor (Cs) connected to the CS terminal (pin 15) starts charging and the error amp provides a soft start by comparing the CH1 to CH5 output voltage to the voltage at the CS terminal.



(1) to (2) : CH6 soft start interval
(3) : VREF Output start
(4) to (5) : CH1 to CH3 soft start interval
(6) to (7) : CH4, CH5 soft start interval
(6)' to (7)' : CH4 (CH5) soft start interval (waveform) as CTL4 (CTL5) go "H" from "L" during CH1 to CH3 soft start interval

Note : Each of the terminals CTL1,2, CTL3, CTL4, and CTL5 can be switched on or off independently. When any of these CTL terminals is switched on, a soft start operation is provided as shown in the above timing chart.

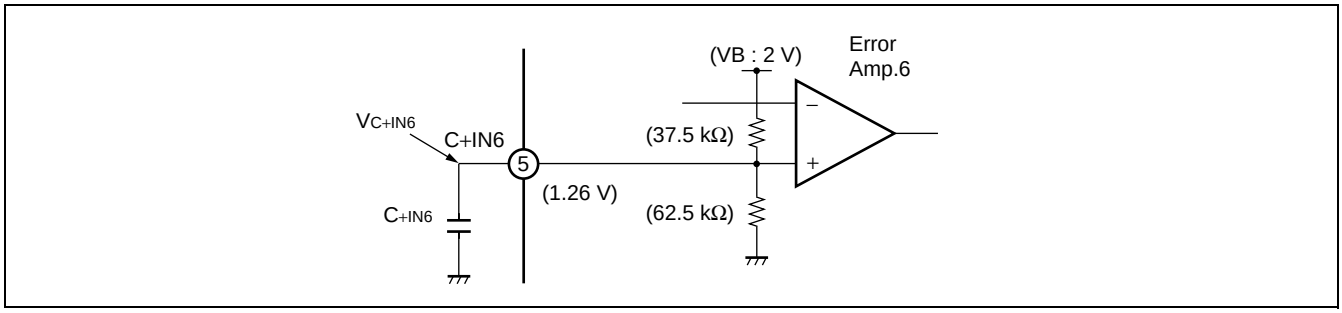
2. Soft Start Settings

- CH6 soft start time

The soft start operation is determined by the capacitor (C+IN6) connected to the C+IN6 terminal (pin 5). The soft start time depends on the input voltage and load current.

CH6 soft start time

$$ts\ (s) = -\frac{C_{+IN6}\ (F) \times 37.5\ (k\Omega) \times 62.5\ (k\Omega)}{100\ (k\Omega)} \ln\left(1 - \frac{V_{C+IN6}\ (V)}{1.26\ (V)}\right)$$



CH6 soft start equivalent circuit

Example: The soft start time until CH6 output voltage reaches 95% of the set voltage is determined as follows:

$$ts\ (s) \fallingdotseq 0.07 \times C_{+IN6}\ (\mu F)$$

- CH1 to CH5 soft start time

CH1 to CH5 soft start time

$$ts\ (s) \fallingdotseq 1.25 \times C_S\ (\mu F)$$

Note : The short-circuit detection function remains working during soft start operation on channels 1 through 5.

■ SETTING THE TRIANGULAR OSCILLATOR FREQUENCY

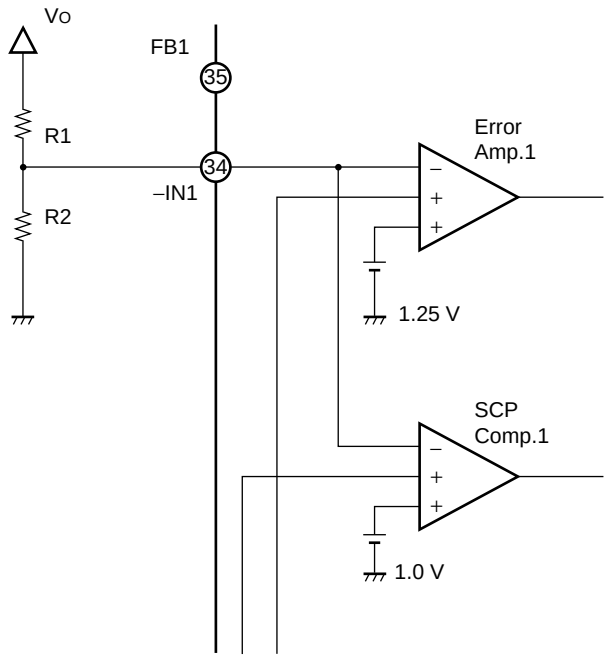
The triangular oscillator frequency is determined by the timing capacitor (C_T) connected to the CT terminal (pin 26), and the timing resistor (R_T) connected to the RT terminal (pin 25).

Triangular oscillator frequency

$$f_{OSC}\ (kHz) \fallingdotseq \frac{900000}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

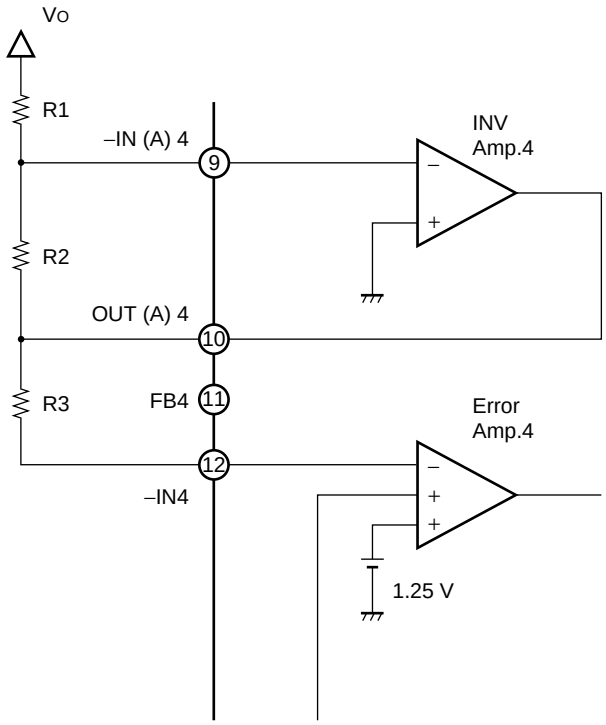
■ SETTING THE OUTPUT VOLTAGE

• CH1 to CH3, CH5



$$V_O = \frac{1.25\ V}{R2}\ (R1 + R2\ )$$

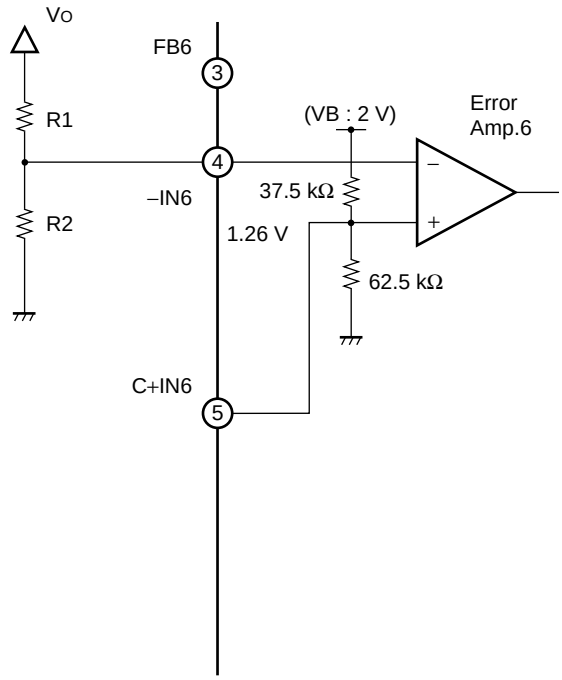
• CH4



$$V_O = \frac{V_{-IN\ (A)\ 4} - V_{OUT\ (A)\ 4}}{R2}\ R1$$

$$\left[\ V_{OUT\ (A)\ 4} = V_{-IN4}\ \right]$$

• CH6



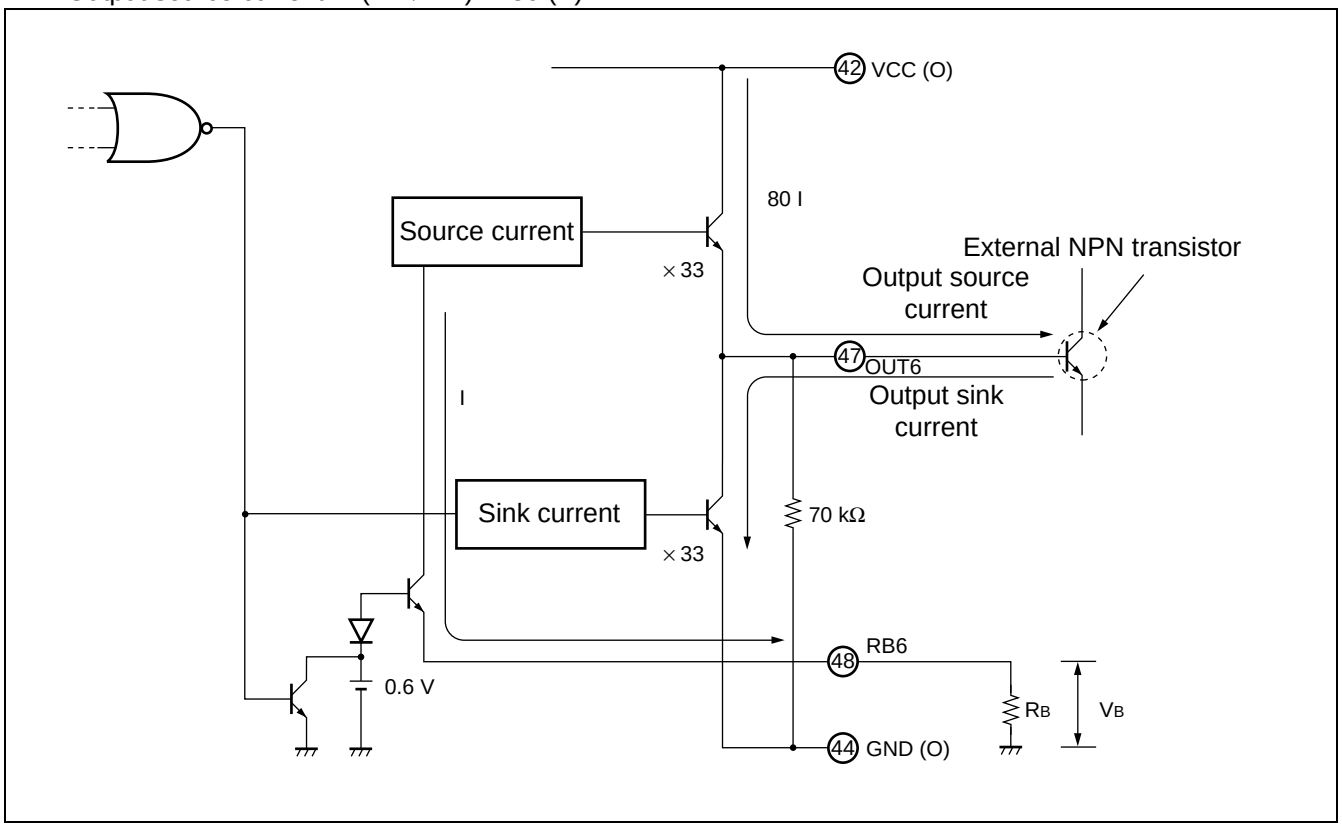
$$V_O = \frac{1.26\ V}{R2}\ (R1 + R2)$$

■ SETTING THE OUTPUT CURRENT

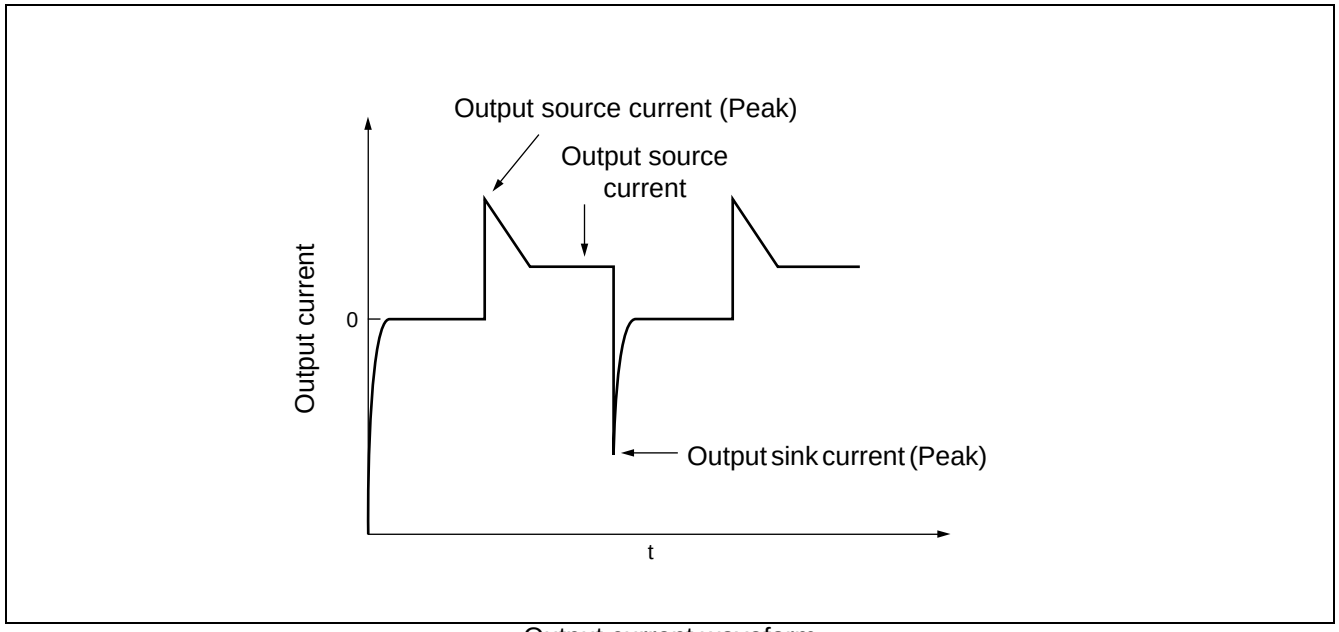
The output circuit (drive 6) is structured as illustrated below (in the output circuit diagram). As found in “Output Current Waveform” below, the source current value of the output current waveform has a constant current setting.

Note that the source current is set by the following equation:

- Output source current = (VB / RB) × 80 (A)



In the output circuit diagram



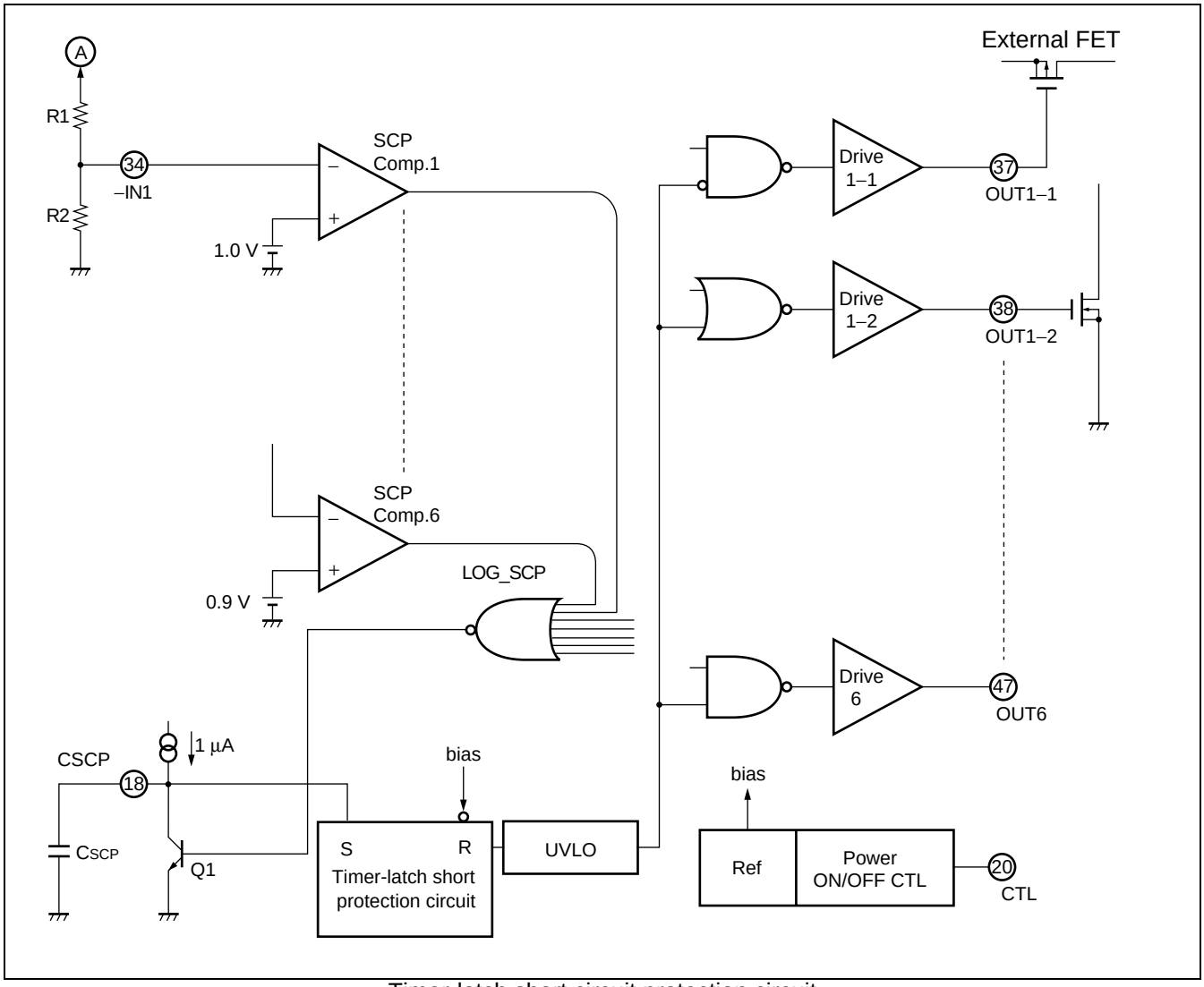
Output current waveform

■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

The short detection comparator (SCP comparator) in each channel monitors the output voltage.
While the switching regulator load conditions are stable on all channels, the LOG_SCP output remains at “H” level, transistor Q1 is turned on, and the CSCP terminal (pin 18) is held at “L” level.
If the load condition on a channel changes rapidly due to a short of the load, causing the output voltage to drop, the output of the short detection comparator on that channel goes to “H” level. This causes transistor Q1 to be turned off and the external short protection capacitor C_{SCP} connected to the CSCP terminal to be charged at 1.0 µA.
Short detection time (t_{PE})

$$t_{PE}\ (s) \fallingdotseq 0.70 \times C_{SCP}\ (\mu F)$$

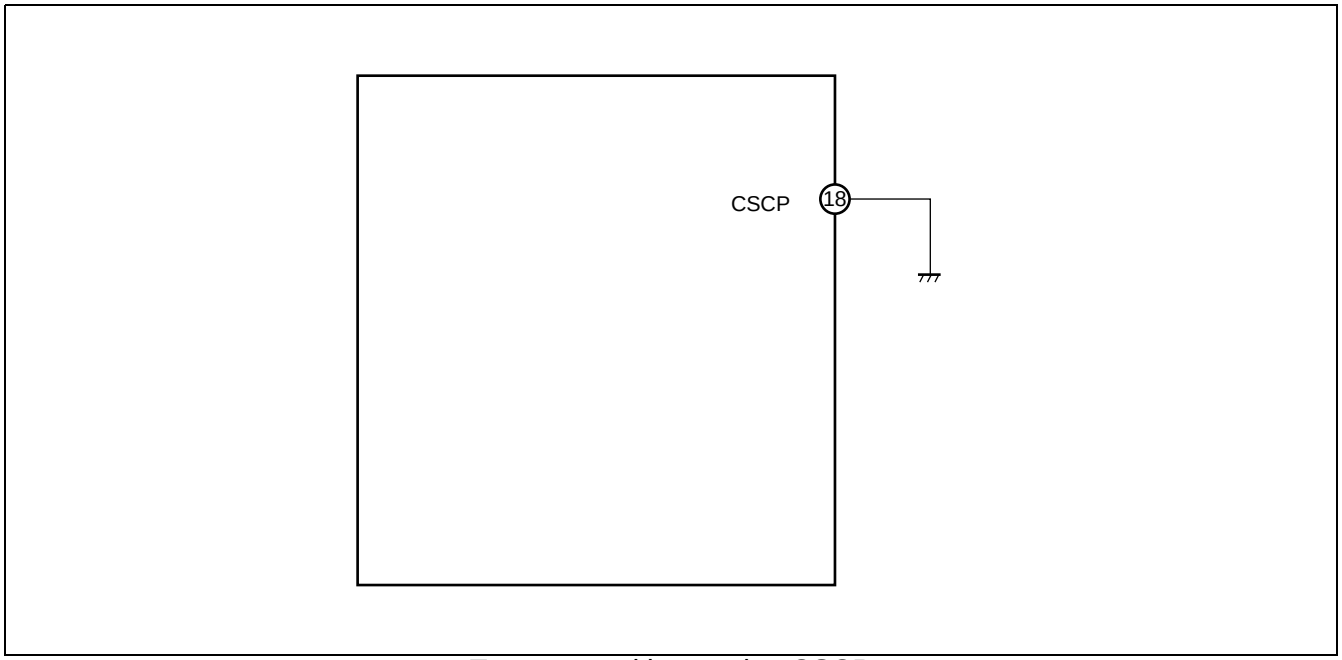
When the capacitor C_{SCP} is charged to the threshold voltage (VTH ≒ 0.70 V), the latch is set and the external FET is turned off (dead time is set to 100%). At this point, the latch input is closed and the CSCP terminal is held at “L” level.



Timer-latch short circuit protection circuit

■ TREATMENT WITHOUT USING CSCP

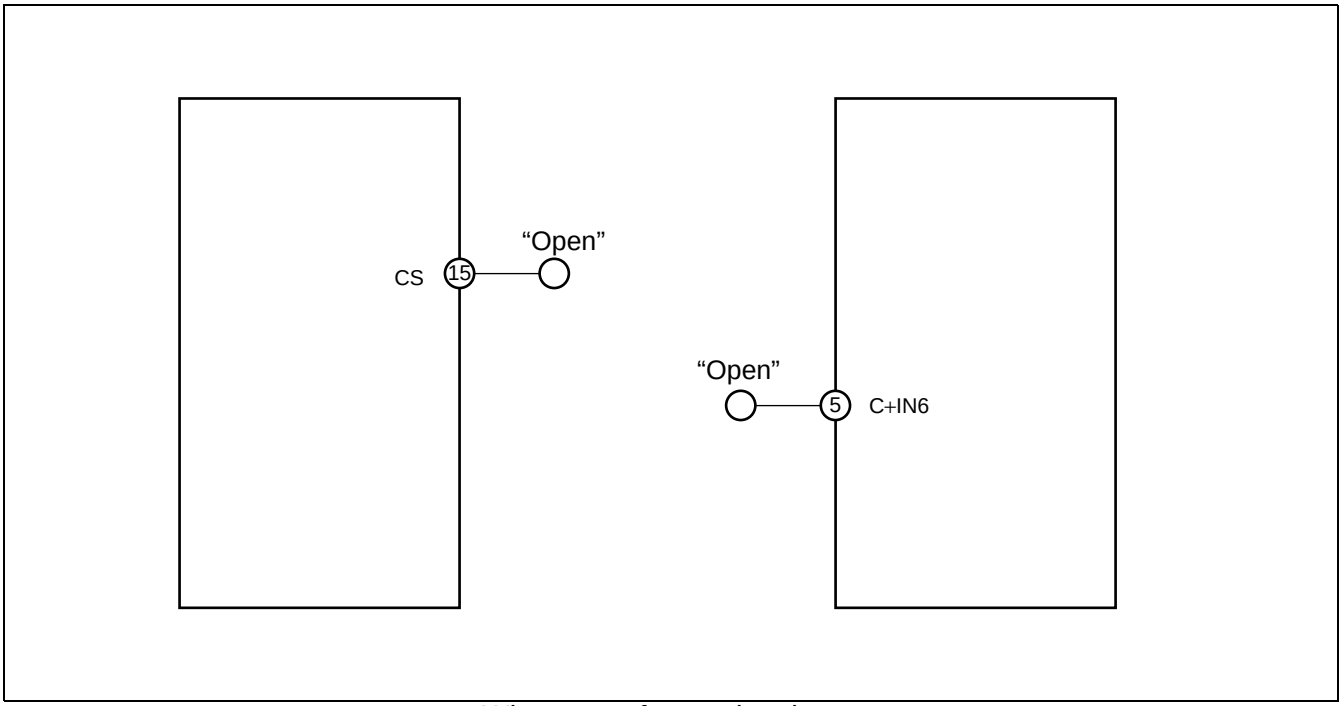
When not using the timer-latch short protection circuit, connect the CSCP terminal (pin 18) to GND with the shortest distance.



Treatment without using CSCP

■ OPERATING WITHOUT THE SOFT START FUNCTION

To disable the CH1 to CH5 soft start function, leave the CS terminal (pin 15) open.
To disable the CH6 soft start function, leave the C+IN6 terminal (pin 5) open.



When no soft start time is set

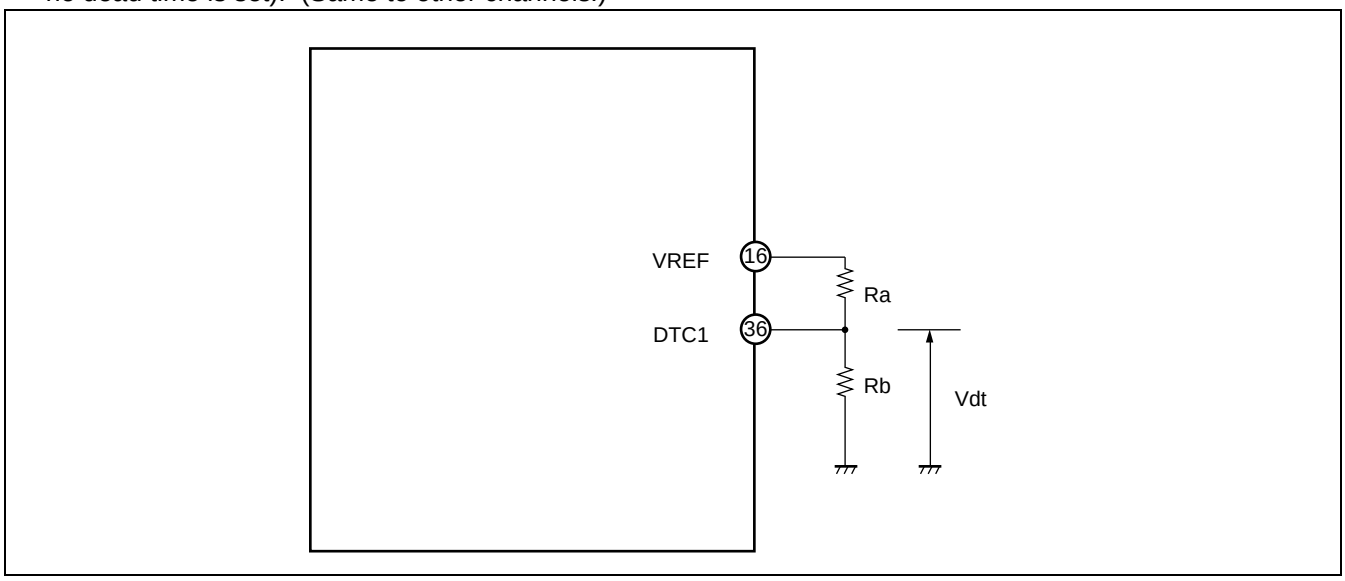
■ SETTING THE DEAD TIME

When the device is set for step-up inverted output based on the step-up or step-up/down Zeta method or flyback method, the FB pin voltage may reach and exceed the rectangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100 %). To prevent this, set the maximum duty of the output transistor. To set it, set the voltage at the DTC1 terminal (pin 36) by applying a resistive voltage divider to the VREF voltage as shown below.

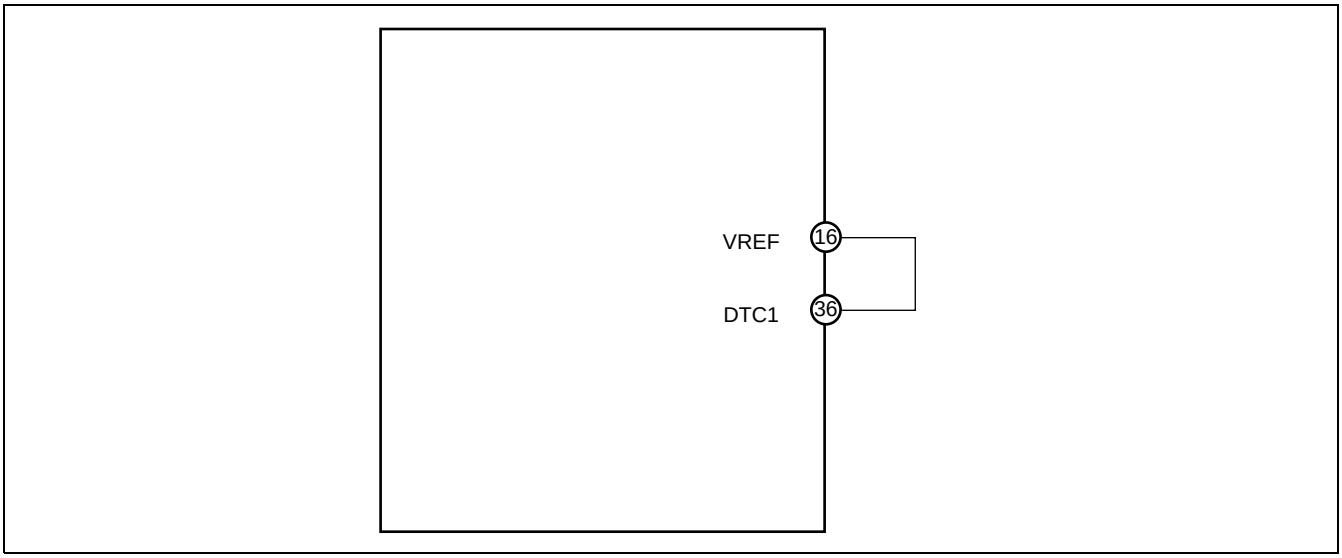
When the voltage at the DTC1 terminal (pin 36) is higher than the triangular wave voltage (CT1), the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude ≒ 0.7 V and triangular wave minimum voltage ≒ 1.1 V is given below. (Same to other channels.)

$$\text{DUTY (ON) max} \fallingdotseq \frac{\text{Vdt} - 1.1\ \text{V}}{0.7\ \text{V}} \times 100\,(\%)\ ,\ \text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF}$$

When the DTC1 terminal is not used, connect it directly to the VREF terminal (pin 16) as shown below (when no dead time is set). (Same to other channels.)



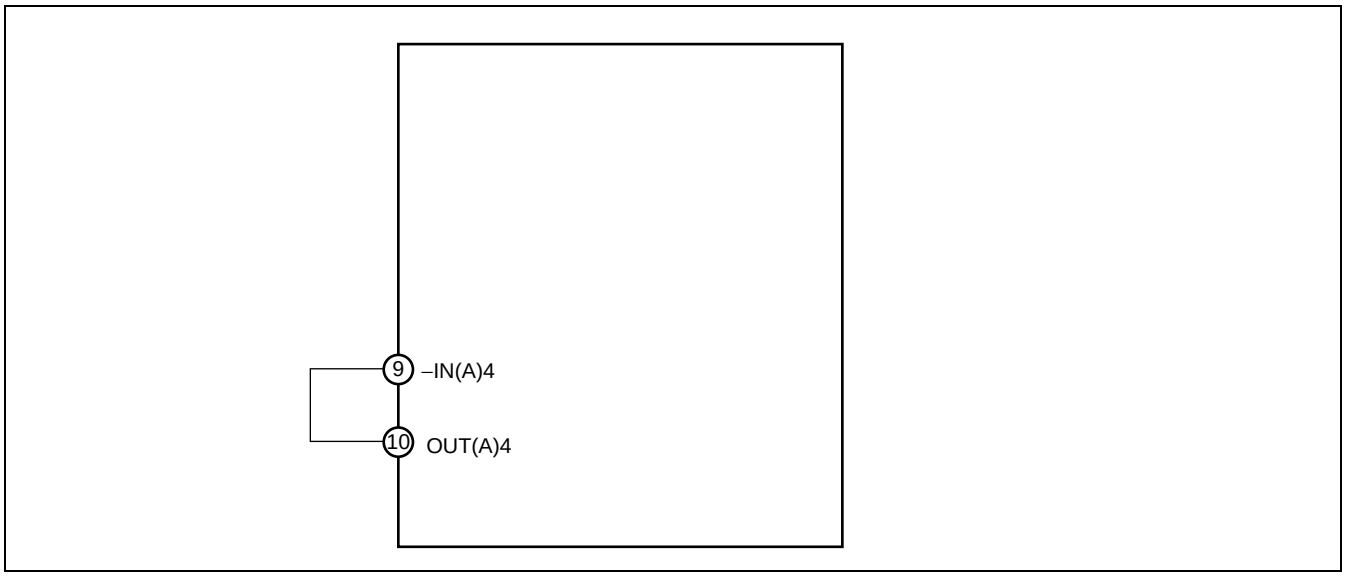
When using DTC to set dead time (Same to other channels.) (CH1)



When no dead time is set (Same to other channels.) (CH 1)

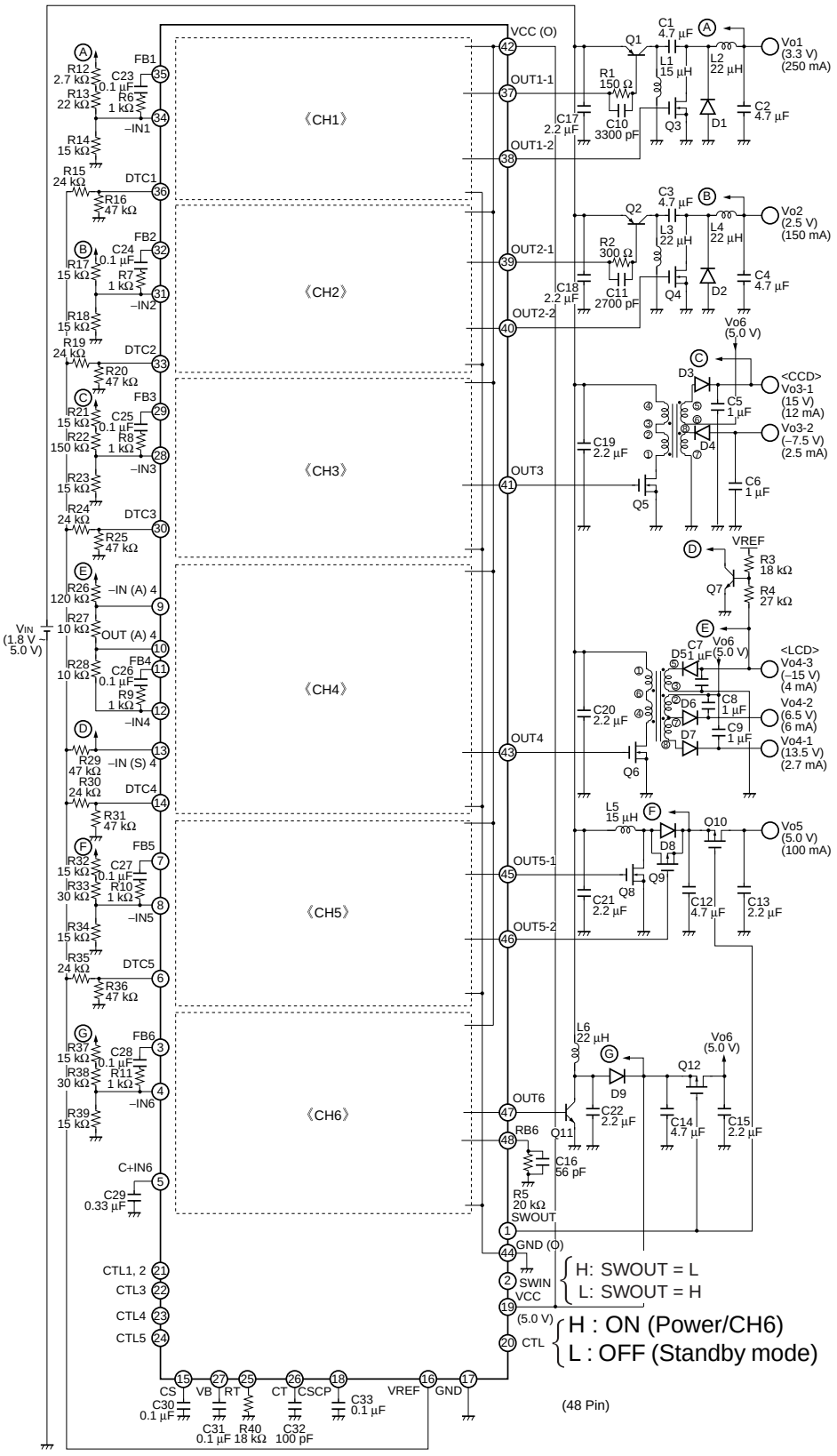
■ TREATMENT WITHOUT USING CH4 INV Amp.

When not using the CH4 INV Amp., connect the -IN(A)4 terminal (pin 9) to the OUT(A)4 terminal (pin 10) with the shortest distance.

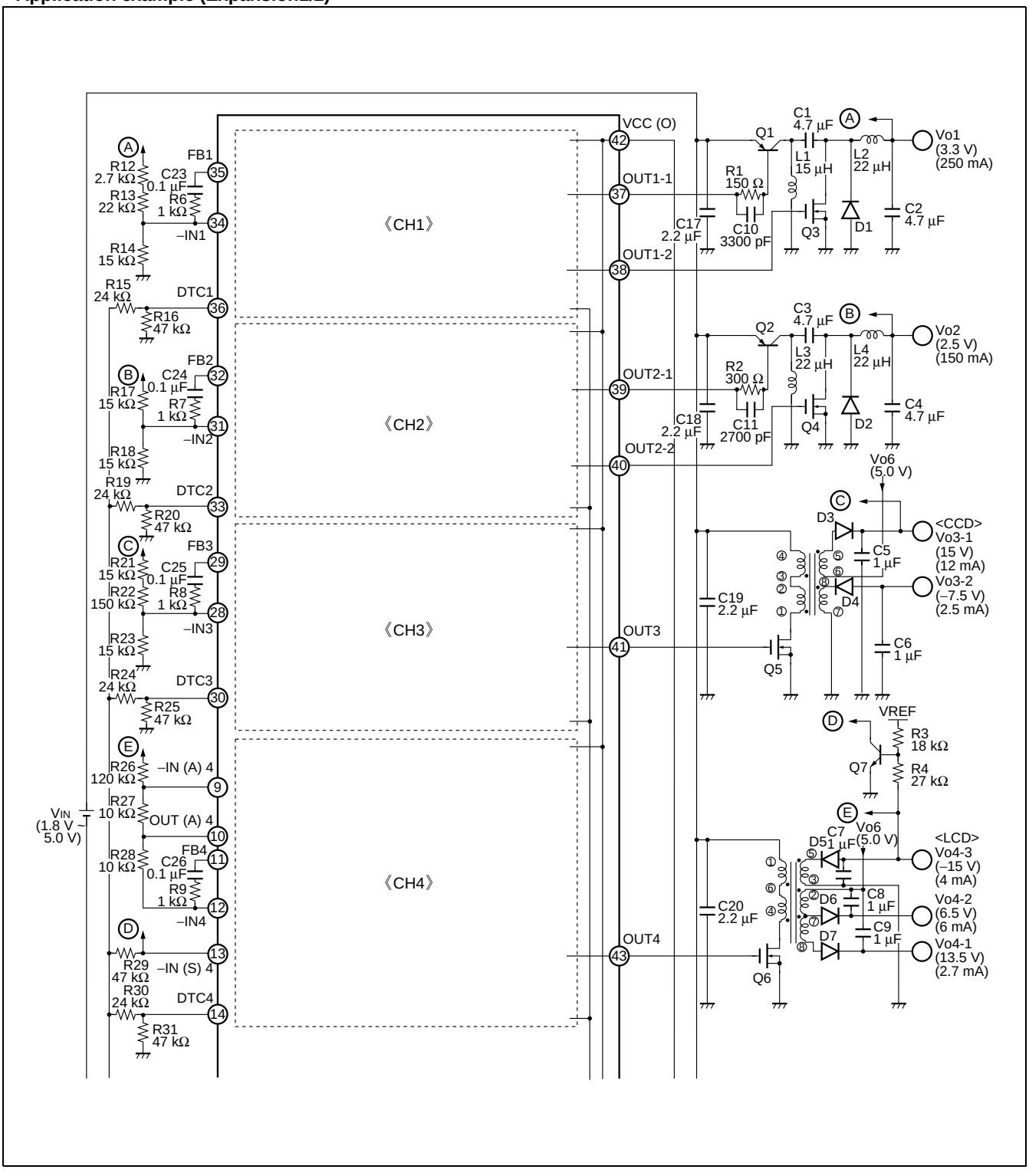


Treatment without using CH4 INV Amp.

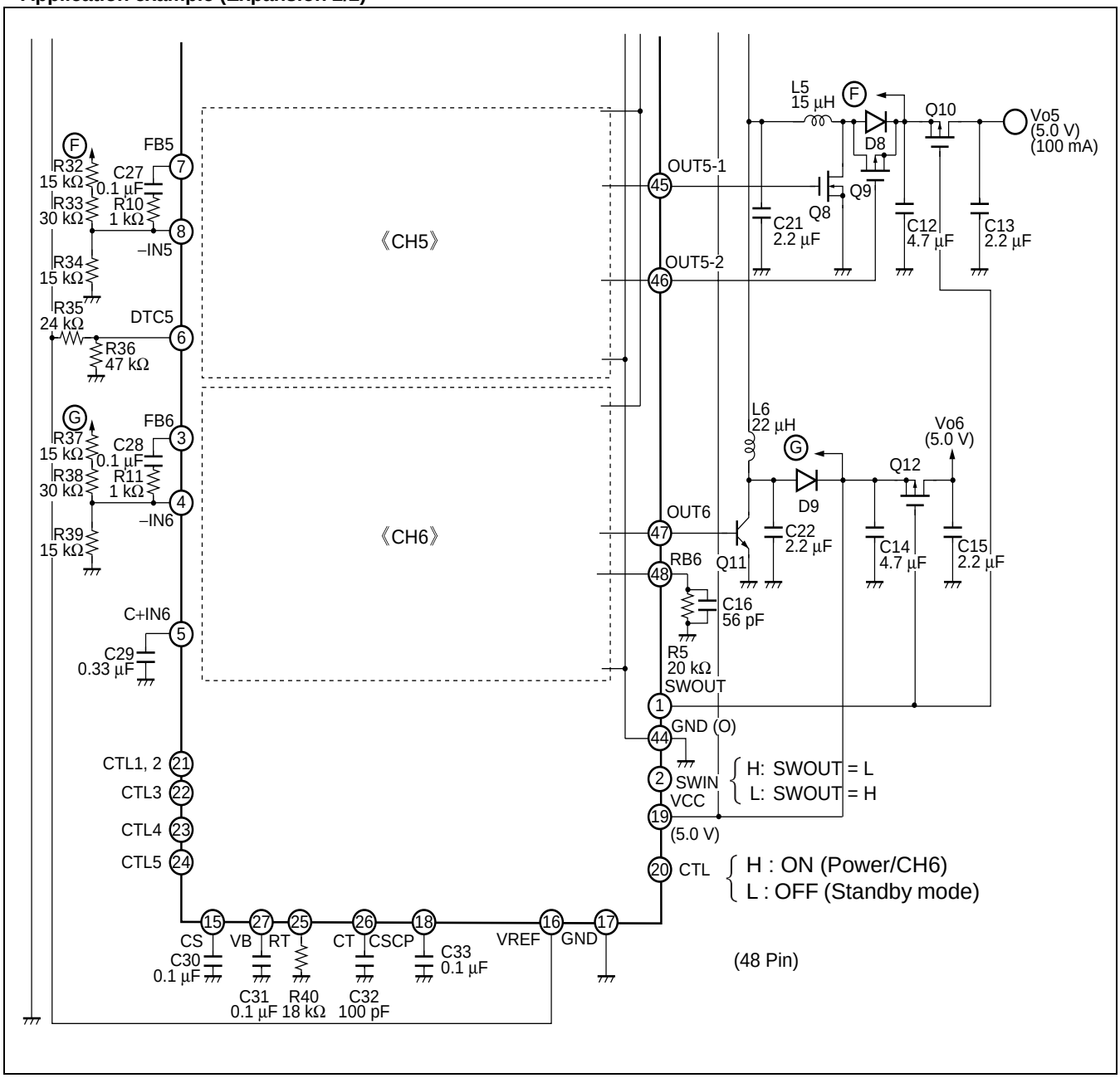
■ APPLICATION EXAMPLE



• **Application example (Expansion1/2)**



• **Application example (Expansion 2/2)**



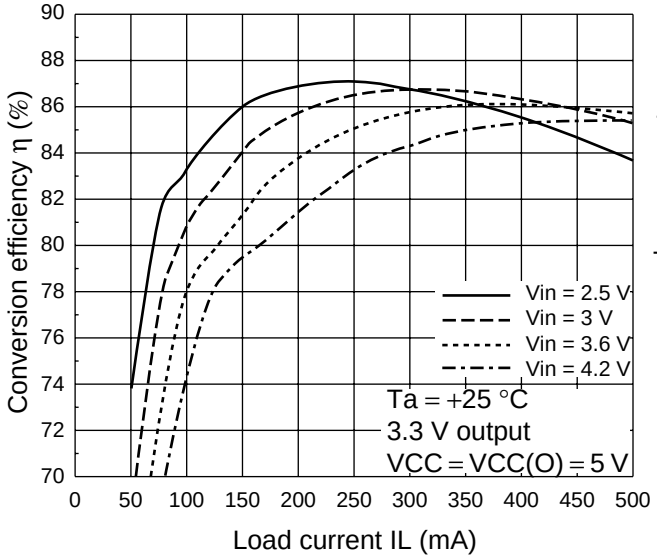
■ PARTS LIST

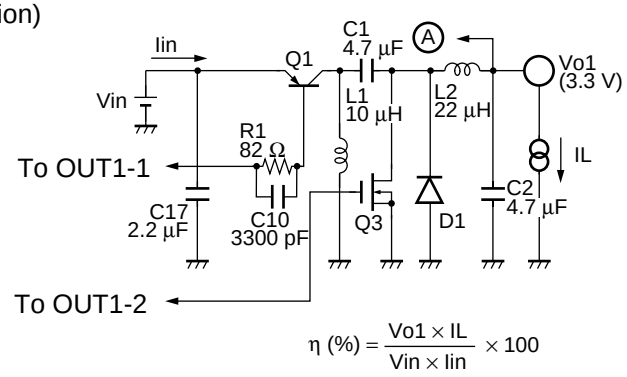
COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS NO.
Q1, Q2	PNP Tr	VCEO = –12 V		SANYO	CPH3106
Q3 to Q6, Q8	FET	VDSS = 30 V		Fairchild	NDS355AN
Q9, Q10, Q12	FET	VDSS = –20 V		SANYO	CPH3303
Q7, Q11	NPN Tr	VCEO = 15 V		SANYO	CPH3206
D1, D2, D8, D9	Diode	VF = 0.40 V (Max.) , IF = 1 A		SANYO	SBS004
D3 to D7	Diode	VF = 0.55 V (Max.) , IF = 500 mA		SANYO	SB05-05CP
L1, L5	Coil	15 µH	1 A, 74.5 mΩ	TDK	SLF6028T-150M1R0
L2 to L6	Coil	22 µH	0.77 A, 104 mΩ	TDK	SLF6028T-220MR77
C1 to C4	Ceramics Condensor	4.7 µF	10 V		
C5 to C9	Ceramics Condensor	1 µF	25 V		
C10	Ceramics Condensor	3300 pF	50 V		
C11	Ceramics Condensor	2700 pF	50 V		
C12, C14	Ceramics Condensor	4.7 µF	10 V		
C13, C15	Ceramics Condensor	2.2 µF	16 V		
C16	Ceramics Condensor	56 pF	50 V		
C17 to C22	Ceramics Condensor	2.2 µF	16 V		
C23 to C28	Ceramics Condensor	0.1 µF	16 V		
C29	Ceramics Condensor	0.33 µF	10 V		
C30, C31, C33	Ceramics Condensor	0.1 µF	16 V		
R1	Resistor	150 Ω	1/16 W		
R2	Resistor	300 Ω	1/16 W		
R3	Resistor	18 kΩ	1/16 W		
R4	Resistor	27 kΩ	1/16 W		
R5	Resistor	20 kΩ	1/16 W		
R8 to R11	Resistor	1 kΩ	1/16 W		
R12	Resistor	2.7 kΩ	1/16 W		
R13	Resistor	22 kΩ	1/16 W		
R14	Resistor	15 kΩ	1/16 W		
R15, R19, R24	Resistor	24 kΩ	1/16 W		
R16, R20, R25	Resistor	47 kΩ	1/16 W		
R17, R18, R21	Resistor	15 kΩ	1/16 W		
R22	Resistor	150 kΩ	1/16 W		
R23, R39	Resistor	15 kΩ	1/16 W		
R26	Resistor	120 kΩ	1/16 W		
R27, R28	Resistor	10 kΩ	1/16 W		
R29, R31, R36	Resistor	47 kΩ	1/16 W		
R30, R35	Resistor	24 kΩ	1/16 W		
R32, R34, 37	Resistor	15 kΩ	1/16 W		
R33, R38	Resistor	30 kΩ	1/16 W		
R40	Resistor	18 kΩ	1/16 W		

Note : SANYO : SANYO Electric Co., Ltd.
Fairchild : Fairchild Semiconductor Corporation
TDK : TDK Corporation

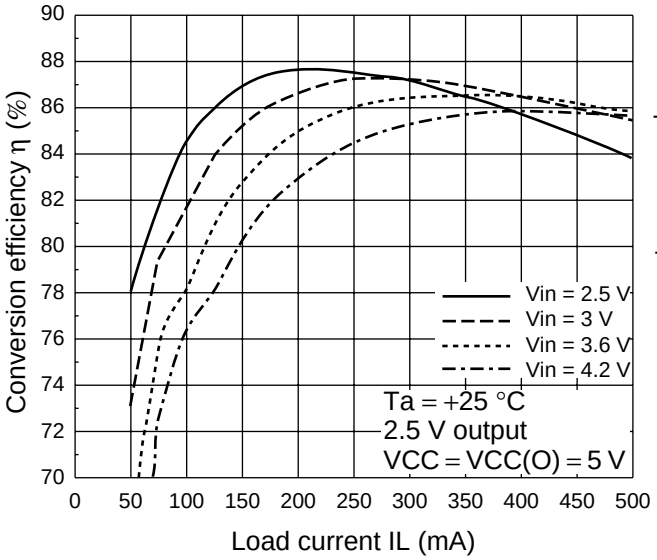
■ REFERENCE DATA

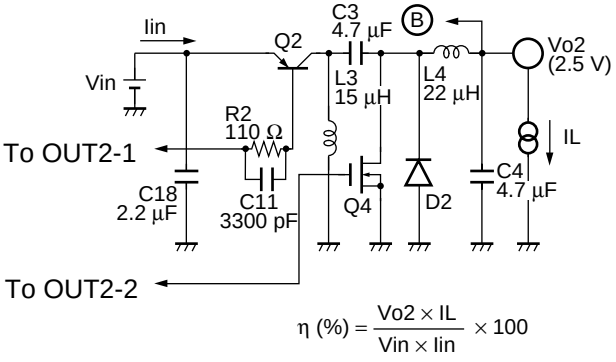
Conversion efficiency vs. load current
(CH1 : Zeta method with synchronous rectification)





Conversion efficiency vs. load current
(CH2 : Zeta method with synchronous rectification)



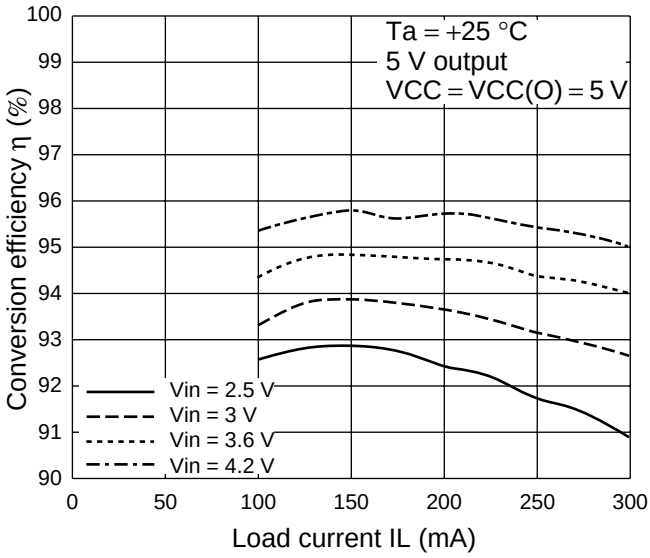


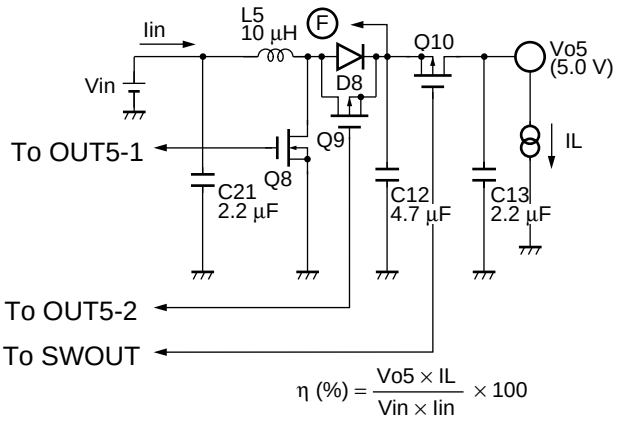
Note : The above application uses a constant of
Vin=2.5 V, with settings made at maximum load.

(Continued)

(Continued)

Conversion efficiency vs. load current
(CH5 : Up conversion method with synchronous rectification)





Note : The above application uses a constant of
Vin=2.5V, with settings made at maximum load.

■ USAGE PRECAUTION

• Printed circuit board ground lines should be set up with consideration for common impedance.

• Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

• Do not apply negative voltages.

The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

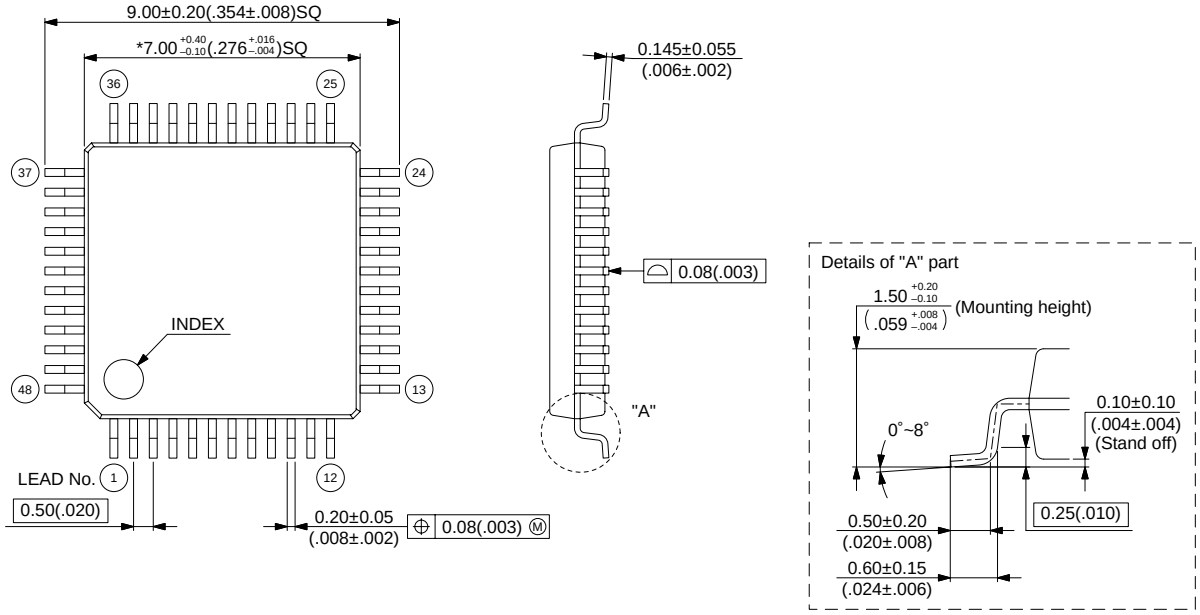
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3883PFV	48-pin plastic LQFP (FPT-48P-M05)	
MB3883PV	48-pad plastic BCC (LCC-48P-M02)	

■ PACKAGE DIMENSIONS

48-pin plastic LQFP
(FPT-48P-M05)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



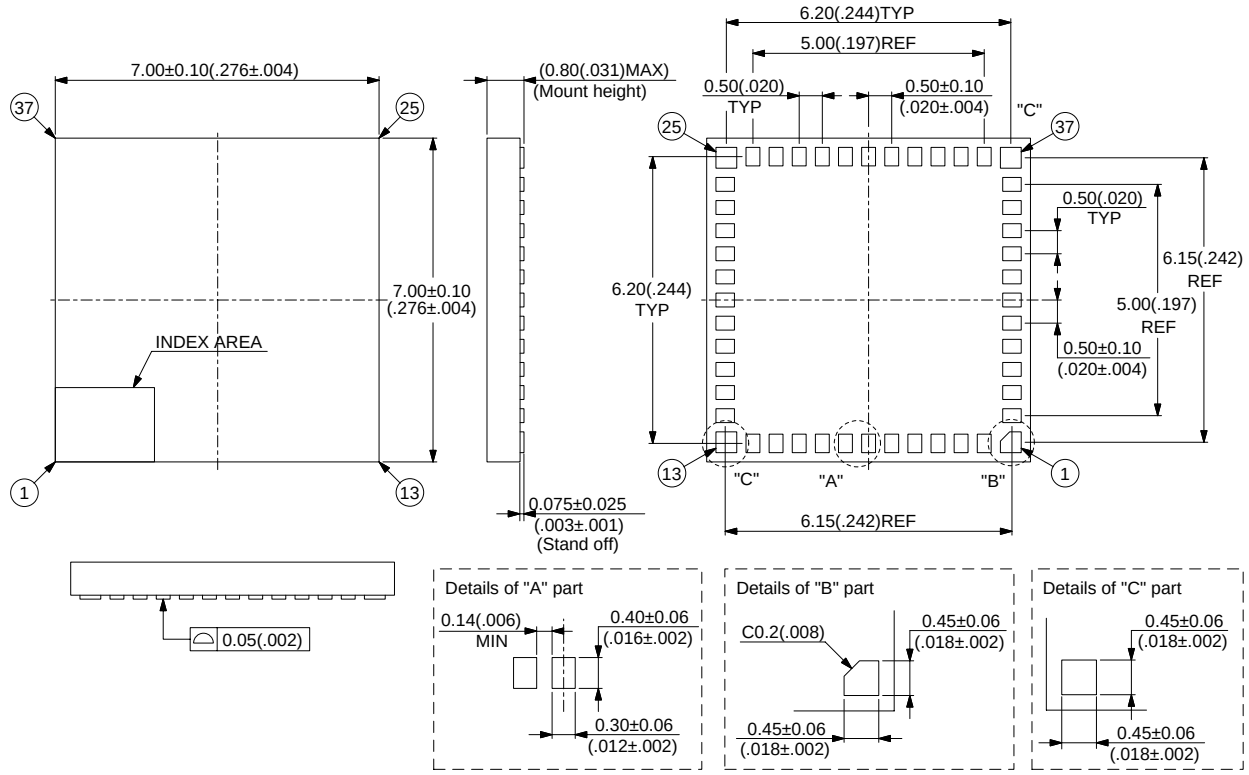
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Dimensions in mm (inches)

(Continued)

(Continued)

48-pin plastic BCC
(LCC-48P-M02)



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Dimensions in mm (inches)

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