Dual DMOS Full-Bridge Microstepping PWM Motor Driver

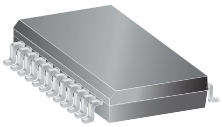
Features and Benefits

- ±1 A, 35 V Continuous Output Rating
- Low $R_{DS(on)}$ DMOS Output Drivers
- Optimized Microstepping via 6-Bit Linear DACs
- Programmable Mixed, Fast, and Slow Current Decay Modes
- 4 MHz Internal Oscillator for Digital Timing
- Serial-Interface Controls Chip Functions
- Synchronous Rectification for Low Power Dissipation
- Internal UVLO and Thermal Shutdown Circuitry
- Crossover-Current Protection
- Precision 2 V Reference
- Inputs Compatible with 3.3 or 5 V Control Signals
- Sleep and Idle Modes

Packages:



Package B, 24-pin DIP with two batwing power tabs



Package LB, 24 pin SOICW with 4 fused leads

Not to scale

Description

Designed for pulse-width modulated (PWM) current control of bipolar microstepping stepper motors, the A3973 is capable of continuous output currents to ±1 A and operating voltages to 35 V. Internal fixed off-time PWM current-control timing circuitry can be programmed via a serial interface to operate in slow, fast, and mixed current-decay modes.

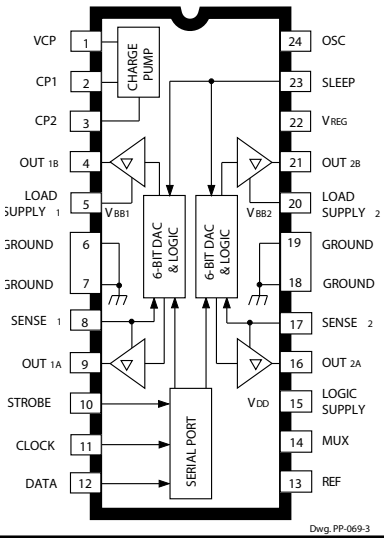
The desired load-current level is set via the serial port with two 6-bit linear DACs in conjunction with a reference voltage. The six bits of control allow maximum flexibility in torque control for a variety of step methods, from microstepping to full-step drive. Load current is set in 1.56% increments of the maximum value.

Synchronous rectification circuitry allows the load current to flow through the low $R_{DS(on)}$ of the DMOS output driver during the current decay. This feature eliminates the need for external clamp diodes in most applications, saving cost and external component count, while minimizing power dissipation.

Internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover-current protection. Special power-up sequencing is not required.

The B package is a 24-lead DIP with two copper batwing power tabs. The LB is a 24-lead SOICW with four internally fused leads for enhanced power dissipation. These power tabs and pins are at ground potential and need no electrical isolation. The A3973 B and LB packages are electrically identical.

Pin-out Diagram



Selection Guide

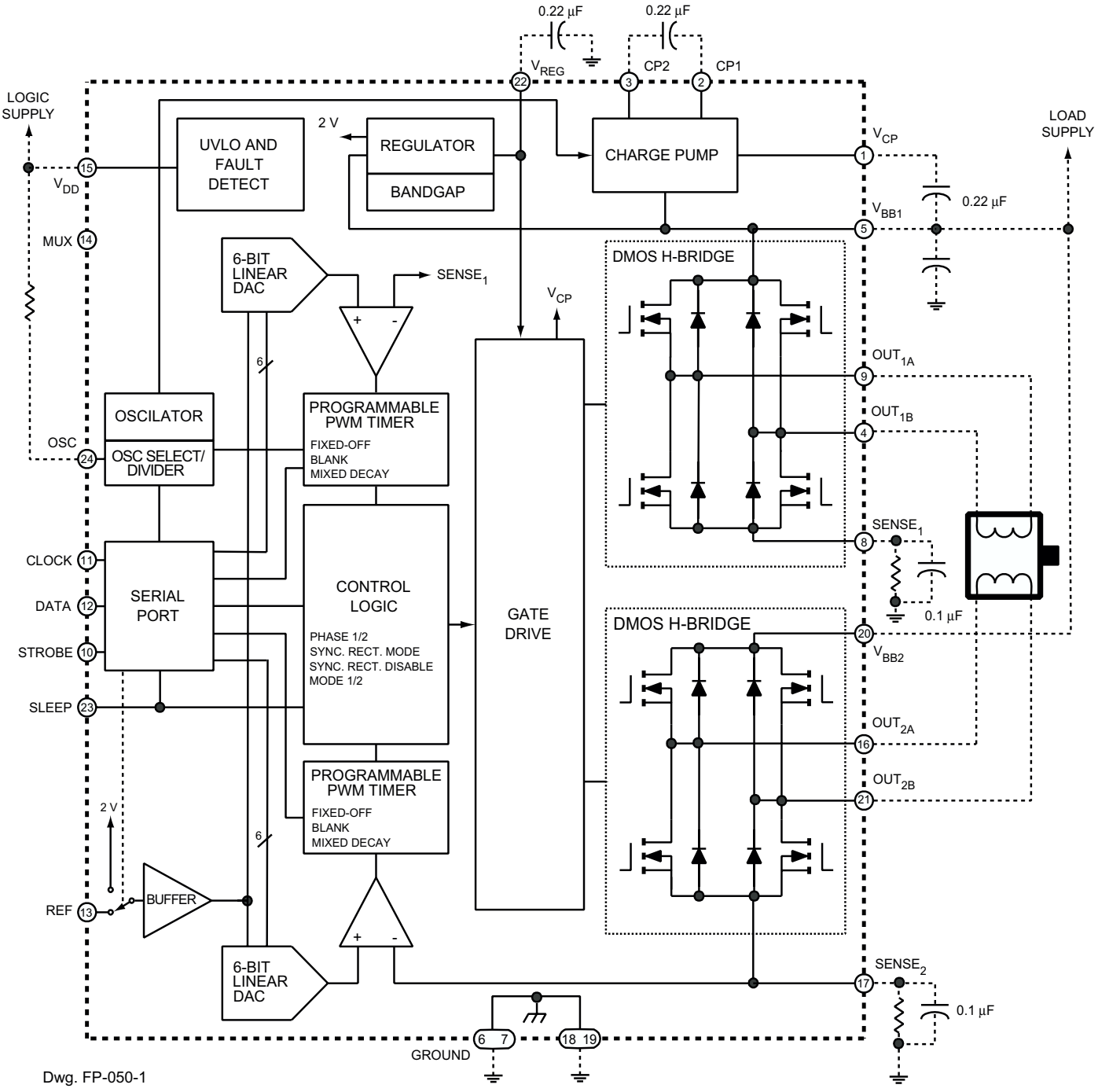
Part Number	Package	Packing
A3973SB-T	24 pin DIP with two power tabs	15 pieces per tube
A3973SLB-T	24 pin SOICW with four internally fused pins	31 pieces per tube
A3973SLBTR-T	24 pin SOICW with four internally fused pins	1000 pieces per reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		35	V
Output Current*	I_{OUT}		±1.0	A
Logic Supply Voltage	V_{DD}		7.0	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{DD} + 0.3	V
Reference Voltage	V_{REF}		3	V
Sense Voltage (DC)	V_S		500	mV
Package Power Dissipation	P_D	Package B	3.1	W
		Package LB	2.2	W
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Junction Temperature	T_J		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-050-1

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 35 V, V_{DD} = 5.0 V, V_S = 0.5 V, f_{PWM} < 50 kHz (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Load Supply Voltage Range	V_{BB}	Operating	15	—	35	V
		During sleep mode	0	—	35	V
Logic Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Load Supply Current	I_{BB}	f_{PWM} < 50 kHz	—	—	8.0	mA
		Operating, outputs disabled	—	—	6.0	mA
		Sleep or idle mode	—	—	20	µA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	—	—	12	mA
		Outputs off	—	—	10	mA
		Idle mode (D0 = 1, D18 = 0)	—	—	1.5	mA
		Sleep mode	—	—	100	µA
Output Drivers						
Output Leakage Current	I_{DSS}	V_{OUT} = V_{BB}	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<-1.0	-50	µA
Output On Resistance	$r_{DS(on)}$	Source driver, I_{OUT} = –1.0 A	—	0.54	0.60	Ω
		Sink driver, I_{OUT} = 1.0 A	—	0.54	0.60	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = 1.0 A	—	—	1.2	V
		Sink diode, I_F = 1.0 A	—	—	1.2	V
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-20	µA
OSC Input Frequency Range	f_{OSC}	Divide by one (D0 =1, D13 = 0, D14 = 1)	2.5	—	6.0	MHz
OSC Input Duty Cycle	—		40	—	60	%
Input Hysterisis	ΔV_{IN}		0.20	—	0.40	V

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 35 V, V_{DD} = 5.0 V, V_S = 0.5 V, f_{PWM} < 50 kHz (unless otherwise noted).

Characteristics	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic (continued)						
Internal Oscillator	f_{OSC}	OSC shorted to ground	3.0	4.0	5.0	MHz
		R_{OSC} = 51 kΩ	3.4	4.0	4.6	MHz
DAC Accuracy (total error)	E_T	Relative to DAC reference buffer output, D0 = 0, D17 = 0	—	±1/2	—	LSB
Reference Input Voltage Range	$V_{REF(EXT)}$		0.5	—	2.6	V
Reference Buffer Offset	V_{OS}		—	±10	—	mV
Reference Divider Ratio	V_{REF}/V_S	D0 = 0, D18 = 0	—	8.0	—	—
		D0 = 0, D18 = 1	—	4.0	—	—
Reference Input Current	I_{REF}	V_{REF} = 2.0 V	—	—	±0.5	µA
Internal Reference Voltage	$V_{REF(INT)}$		1.94	2.0	2.06	V
Gain (G_m) Error (note 3)	E_G	D0 = 0, D17 = 0,				
		D18 = 0, DAC = 63	—	0	±6	%
		D18 = 0, DAC = 31	—	0	±9	%
		D18 = 1, DAC = 63	—	0	±6	%
		D18 = 1, DAC = 15	—	0	±10	%
Comparator Input Offset Voltage	V_{IO}	V_{REF} = 0 V	—	±5.0	—	mV
Propagation Delay Times	t_{pd}	50% to 90%:				
		PWM change to source on	500	800	1200	ns
		PWM change to source off	50	150	350	ns
		PWM change to sink on	500	800	1200	ns
		PWM change to sink off	50	150	350	ns
Crossover Dead Time	t_{dt}		300	700	900	ns
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{DD}	3.9	4.2	4.45	V
UVLO Hysteresis	ΔV_{UVLO}		0.05	0.10	—	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. $E_G = [(V_{REF}/\text{Range}) - V_S]/(V_{REF}/\text{Range})$.

FUNCTIONAL DESCRIPTION

Serial Interface. The A3973SB/SLB is controlled via a 3-wire (clock, data, strobe) serial port. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is written as two 19-bit words: 1 bit to select the word and 18 bits of data. The serial data is clocked in starting with D18.

Word 0 Bit Assignments

Bit	Function
D0	Word select = 0
D1	Bridge 1, DAC, LSB
D2	Bridge 1, DAC, bit 2
D3	Bridge 1, DAC, bit 3
D4	Bridge 1, DAC, bit 4
D5	Bridge 1, DAC, bit 5
D6	Bridge 1, DAC, MSB
D7	Bridge 2, DAC, LSB
D8	Bridge 2, DAC, bit 2
D9	Bridge 2, DAC, bit 3
D10	Bridge 2, DAC, bit 4
D11	Bridge 2, DAC, bit 5
D12	Bridge 2, DAC, MSB
D13	Bridge 1 phase
D14	Bridge 2 phase
D15	Bridge 1 mode
D16	Bridge 2 mode
D17	REF select
D18	Range select

D1 – D6 Bridge 1 Linear DAC. Six-bit word sets desired current level for Bridge 1. Setting all six bits to zero disables Bridge 1, with all drivers off (See current regulation section of functional description).

D7 – D12 Bridge 2 Linear DAC. Six-bit word sets desired current level for Bridge 2. Setting all six bits to zero disables Bridge 2, with all drivers off (See current regulation section of functional description).

D13 Bridge 1 Phase. This bit controls the direction of output current for Load 1.

D13	OUT_{1A}	OUT_{1B}
0	L	H
1	H	L

D14 Bridge 2 Phase. This bit controls the direction of output current for Load 2.

D14	OUT_{2A}	OUT_{2B}
0	L	H
1	H	L

D15 Bridge 1 Mode.

D15	Mode
0	Mixed-decay
1	Slow-decay

D16 Bridge 2 Mode.

D16	Mode
0	Mixed-decay
1	Slow-decay

D17 REF Select. This bit determines the reference input for the 6-bit linear DACs.

D17	Reference Voltage
0	Internal 2 V
1	External (3 V max)

D18 G_m Range Select. This bit determines the scaling factor (4 or 8) used.

D18	Divider	Load Current
0	1/8	$I_{TRIP} = V_{DAC}/8R_S$
1	1/4	$I_{TRIP} = V_{DAC}/4R_S$

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FUNCTIONAL DESCRIPTION (continued)

Word 1 Bit Assignments

Bit	Function
D0	Word select = 1
D1	Blank-time LSB
D2	Blank-time MSB
D3	Off-time LSB
D4	Off-time bit 1
D5	Off-time bit 2
D6	Off-time bit 3
D7	Off-time MSB
D8	Fast-decay time LSB
D9	Fast-decay time bit 1
D10	Fast-decay time bit 2
D11	Fast-decay time MSB
D12	C0 oscillator control
D13	C1 oscillator control
D14	SR control bit 1
D15	SR control bit 2
D16	Reserved for testing
D17	Reserved for testing
D18	Idle mode

D1 – D2 Blank Time. These two bits set the blank time for the current-sense comparator. When a source driver turns on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source-enable latch, the sense comparator is blanked. The blank timer runs after the off-time counter to provide the programmable blanking function. The blank timer is reset when PHASE is changed.

D2	D1	Time
0	0	$4/f_{OSC}$
0	1	$6/f_{OSC}$
1	0	$8/f_{OSC}$
1	1	$12/f_{OSC}$

D3 – D7 Fixed Off Time. These five bits set the fixed off-time for the internal PWM control circuitry. Fixed off-time is defined by:

$$t_{off} = [(1 + N) \times 8/f_{OSC}] - 1/f_{OSC}$$

where N = 0….31

For example, with a master oscillator frequency of 4 MHz, the fixed-off time will be adjustable from 1.75 µs to 63.75 µs in increments of 2 µs.

D8 – D11 Fast Decay Time. These four bits set the fast-decay portion of fixed off-time for the internal PWM control circuitry. The fast-decay portion is defined by:

$$t_{fd} = [(1 + N) \times 8/f_{OSC}] - 1/f_{OSC}$$

where N = 0….15

For example, with an oscillator frequency of 4 MHz, the fast-decay time will be adjustable from 1.75 µs to 31.75 µs in increments of 2 µs. For $t_{fd} > t_{off}$, the device will effectively operate in fast-decay mode.

D12 – D13 Oscillator Control. A 4 MHz internal oscillator is used for the timing functions and charge-pump clock. If more precise control is required, an external oscillator can be input to the OSC terminal. To accommodate a wider range of system clocks, an internal divider is provided to generate the desired MO frequency according to the following table:

D13	D12	OSC
0	0	4 MHz internal clock
0	1	External clock
1	0	External clock/2
1	1	External clock/4

D14 – D15 Synchronous Rectification.

D15	D14	Synchronous Rectifier
0	0	Active
0	1	Disabled
1	0	Passive
1	1	Low side only

The different modes of operation are in the synchronous rectification section of the functional description.

D16, D17. These bits are reserved for testing and should be programmed to zero during normal operation.

D18 Idle Mode. The device can be placed in a low power "idle" mode by writing a "0" to D18. The outputs will be disabled, the charge pump will be turned off, and the device will draw a lower load supply currrent. The undervoltage monitor circuit will remain active. D18 should be programmed high for 1 ms before attempting to enable any output driver.

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FUNCTIONAL DESCRIPTION (continued)

V_{REG}. This internally generated supply voltage is used to run the sink-side DMOS outputs. V_{REG} is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The V_{REG} pin should be decoupled with a 0.22 µF capacitor to ground.

Current Regulation. The reference voltage can be set by analog input to the REF terminal, or via the internal 2 V precision reference. The choice of reference voltage and sense resistor set the maximum trip current.

$$I_{TRIPMAX} = V_{REF}/(\text{Range} \times R_S)$$

Microstepping current levels are set according to the following equations:

$$I_{TRIP} = V_{DAC}/(\text{Range} \times R_S)$$

$$V_{DAC} = [(1 + \text{DAC}) \times V_{REF}]/64$$

where DAC input code equals 1 to 63 and Range is 4 or 8 as selected by Word 0, D18. Programming the DAC input code to zero disables the bridge, and results in minimum load current.

PWM Timer Function. The PWM timer is programmable via the serial port to provide fixed off-time PWM signals to the control block. In mixed-decay mode, the first portion of the off time operates in fast decay, until the fast-decay time count is reached, followed by slow decay for the rest of the fixed off-time period. If the fast-decay time is set longer than the off-time, the device effectively operates in fast-decay mode.

Oscillator. The PWM timer is based on an oscillator input, typically 4 MHz. The A3973SB/SLB can be configured to select either a 4 MHz internal oscillator or, if more precision is required, an external clock can be connected to the OSC terminal. If an external clock is used, three internal divider choices are selectable via the serial port to allow flexibility in choosing f_{OSC}, based on available system clocks. If the internal oscillator option is used, the absolute accuracy is dependent on the process variation of resistance and capacitance. A precision resistor can be connected from the OSC terminal to V_{DD} to further improve the tolerance. The frequency will be:

$$f_{OSC} = 204 \times 10^9/R_{OSC}$$

If the internal oscillator is used without the external resistor, the OSC terminal should be connected to ground.

Sleep Mode. The input terminal SLEEP is dedicated to putting the device into a minimum current draw mode. When pulled low, the serial port will be reset to all zeros and all circuits will be disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on V_{CP} or V_{REG}, the outputs of the device are disabled until the fault condition is removed. At power up, or in the event of low V_{DD}, the UVLO circuit disables the drivers and resets the data in the serial port to zeros.

Synchronous Rectification. When a PWM off-cycle is triggered, either by a bridge disable command or internal fixed off-time cycle, the load current will recirculate according to the decay mode selected by the control logic. The A3973SB/SLB synchronous rectification feature will turn on the appropriate MOSFET(s) during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This will lower power dissipation significantly and can eliminate the need for external Schottky diodes for most applications.

Four distinct modes of operation can be configured with the two serial port control bits:

1. **Active Mode**. Prevents reversal of load current by turning off synchronous rectification when a zero current level is detected.
2. **Passive Mode.** Allows reversal of current but will turn off the synchronous rectifier circuit if the load current inversion ramps up to the current limit.
3. **Disabled.** MOSFET switching will not occur during load recirculation. This setting would only be used with four external clamp diodes per bridge.
4. **Low Side Only.** The low-side MOSFETs will switch on during the off time to short out the current path through the MOSFET body diode. With this setting, the high-side MOSFETs will not synchronously rectify so four external diodes from output to supply are recommended. This mode is intended for use with high-power applications where it is desired to save the expense of two external diodes per bridge. In this mode, the sink-side MOSFETs are chopped during the PWM off time. In all other cases, the source-side MOSFETs are chopped in response to a PWM off command.

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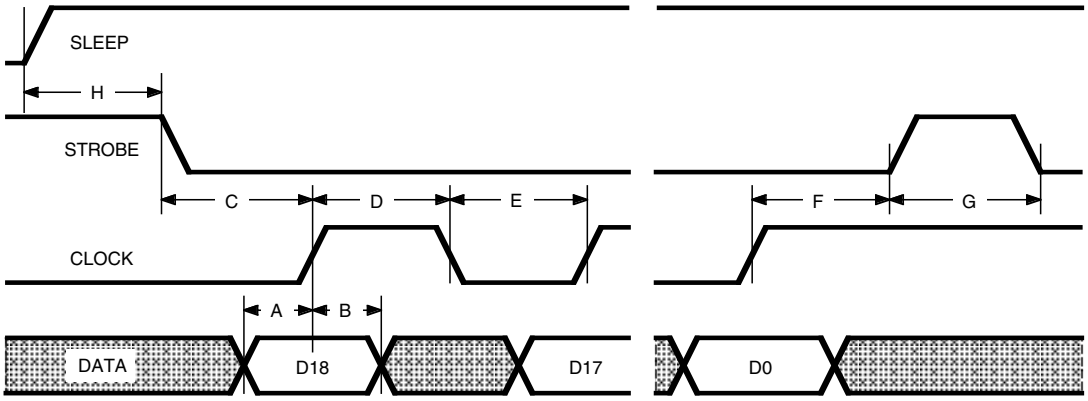
APPLICATIONS INFORMATION

Current Sensing. To minimize inaccuracies in sensing the I_{PEAK} current level caused by ground-trace IR drops, the sense resistor should have an independent ground return to the ground terminal of the device. For low-value sense resistors, the IR drops in the sense resistor's PCB traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

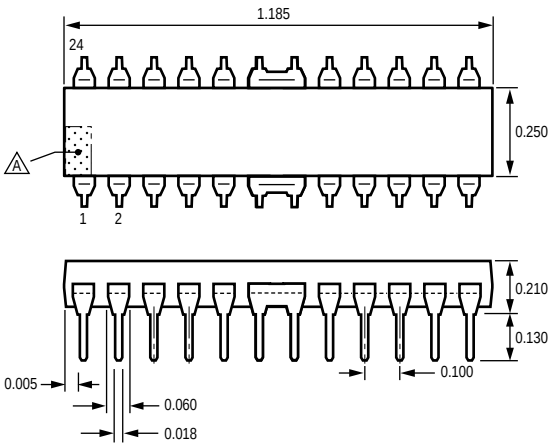
Serial Port Write Timing Operation. Data is clocked into a shift register on the rising edge of CLOCK signal. Normally, STROBE will be held high, and only will be brought low to initiate a write cycle. The data is written MSB first, followed by the word-select bit. Refer to serial port diagram for timing requirements.

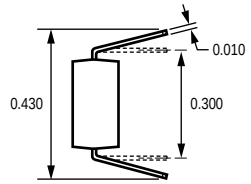
Layout. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance, the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to the ground pin(s) of the driver. This path should be as short as physically possible and should not have any other components connected to it. The load supply pin, V_{BB}, should be decoupled with an electrolytic capacitor (>47 µF is recommended) placed as close to the driver as is possible.



A. Minimum Data Setup Time.....15 ns
B. Minimum Data Hold Time .....10 ns
C. Minimum Setup Strobe to Clock Rising Edge.....150 ns
D. Minimum Clock High Pulse Width.....40 ns
E. Minimum Clock Low Pulse Width.....40 ns
F. Minimum Setup Clock Rising Edge to Strobe.....50 ns
G. Minimum Strobe Pulse Width.....150 ns
H. Minimum Setup Sleep to Strobe falling.....50 µs

B Package, 24-Pin DIP



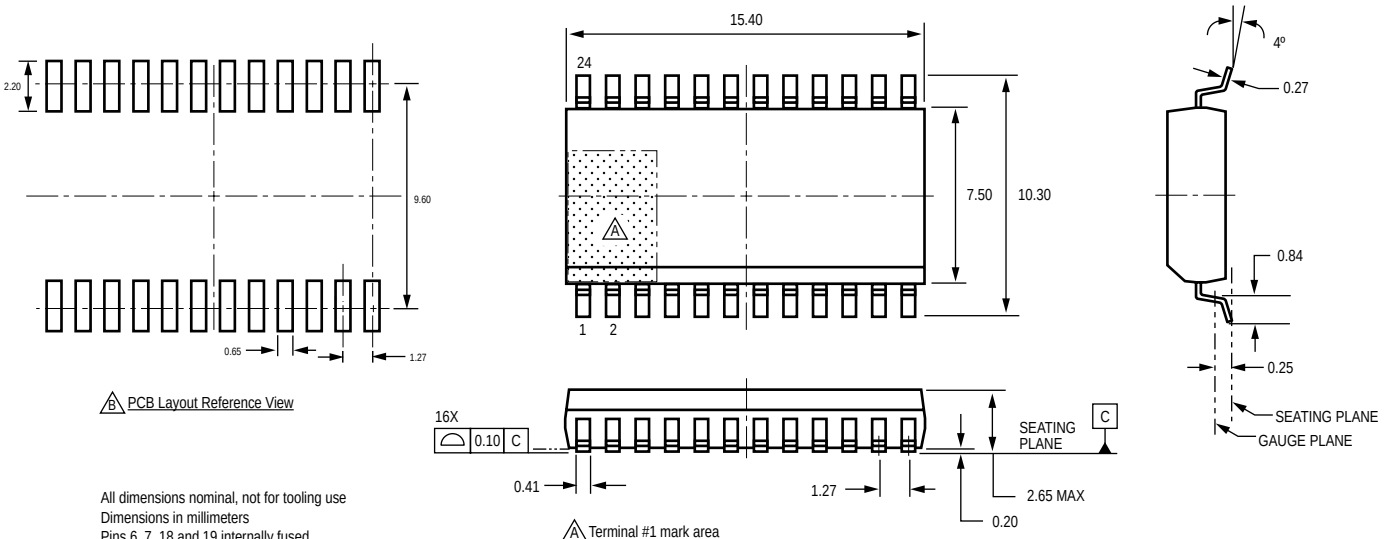


All dimensions nominal, not for tooling use
(reference JEDEC MS-001 BE)
Dimensions in inches
Pins 6, 7, 18 and 19 internally fused

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

LB Package, 24-Pin SOICW



All dimensions nominal, not for tooling use
Dimensions in millimeters
Pins 6, 7, 18 and 19 internally fused
(Reference JEDEC MS-013 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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