Contents

Features 1
Pin Assignment 1
Pin Functions 1
Block Diagram 2
Instruction Set 2
Absolute Maximum Ratings 2
Recommended Operationg Conditions 3
Pin Capacitance 3
Endurance 3
DC Characteristics 4
AC Characteristics 5
Operation 6
Receiving a Start-Bit 9
Three-wire Interface
(DI-DO direct connection) 9
Connecting to CPU with a Serial Port 10
Dimensions (Unit : mm) 11
Ordering Information 11
Characteristics 12

CMOS SERIAL E^2PROM

S-29X90A Series

The S-29X90A Series is high speed, low power 1K/2K/4K-bit serial E^2PROM with a wide operating voltage range. They are organized as 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented for each 16-bit block.
Interface is structured so that this IC can be directly connected to the CPU with serial ports. 8-bit instructions make it easy to prepare your own software.

■ Features

- Low power consumption
  Standby : 1.0 μA Max. (Vcc = 6.5 V)
  Operating : 0.8 mA Max. (Vcc = 5.5 V)
  0.4 mA Max. (Vcc = 2.5 V)
- Wide operating voltage range
  Write : 2.5 to 6.5 V
  Read : 1.8 to 6.5 V
- Sequential read capable
- Can be easily connected to the serial port
- Endurance : 10^5 cycles/word
- Data retention : 10 years
- S-29190A : 1 Kbits
- S-29290A : 2 Kbits
- S-29390A : 4 Kbits

■ Pin Assignment

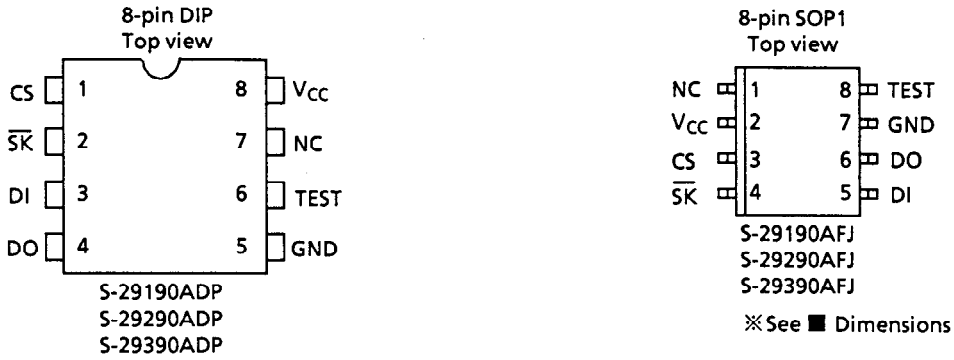


Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP1	
CS	1	3	Chip select input
SK	2	4	Serial clock input
DI	3	5	Serial data input
DO	4	6	Serial data output
GND	5	7	Ground
TEST	6	8	Test: Normally kept open (can also be connected to GND or Vcc)
NC	7	1	No Connection
Vcc	8	2	Power supply

■ Block Diagram

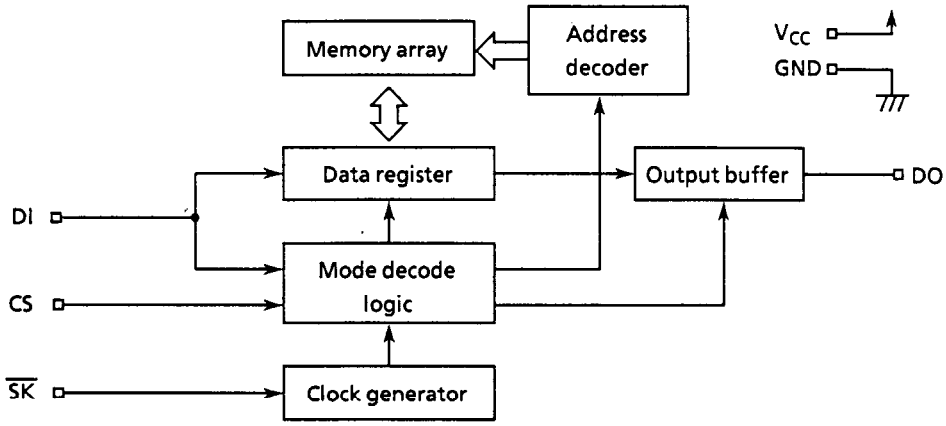


Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	Address			Data
			S-29190A	S-29290A	S-29390A	
READ (Read data)	1	1000xxx	xx A5 to A0	x A6 to A0	A7 to A0	D_{15} to D_0 Output*
PROGRAM (Program data)	1	x 100 xxx	xx A5 to A0	x A6 to A0	A7 to A0	D_{15} to D_0 Input
WRAL (Write all)	1	0001xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	D_{15} to D_0 Input
ERAL (Erase all)	1	0010xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PEN (Program enable)	1	0011xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PDS (Program disable)	1	0000xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—

x : Doesn't matter.

*: When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	− 0.3 to + 7.0	V
Input voltage	V_{IN}	− 0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	− 0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	− 50 to + 95	°C
Storage temperature	T_{stg}	− 65 to + 150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation Write Enable/Disable	1.8	—	6.5	V
		Write Operation	2.5	—	6.5	V
High level input voltage	V_{IH}	V_{CC} = 5.5 to 6.5 V	0.8 × Vcc	—	Vcc	V
		V_{CC} = 4.5 to 5.5 V	2.0	—	Vcc	V
		V_{CC} = 2.7 to 4.5 V	0.8 × Vcc	—	Vcc	V
		V_{CC} = 1.8 to 2.7 V	0.8 × Vcc	—	Vcc	V
Low level input voltage	V_{IL}	V_{CC} = 5.5 to 6.5 V	0.0	—	0.2 × Vcc	V
		V_{CC} = 4.5 to 5.5 V	0.0	—	0.8	V
		V_{CC} = 2.7 to 4.5 V	0.0	—	0.2 × Vcc	V
		V_{CC} = 1.8 to 2.7 V	0.0	—	0.15 × Vcc	V
Operating temperature	T_{opr}		− 40	—	+ 85	°C

■ Pin Capacitance

Table 5

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Characteristics

Table 7

Parameter	Smbl	Conditions	V_{CC} = 5.5 V to 6.5 V			V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	1.0	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	2.5	—	—	2.0	—	—	1.5				mA

Table 8

Parameter	Smbl	Conditions	V_{CC} = 4.5 V to 6.5 V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	CS = GND DO = Open Other input: Connected to V_{CC} or GND	—	—	1.0	—	—	0.6	—	—	0.4	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.45							V
		I_{OL} = 100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = -400 μA	2.4	—	—							V
		I_{OH} = -100 μA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—				V
		I_{OH} = -10 μA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when program disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V

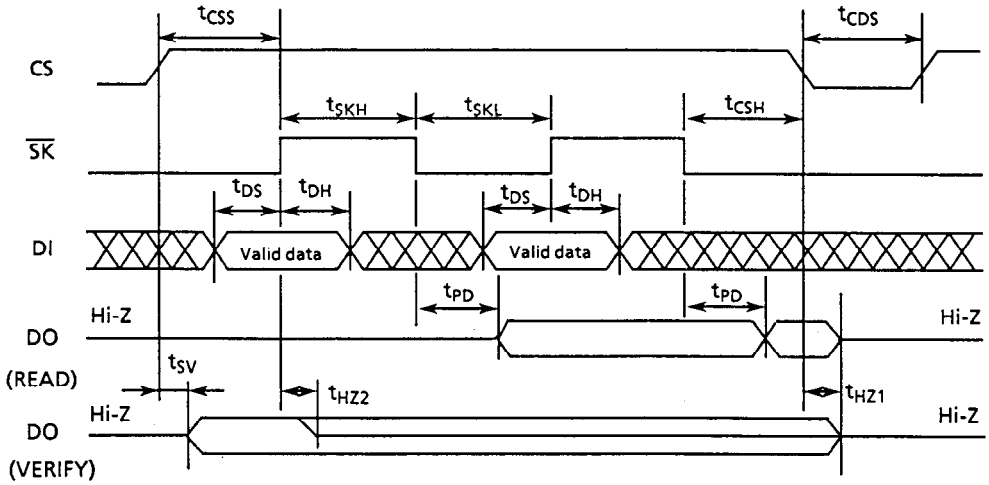
■ AC Characteristics

Table 9 Measuring conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

Table 10

Parameter	Smbl	V_{CC} = 4.5 to 6.5V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.8 to 2.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	μs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Output delay time	t_{PD}	—	—	0.4	—	—	1.0	—	—	2.0	μs
Clock frequency	f_{SK}	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	t_{SKH} t_{SKL}	0.25	—	—	1.0	—	—	2.0	—	—	μs
Output disable time	t_{HZ1} t_{HZ2}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Output enable time	t_{SV}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Programming time	t_{PR}	—	4.0	10.0	—	4.0	10.0				ms



Input data is retrieved on the rising edge of $\overline{SK}$.
Output data is triggered on the falling edge of $\overline{SK}$.

Figure 3 Timing Chart

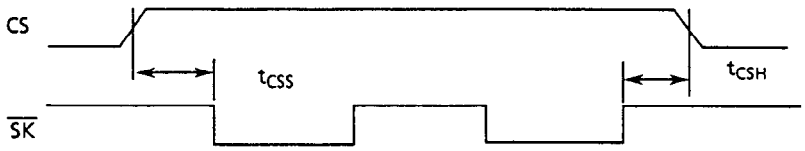


Figure 4 Timing Chart for t_{CSS} and t_{CSH} when $\overline{SK}$ is "H"

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of $\overline{SK}$ after CS goes high. A start-bit can only be recognized when the high of DI is latched at the rising edge of $\overline{SK}$ after changing CS to high, it is impossible for it to be recognized as long as DI is low, even if there are $\overline{SK}$ pulses after CS goes high. Instruction finishes when CS goes low, where it must be low between commands during t_{CDS}.

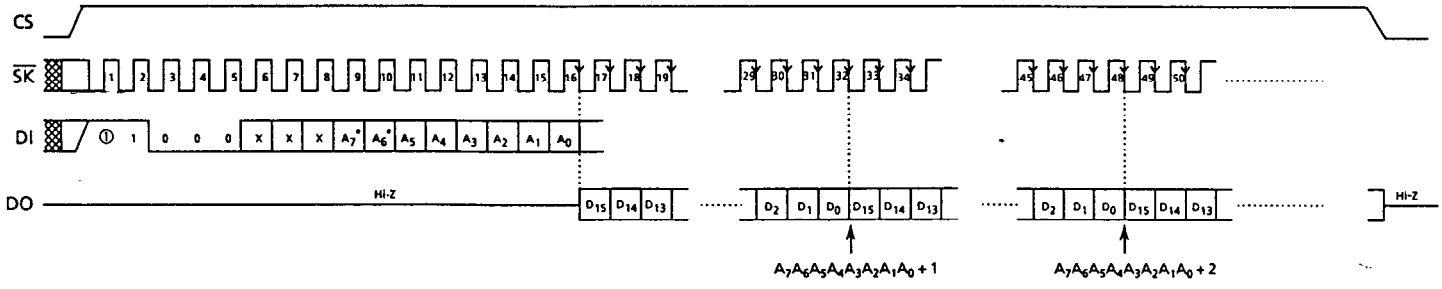
All input, including DI and $\overline{SK}$ signals, is ignored while CS is low, which is stand-by mode. The start bit + instruction, address, and data are 8-bit instructions. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. After A0 is latched at the rising edge of $\overline{SK}$, 16-bit data is continuously output in synchronization with the falling edge of $\overline{SK}$.

When all of the data (D_{15} to D_0) in the specified address has been read, data in the next address can be read with the input of another $\overline{SK}$ clock. Thus, the data over whole area of the memory can be read by continuously inputting $\overline{SK}$ clocks as long as CS is high.

The last address (An ··· A1 A0 = 1 ··· 11) rolls over to the top address (An ··· A1 A0 = 0 ··· 00).



* On the S-29190A, A_7 and A_6 are optional.
On the S-29290A, A_7 is optional.

Figure 5 Read Timing (S-29390A)

2. Write (PROGRAM ,WRAL, ERAL)

The write instructions (PROGRAM, WRAL, ERAL) automatically begins writing to the non-volatile memory when CS goes low at the completion of the specified clock input.

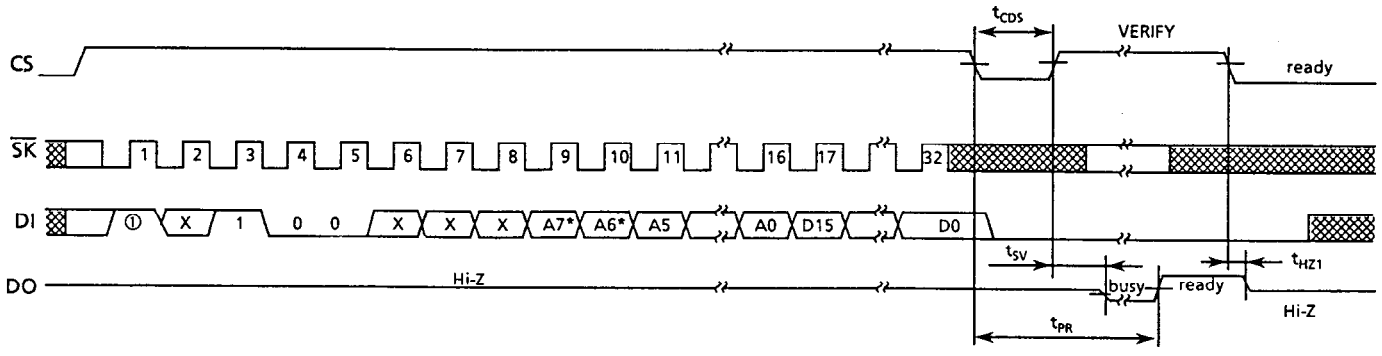
The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29X90A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting CS to high and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again. There are two methods to detect a change in the DO output. One is to detect a change from low to high setting CS to high, and the other is to detect a change from low to high as a result of repetitous operations of returning the CS to low after setting CS to high and checking the DO output.

Because all $\overline{SK}$ and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedance state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedance state upon the recognition of a high of DI (start-bit) attached to the rising edge of an $\overline{SK}$ pulse.

DI input should be low during the VERIFY procedure.

2.1 PROGRAM

This instruction writes 16-bit data to a specified address.
After changing CS to high, input a start-bit, op-code (PROGRAM), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing CS to low will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.



* On the S-29190A, A_7 and A_6 are optional.
On the S-29290A, A_7 is optional.

Figure 6 WRITE Timing (S-29390A)

2.2 Write all (WRAL)

This instruction writes the same 16-bit data into every address.
After changing CS to high, input a start-bit, op-code (WRAL), address (optional), and 16-bit data. If there is a data overflow of more than 16 bits, the write data is shifted for every clock in succession and only the last 16-bit data is valid. Changing CS to low starts the WRAL operation. It is not necessary to make the data "1" before initiating the WRAL operation.

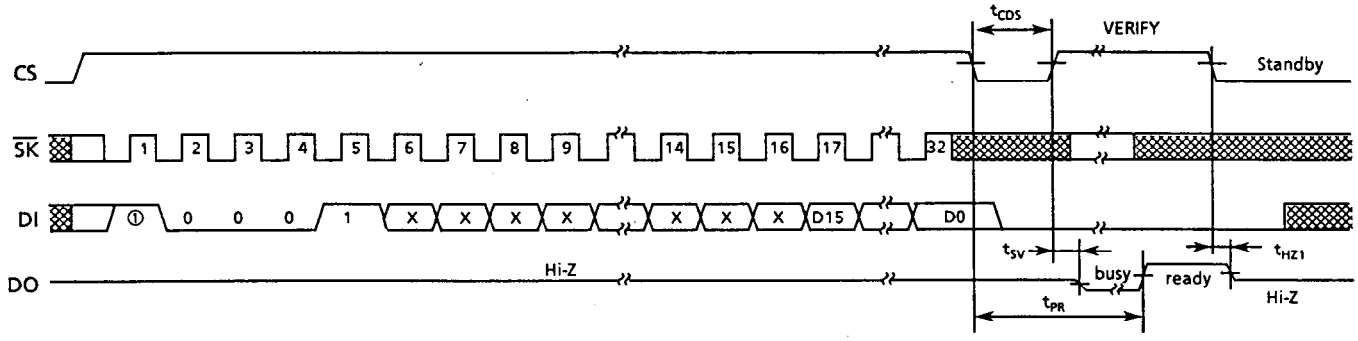


Figure 7 WRAL Timing

2.3 Erase all (ERAL)

This instruction erases the data in every address. All data changes to "1."
After changing CS to high, input a start-bit, op-code (ERAL), and address (optional) . It is not necessary to input data. Changing CS to low starts the ERAL operation.

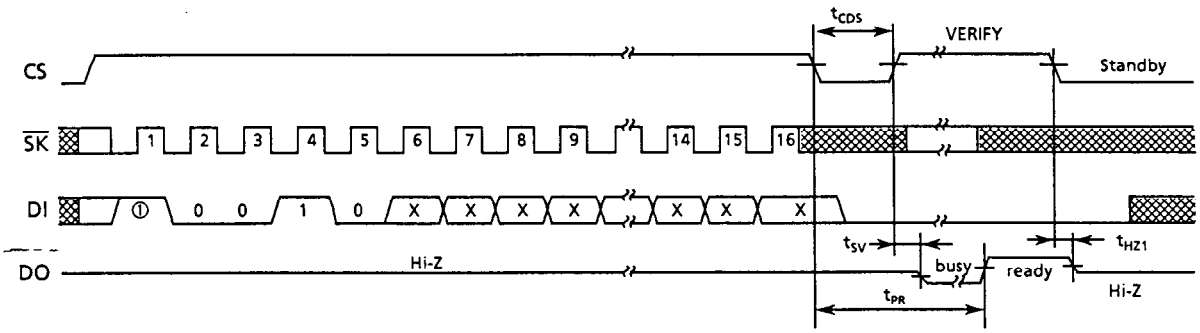


Figure 8 ERAL Timing

3. Write enable (PEN) and Write disable (PDS)

The PEN instruction puts the S-29X90A Series into write enable mode, which accepts PROGRAM, WRAL, and ERAL instruction. The PDS instruction puts the S-29X90A Series into write disable mode, which refuses PROGRAM, WRAL, and ERAL instruction.
The S-29X90A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

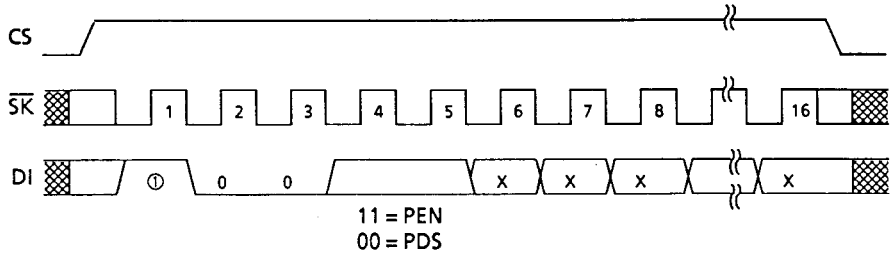


Figure 9 PEN/PDS Timing

■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of $\overline{SK}$ after changing CS to high (Start-Bit Recognition). The write operation begins by inputting the write instruction and setting CS to low. The DO pin then outputs low during the write operation and high at its completion by setting CS to high (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having CS go high, the DO pin is switched from a state of high-impedance to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedance (see Figure 3).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

■ Three-Wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to CS, $\overline{SK}$, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI(See Figure 10).

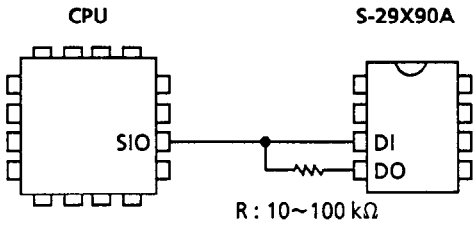


Figure 10 3-wire interface

■ Connecting to the CPU with Serial Port

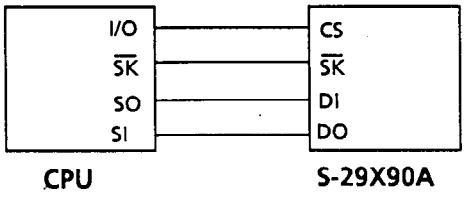


Figure 11 Connectin Example

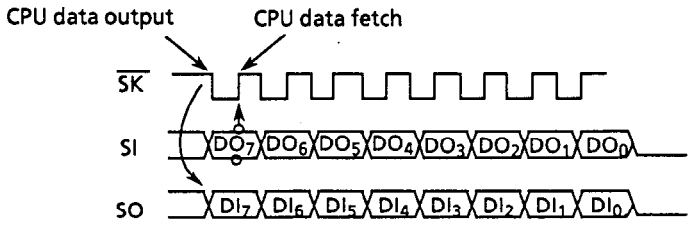


Figure 12 Serial Shift Timing

■ Dimensions (Unit : mm)

1. 8-pin DIP

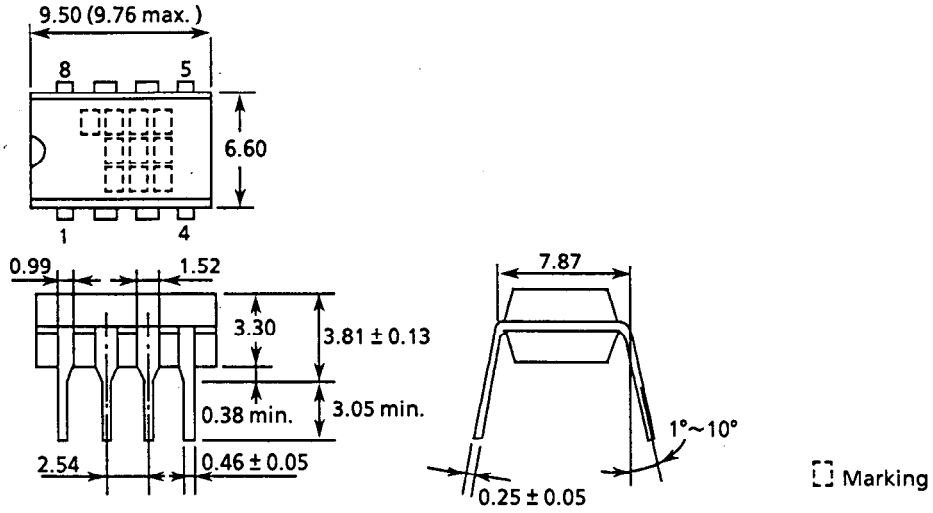


Figure 13

2. 8-pin SOP

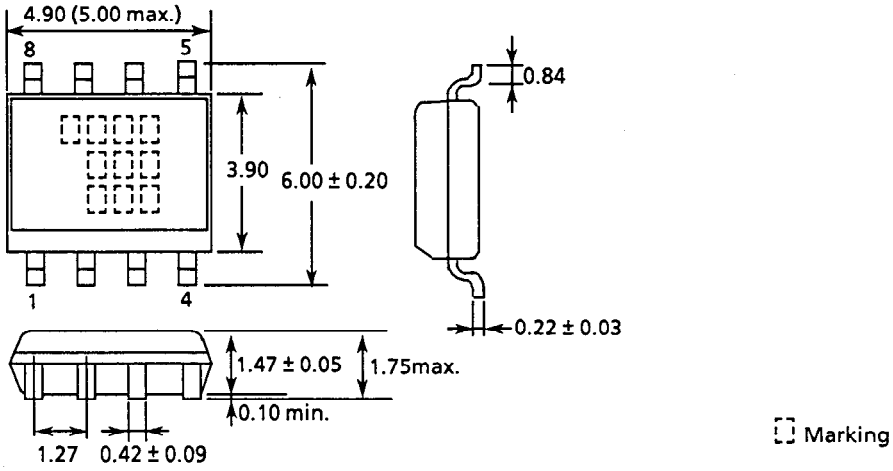


Figure 14

■ Ordering Information

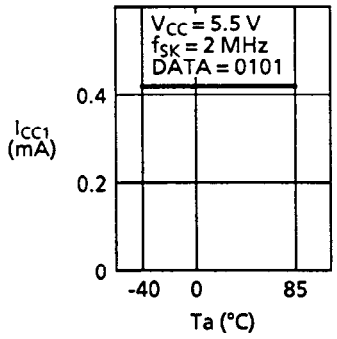
S-29X90A XX

- Package: DP: DIP; FJ : SOP1
- Product name: S-29190A : 1K-bit; S-29290A : 2K-bit; S-29390A : 4K-bit

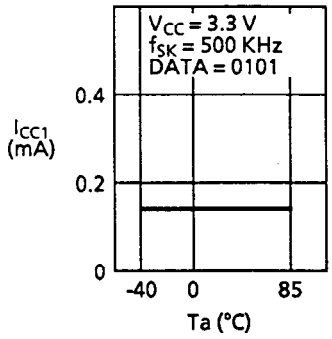
■ Characteristics

1. DC Characteristics

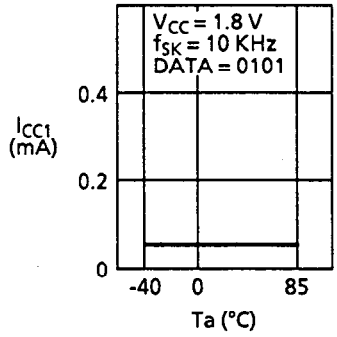
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



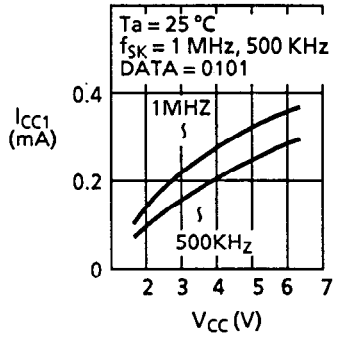
1.2 Current consumption (READ) I_{CC1} — Ambient temperature Ta



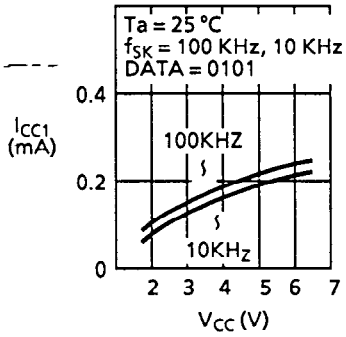
1.3 Current consumption (READ) I_{CC1} — Ambient temperature Ta



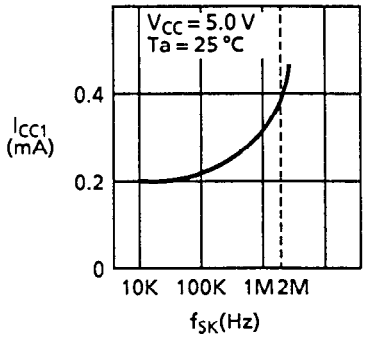
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



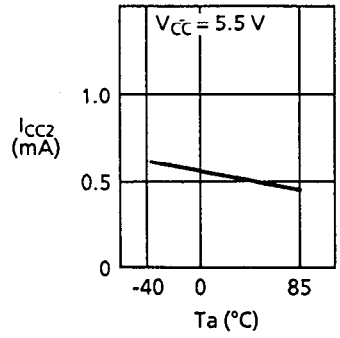
1.5 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



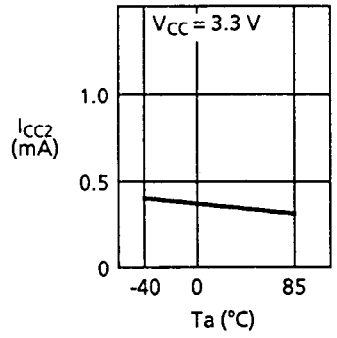
1.6 Current consumption (READ) I_{CC1} — Clock frequency f_{SK}



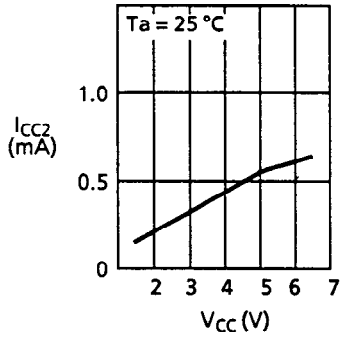
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



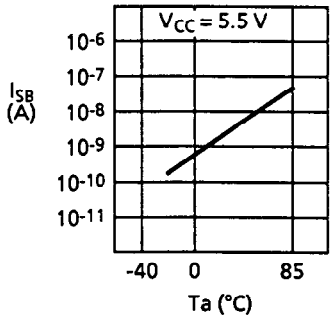
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



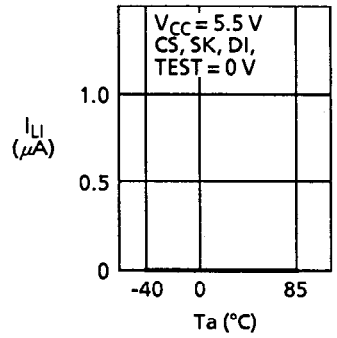
1.9 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



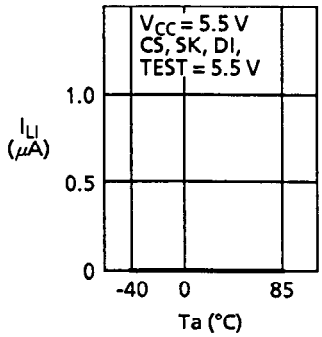
1.10 Standby current consumption I_{SB}— Ambient temperature Ta



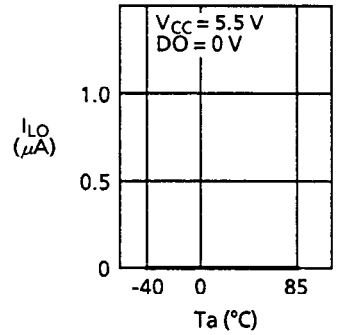
1.11 Input leakage current I_{LI} – Ambient temperature Ta



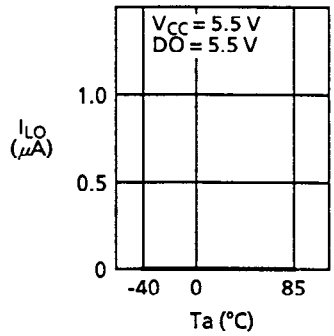
1.12 Input leakage current I_{LI} – Ambient temperature Ta



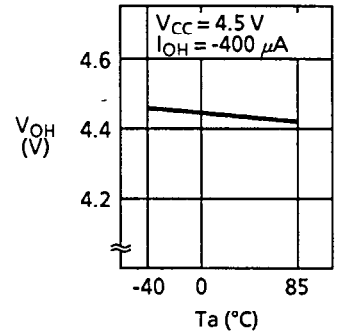
1.13 Output leakage current I_{LO} – Ambient temperature Ta



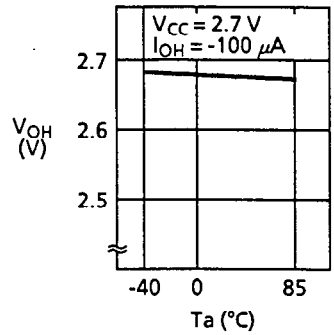
1.14 Output leakage current I_{LO} – Ambient temperature Ta



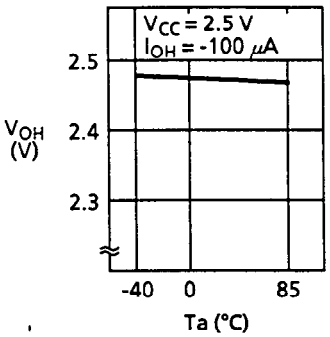
1.15 High level output voltage V_{OH} – Ambient temperature Ta



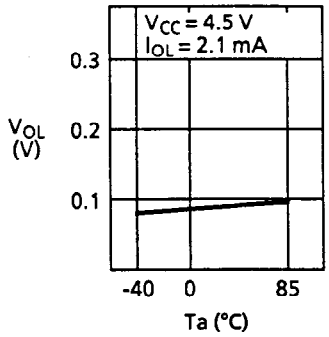
1.16 High level output voltage V_{OH} – Ambient temperature Ta



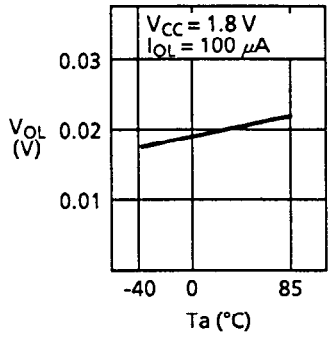
1.17 High level output voltage V_{OH} – Ambient temperature Ta



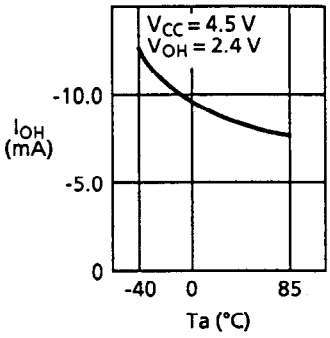
1.18 Low level output voltage V_{OL} – Ambient temperature Ta



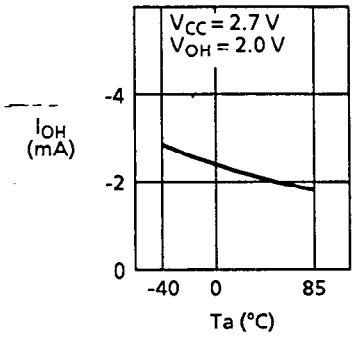
1.19 Low level output voltage V_{OL} – Ambient temperature Ta



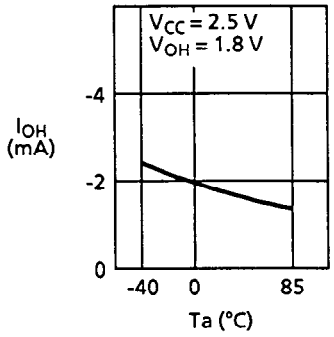
1.20 High level output current I_{OH} – Ambient temperature Ta



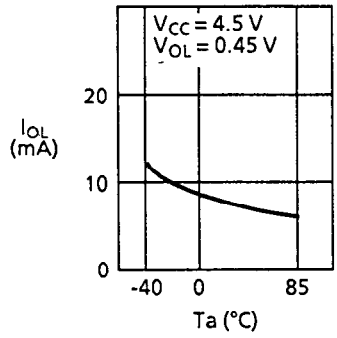
1.21 High level output current I_{OH} – Ambient temperature Ta



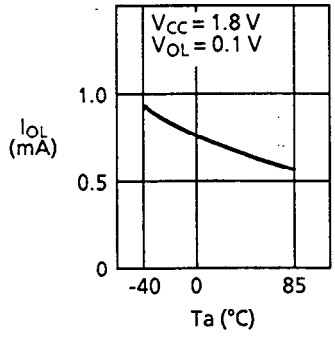
1.22 High level output current I_{OH} – Ambient temperature Ta



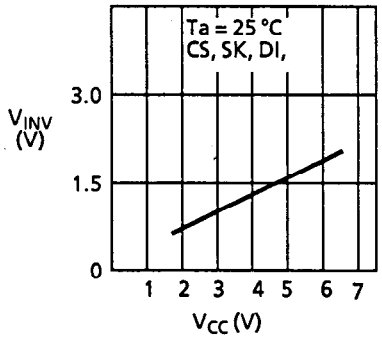
1.23 Low level output current I_{OL} – Ambient temperature Ta



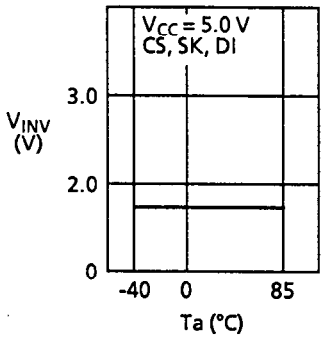
1.24 Low level output current I_{OL} – Ambient temperature Ta



1.25 Input inversion voltage V_{INV} – Power supply voltage V_{CC}

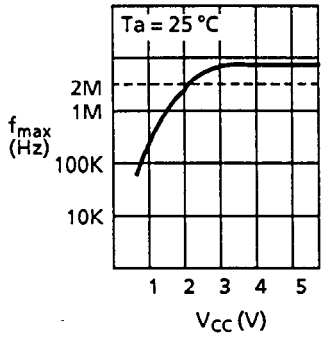


1.26 Input inversion voltage V_{INV} – Ambient temperature Ta

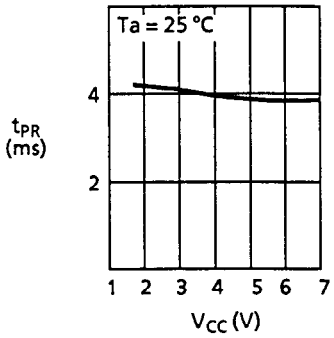


2. AC Characteristics

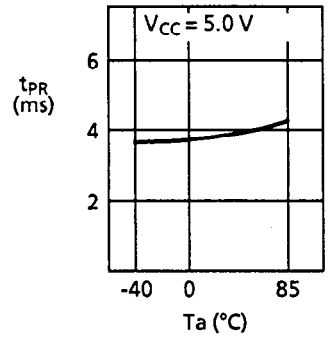
2.1 Maximum operating frequency f_{max} – Power supply voltage V_{CC}



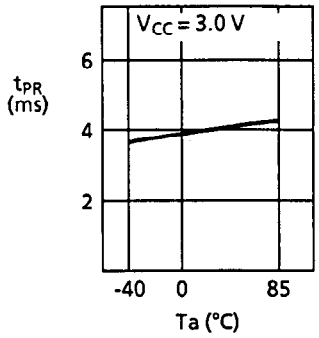
2.2 Program time t_{PR} – Power supply voltage V_{CC}



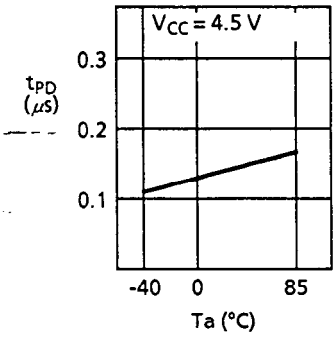
2.3 Program time t_{PR} – Ambient temperature Ta



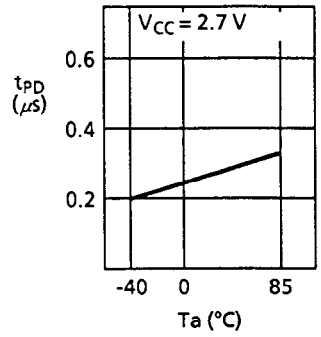
2.4 Program time t_{PR} – Ambient temperature Ta



2.5 Data output delay time t_{PD} – Ambient temperature Ta



2.6 Data output delay time t_{PD} – Ambient temperature Ta



2.7 Data output delay time t_{PD} – Ambient temperature Ta

