Dual 8-Bit CMOS D/A Converter with Voltage Output

DAC8228

FEATURES

- Two 8-Bit Voltage Out DACs in a Single Chip
- Fits 7528/7628 Sockets
- Adjustment Free Internal CMOS Op Amps
- Single +12V to +15V Operation
- TTL Compatible Over Full V_{DD} Range
- Fast Interface Timing ..... T_{WR} = 50ns
- Improved Resistance to ESD
- Available in Small Outline Package
- CerDIP and Epoxy Packages Come in the Extended Industrial Temperature Range of –40°C to +85°C
- Available in Die Form

APPLICATIONS

- Disk Drive Systems
- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Programmable Instrumentation
- Multi-Channel Microprocessor-Controlled Systems
- Servo Control Systems

ORDERING INFORMATION †

		PACKAGE: 20-PIN DIP/SOL
RELATIVE ACCURACY	GAIN ERROR	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C
±1/2 LSB	±2 LSB	DAC8228FR
±1/2 LSB	±2 LSB	DAC8228FP
±1/2 LSB	±2 LSB	DAC8228FS

† All commercial and industrial temperature range parts are available with burn-in.

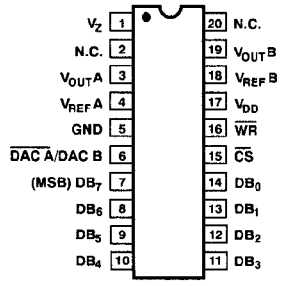
GENERAL DESCRIPTION

The DAC-8228 is a dual 8-bit, voltage output, CMOS, D/A converter in a single chip. It was designed to drop into AD7528/7628 sockets eliminating two external op amps in applications such as hard disk drives. These applications generally operate the AD7528/7628 with zero volts applied to V_{REF} and offset AGND to +2.5 or +5 volts. The DAC-8228 is tested under both these conditions.

The DAC-8228 can also be used in those applications requiring a unipolar output voltage. It can deliver an output voltage between 0V and +10V with V_{DD} = +14V (maximum output voltage is V_{DD} –4V). The DAC-8228's reference input can accept a negative voltage from 0V to –10V (the DAC's internal unity-gain inverting amplifier inverts the input signal). Choose the DAC-8229 for bipolar operation.

Continued

PIN CONNECTIONS

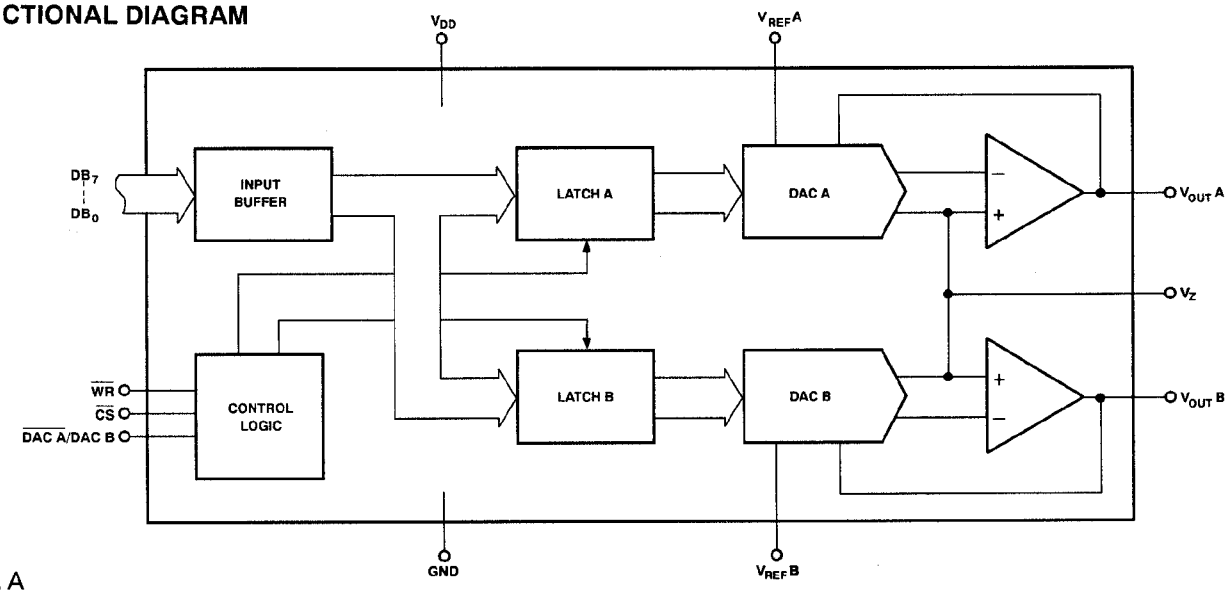


20-PIN 0.3" CERDIP (R-Suffix)

20-PIN SOL (S-Suffix)

20-PIN EPOXY DIP (P-Suffix)

FUNCTIONAL DIAGRAM



REV. A

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GENERAL DESCRIPTION *Continued*

The DAC-8228 offers CerDIP and plastic packaged devices in the extended industrial temperature range of –40°C to +85°C. Applications requiring the military temperature range should use the DAC-8229. To make the DAC-8229 pin and functionally compatible with the DAC-8228, AGND A and AGND B should be tied together to function as V_Z, and V_{SS} connected to GND.

The DAC-8228 consists of two CMOS voltage output amplifiers, two high-accuracy R-2R resistor ladder networks, interface control logic, and two 8-bit registers. An internal regulator maintains TTL logic compatibility and fast microprocessor interface timing over the full V_{DD} range.

The DAC-8228 dissipates only 90mW in the space saving 20-pin 0.3" DIP or the 20-lead SO surface mount package. Its compact size, low power, and economical cost per channel, makes it attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. Reduced parts count also improves system reliability.

Using PMI's advanced oxide-isolated, silicon-gate CMOS process, coupled with its highly-stable thin-film resistor ladder, allows the DAC-8228 to offer superior matching and temperature tracking between DACs.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to V_Z or GND ..... –0.3V, +17V
V_Z to GND ..... –0.3V, V_{DD}
Digital Input Voltage to GND ..... –0.3V, V_{DD}
$V_{REF\ A}$, $V_{REF\ B}$ to GND ..... –17V, V_Z
$V_{OUT\ A}$, $V_{OUT\ B}$ to V_Z (Note 1) ..... –0.3V, V_{DD}
Operating Temperature Range
FR/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to GND is 50mA.
2. Use proper anti-static handling procedures when handling these devices.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	DAC-8228 TYP	DAC-8228 MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		8	–	–	Bits
Relative Accuracy (Note 2)	INL		–	–	±1	LSB
Differential Nonlinearity (Note 3)	DNL		–	–	±1	LSB
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	–	–	±2	LSB
Gain Error Temperature Coefficient (Note 4)	TCG_{FS}		–	±0.0003	±0.002	%/°C
Zero Code Error	V_{ZSE}		–	–	±15	mV
Zero Code Error Temperature Coefficient (Note 4)	TCV_{ZS}		–	±10	–	µV/°C
REFERENCE INPUT (Note 8)						
Input Resistance (Note 5)	R_{IN}	Pin 4 and Pin 18	7	–	15	kΩ
Input Resistance Match ($V_{REF}A/V_{REF}B$)	$\frac{\Delta R_{IN}}{R_{IN}}$		–	±0.1	±1	%
Input Capacitance (Note 4)	C_{IN}		–	9	20	pF
V_Z Input Resistance (Note 10)	R_{VZ}	Digital Inputs = 0V	2	–	–	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

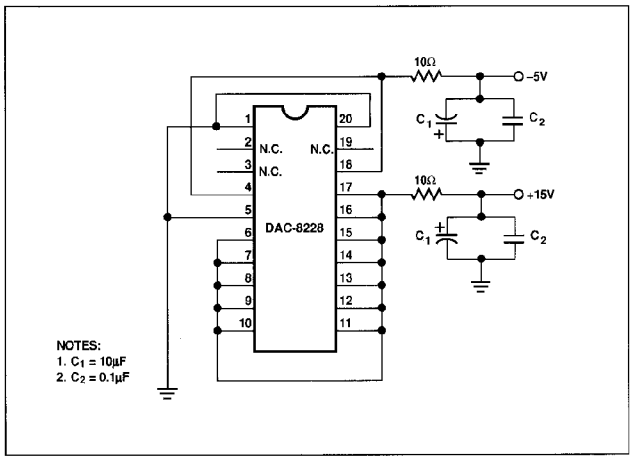
PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	DAC-8228 TYP	DAC-8228 MAX	UNITS
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	–	–	V
Digital Input Low	V_{INL}		–	–	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	–	±1	µA
Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
POWER SUPPLIES						
Supply Current (Note 6)	I_{DD}		–	–	7	mA
Power Dissipation	P_D	V_{DD} = +12V 12 x 7mA	–	–	84	mW
		V_{DD} = +15V 15 x 7mA	–	–	105	
DC Power Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$)	PSRR	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
Slew Rate (V_{OUT}) (Note 4)	SR	T_A = +25°C Digital Inputs = 0V to +5V	–	2.5	–	V/µs
Settling Time (V_{OUT}) Positive or Negative (Note 4, 7)	t_s	Digital Inputs = 0V to +5V	–	2	5	µs
Channel-to-Channel Isolation (Note 4)	CCI	T_A = +25°C $V_{REF}B$ to $V_{OUT}A$ or $V_{REF}A$ to $V_{OUT}B$ $V_{REF}B = V_{REF}A = 20V_{p-p}$ @ f = 10kHz	–	–80	–	dB
Digital Crosstalk (Notes 4, 9)	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	4	10	nVs
Digital Charge Injection	Q	T_A = +25°C For Code Transition 0000 0000 to 1111 1111	–	100	–	nVs
AC Feedthrough (Notes 4, 11)	FT		–	–	–70	dB
Harmonic Distortion	THD	T_A = +25°C $V_{IN} = 6V_{RMS}$ @ f = 1kHz	–	–85	–	dB

ELECTRICAL CHARACTERISTICS at V_{DD} = +12V ±5%, V_{REF} = 0V, V_Z = +2.5V and V_{DD} = +15V ±5%, V_{REF} = 0V, V_Z = +5V. T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted. *Continued*

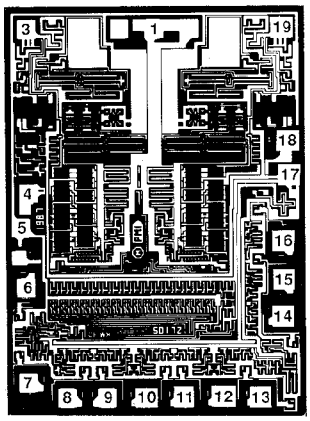
PARAMETER	SYMBOL	CONDITIONS	DAC-8228 MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4)						
Chip Select to Write Set-Up Time	t_{CS}		60	–	–	ns
Chip Select to Write Hold Time	t_{CH}		10	–	–	ns
DAC Select to Write Set-Up Time	t_{AS}		60	–	–	ns
DAC Select to Write Hold Time	t_{AH}		10	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}		60	–	–	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}		50	–	–	ns

NOTES:
1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All devices are guaranteed to be monotonic over the full operating temperature range.
4. These characteristics are for design guidance only and not subject to production test.
5. Input resistance temperature coefficient = +300ppm/°C.
6. $V_{IN} = V_{INL}$ or V_{INH}; outputs unloaded.
7. V_{REF} = ±2.5V; to where output settles to ±1/2 LSB.
8. V_{REF} voltage range is 0V to −10V; the absolute maximum negative value is: $|V_{REF}| = V_{DD} - 4V$.
9. Digital crosstalk is a measure of the amount of digital input pulse appearing at the analog output of the unselected DAC while applying it to the digital inputs of the other DAC.
10. Resistance looking into the V_Z terminal.
11. $V_{REF}A$, $V_{REF}B$ = 20V_{p-p} Sinewave @ f = 10kHz; $V_{REF}A$ to $V_{OUT}A$ or $V_{REF}B$ to $V_{OUT}B$, both DAC latches loaded with 0000 0000.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.082x 0.111 inch, 9,102 sq. mils
(2.08 x 2.82 mm, 5.87 sq. mm)

1. AMPLIFIER REFERENCE (V_Z)
2. N.C.
3. VOLTAGE OUTPUT ($V_{OUT}A$)
4. DAC A REFERENCE INPUT ($V_{REF}A$)
5. GROUND (GND)
6. DAC SELECTION ($\overline{\text{DAC A}}$/DAC B)
7. DIGITAL INPUT DB_7 (MSB)
8. DIGITAL INPUT DB_6
9. DIGITAL INPUT DB_5
10. DIGITAL INPUT DB_4
11. DIGITAL INPUT DB_3
12. DIGITAL INPUT DB_2
13. DIGITAL INPUT DB_1
14. DIGITAL INPUT DB_0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. VOLTAGE OUTPUT ($V_{OUT}B$)
20. N.C.

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at $V_{DD} = V_{DD} = +12V \pm 5\%$, $V_{REF} = 0V$, $V_Z = 2.5V$ or $V_{DD} = +15V \pm 5\%$, $V_{REF} = 0V$, $V_Z = +5V$, $T_A = +25°C$.

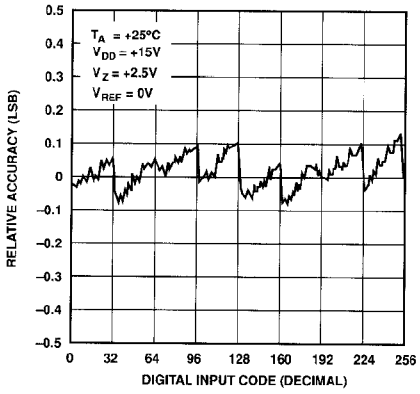
PARAMETER	SYMBOL	CONDITIONS	DAC-8228GBC LIMITS	UNITS
Relative Accuracy (Note 3)	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity (Notes 1, 3)	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111	±2	LSB MAX
Zero Code Error	V_{ZSE}		±15	mV MAX
Input Resistance	R_{IN}	Pad 4 and 18	7/15	kΩ MIN/kΩ MAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\frac{\Delta R_{IN}}{R_{IN}}$		1	% MAX
V_Z Input Resistance (Note 3)	R_{VZ}	Digital Inputs = 0V	2	kΩ MIN
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	±1	µA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	$V_{DD} = \pm 5\%$	0.01	%/% MAX
Positive Supply Current (Note 2)	I_{DD}		7	mA MAX

NOTES:
1. All dice guaranteed monotonic over the full operating temperature range.
2. $V_{IN} = V_{INL}$ or V_{INH}; output unloaded.
3. Resistance looking into the V_Z terminal.

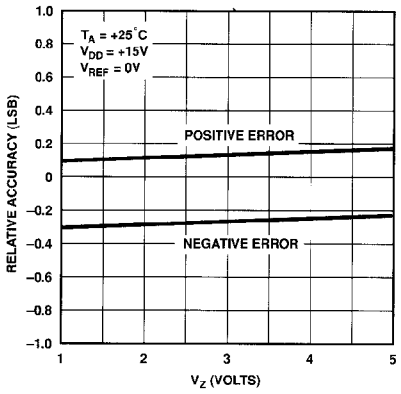
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

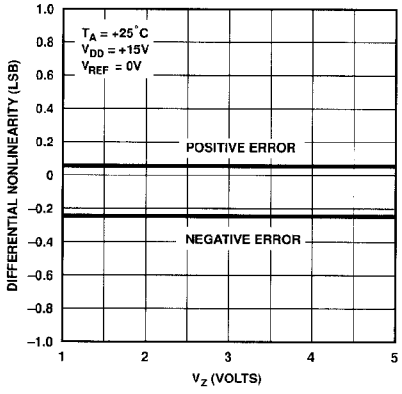
RELATIVE ACCURACY vs CODE (V_{REF}= 0V, V_Z = +2.5V)



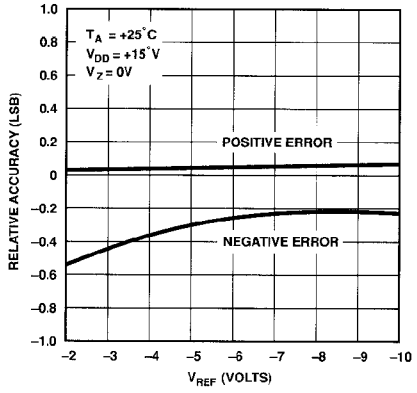
RELATIVE ACCURACY vs V_Z



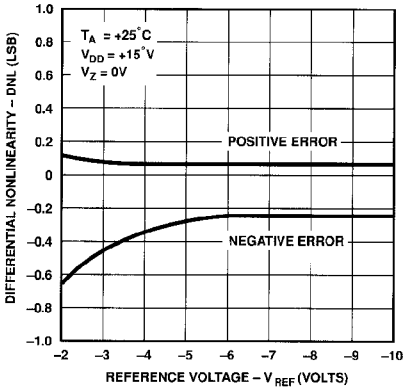
DIFFERENTIAL NONLINEARITY vs V_Z



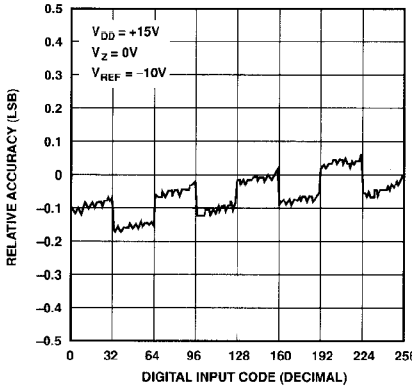
RELATIVE ACCURACY vs REFERENCE VOLTAGE



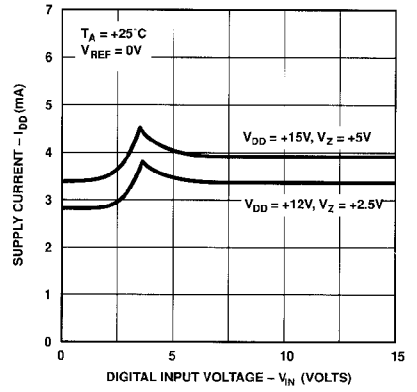
DIFFERENTIAL NONLINEARITY vs REFERENCE VOLTAGE



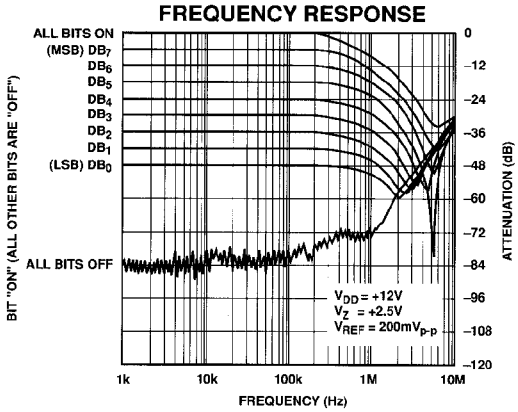
RELATIVE ACCURACY vs CODE (V_{REF}= –10V, V_Z = 0V)



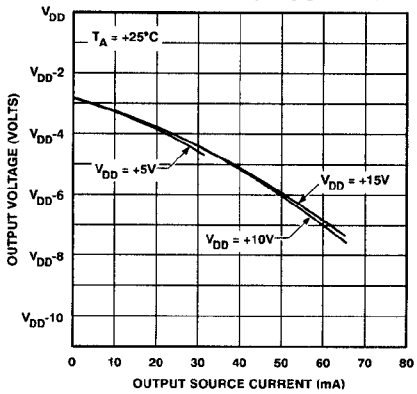
SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE



MULTIPLYING MODE FREQUENCY RESPONSE

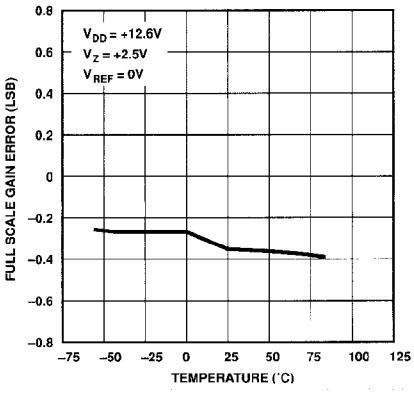


OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

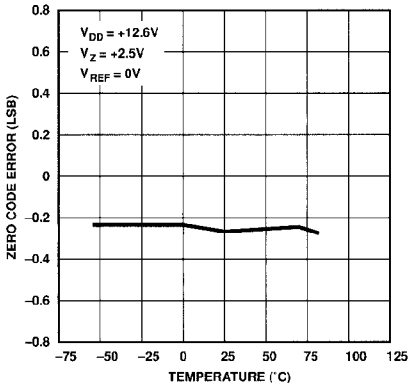


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

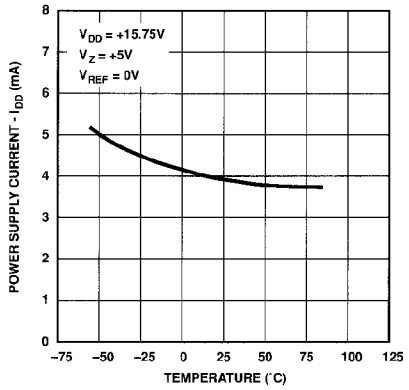
FULL SCALE GAIN ERROR vs TEMPERATURE



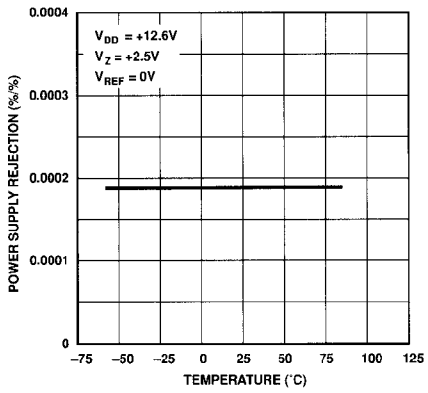
ZERO CODE ERROR vs TEMPERATURE



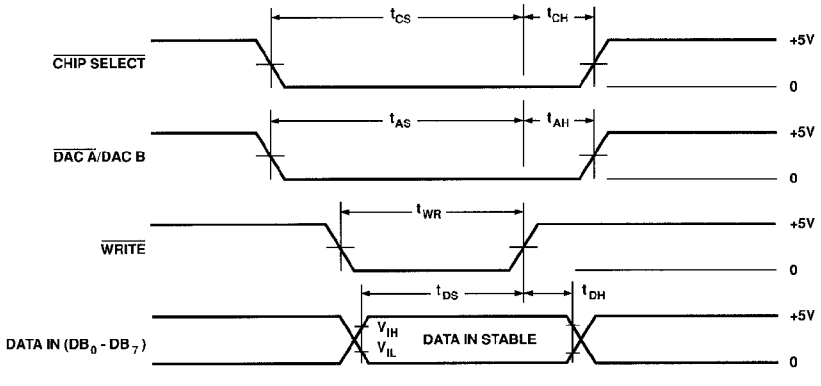
POWER SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION vs TEMPERATURE



WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% ARE $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

PARAMETER DEFINITIONS

RESOLUTION (N)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bits (LSB), or as a percent of full-scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 may be non-monotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal. Zero code error is not included in this measurement.

ZERO CODE ERROR (V_{ZSE})

Zero Code Error means, for the DAC-8228 specification table, the amount of offset voltage referenced to V_Z, i.e., V_Z = +2.5V, ±10mV offset is equal to +2.490V to +2.510V referenced to ground.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

The DAC-8228 consists of two voltage output amplifiers, two high accuracy R-2R resistor ladder networks, an 8-bit input buffer, two 8-bit DAC registers, and interface control logic circuitry.

Also included are 16 single-pole, double-throw NMOS transistor switches. These switches, which are controlled by the digital input code, were designed to switch each 2R resistor leg between the amplifier inverting input and V_Z, see Figure 1. This configuration inverts the reference input voltage, and also allows biasing V_Z above digital ground simplifying many applications.

REFERENCE INPUT

The DAC-8228's reference input voltage range is limited by the internal amplifier voltage swing. The amplifier output can swing from 0V to +10V when V_{DD} = +14V; note that the output voltage is 4 volts less than V_{DD}. V_{DD} –4V sets the maximum voltage that the reference input can accept (but in the negative direction due to the inverting amplifier, see Figure 1). V_{REF} voltage range is 0V to $-|V_{DD}-4V|$; in equation form: $-V_{REF}(max) = |V_{DD}-4V|$.

BUFFER AMPLIFIER SECTION

The DAC-8228 internal amplifier's output stage is an NPN bipolar transistor connected to a 450µA current source, see Figure 2. This transistor provides a low output impedance that can drive 5mA across a 2k load. In fact, it can drive up to 65mA, but with a reduced output amplitude. See the Output Voltage vs. Output Source Current graph under the typical electrical characteristics curves. The user must use caution that the package power dissipation is not exceeded when driving low impedances and high currents.

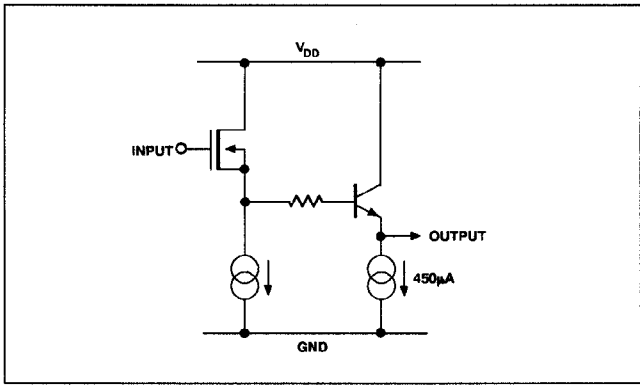


FIGURE 2: *Amplifier Output Stage*

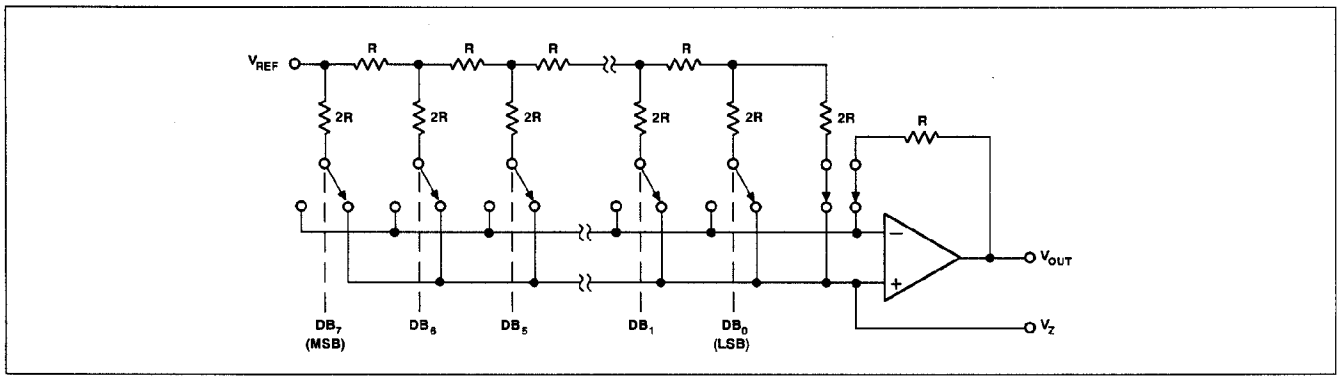


FIGURE 1: *Simplified single DAC configuration (switches shown for all digital inputs at logic "0").*

Figure 3 depicts a typical output current-sink versus voltage graph for the amplifier's output stage. It shows the output coming out of its saturation region and starting to appear resistive as the output approaches zero volts.

The amplifier's internal gain stages were designed to maintain sufficient gain over its common mode range. This results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during manufacturing. This eliminates user offset trimming.

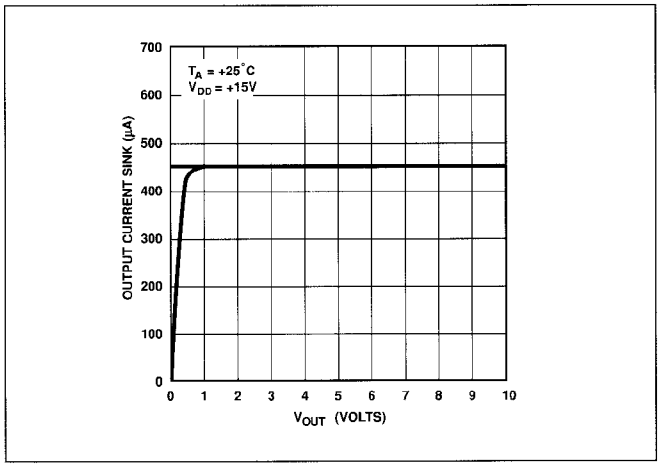


FIGURE 3: *DAC Output Current Sink*

DIGITAL SECTION

Figure 4 shows one digital input structure of the DAC-8228. A built-in 5V regulator and level shifter converts TTL digital input signals into CMOS levels to drive the internal circuitry. This provides full TTL compatibility over a V_{DD} range of 5 to 15V.

As shown in Figure 4, each digital input is protected from electrostatic-discharge with two internal diodes connected between V_{DD} and GND. Each input has a typical input current of less than 1nA.

INTERFACE CONTROL INFORMATION

DAC SELECTION

DAC A and DAC B both share a common 8-bit input port. The control input, $\overline{\text{DAC A}}$/DAC B, selects which DAC can accept data from the input port. A logic low selects DAC A and a logic high selects DAC B.

DAC OPERATION

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operation of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input buffer and DAC register of the selected DAC are transparent and its analog output responds to the codes on the digital input pins.

HOLD MODE

The selected DAC register latches the data present on the digital input pins just prior to $\overline{\text{CS}}$ and $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective registers.

MODE SELECTION TABLE

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

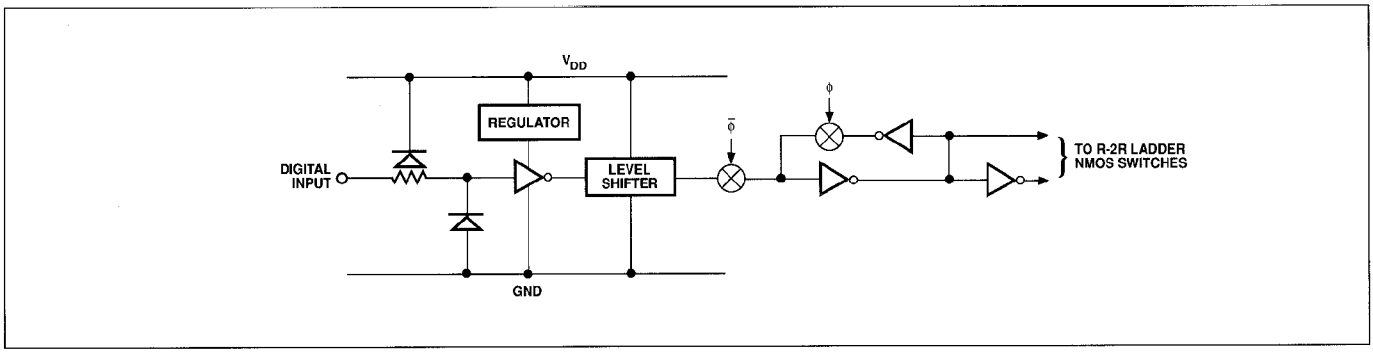


FIGURE 4: *Simplified Digital Input Structure*

APPLICATIONS INFORMATION

Figure 5 shows the DAC-8228 configured to operate with V_Z biased above ground. Note how the reference source is connected between V_Z and ground; also note how the DAC's V_{REF} pin is connected directly to ground. Not shown but equally important is that the reference voltage source at V_Z is common to both DAC A and DAC B.

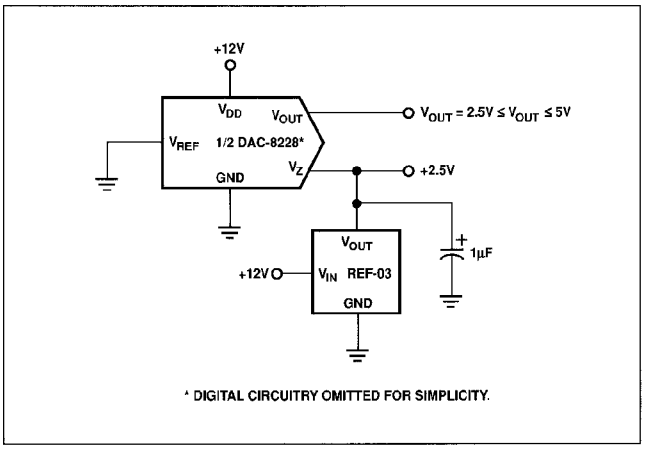


FIGURE 5: *Single Supply Configuration (+2.5V ≤ V_{OUT} ≤ +5V)*

The +2.5V reference voltage is obtained from PMI's REF-03; if greater accuracy is desired, use the REF-43. The REF-02 or REF-05, depending on accuracy required, can be used for +5V applications.

The transfer equation for the circuit of Figure 5 is:

$V_{OUT} = V_Z (1 + D/256)$

where
V_Z = Reference voltage applied to V_Z
D = whole number binary digital input

With all 1s on the digital inputs for the circuit of Figure 5, V_{OUT} results in:

$V_{OUT} = 2.5(1 + 255/256)$
$= +5V$

And with all 0s on all digital inputs:

$V_{OUT} = +2.5V$

Note that this configuration's output voltage range is determined by the input reference voltage and V_Z. A digital zero input provides an output voltage equal to V_Z. An all ones digital input provides an output voltage equal to: $2(V_Z - V_{REF})$.

Figure 6 shows a plot of Relative Accuracy versus V_Z voltage.

Figure 7 shows the DAC-8228 in another single supply configuration. In this circuit, a PMI REF-08 is used for the reference voltage source and V_Z is grounded. The output swings from 0V to +10V, see Figure 8.

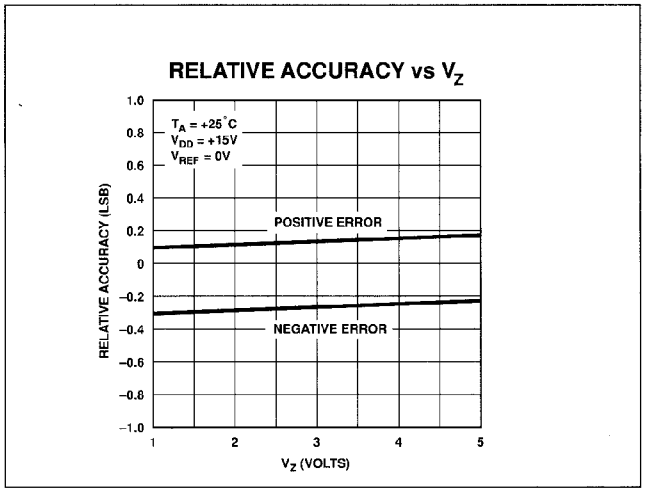


FIGURE 6: *Relative Accuracy vs. AGND*

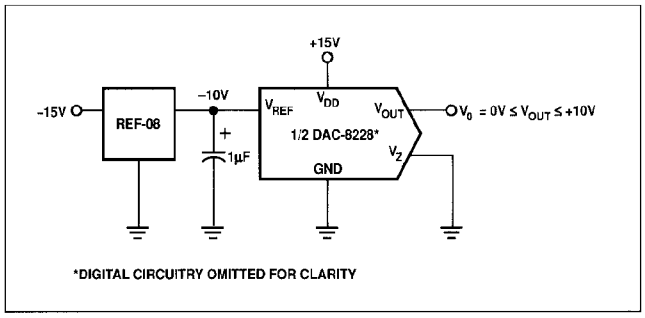


FIGURE 7: *Single Supply Configuration ($V_O \leq V_{OUT} \leq +10V$)*

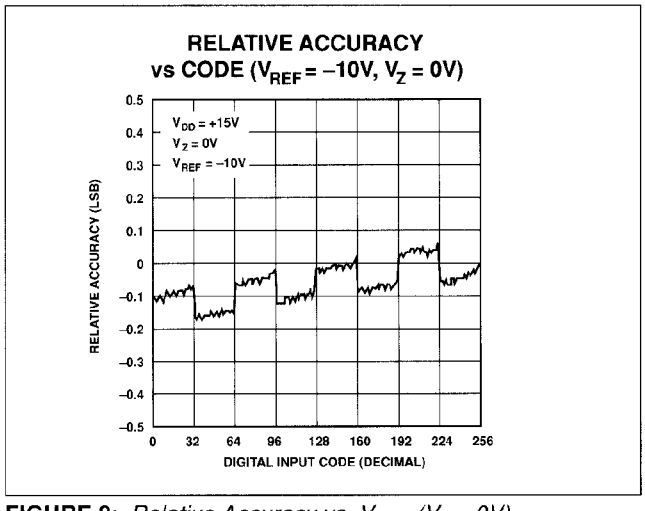


FIGURE 8: *Relative Accuracy vs. V_{REF} (V_Z = 0V)*

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8228's versatile input structure allows direct interface to 8- or 16-bit microprocessors. Its simplicity reduces the number of required glue logic components. Figures 9 and 10 show the DAC-8228 interface configurations with the 6800 and 8085 microprocessors.

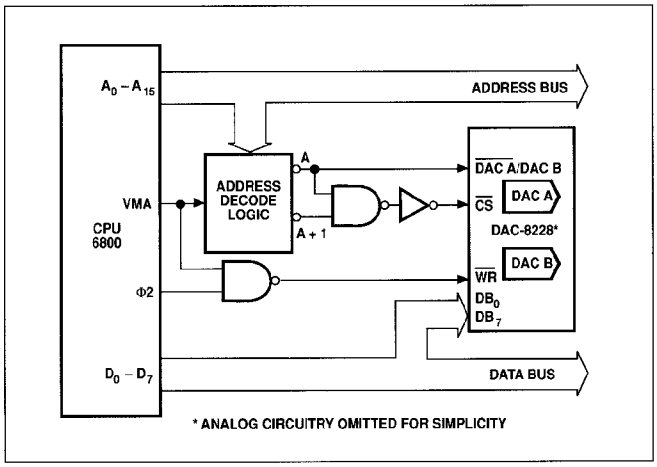


FIGURE 9: *DAC-8228 Interface to 6800 Microprocessor*

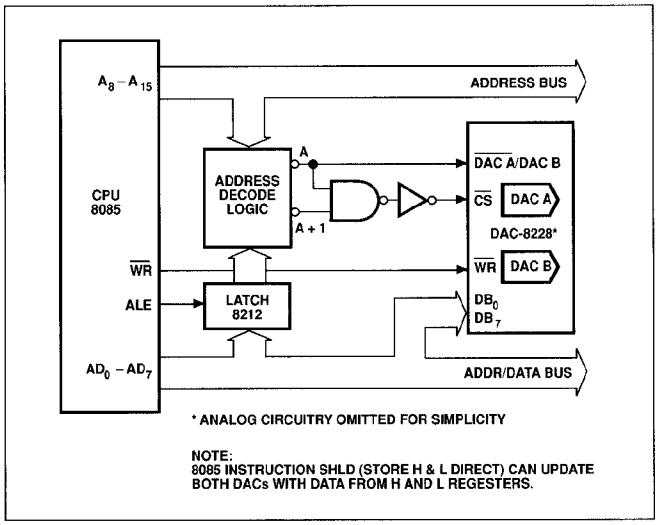


FIGURE 10: *DAC-8228 Interface to 8085 Microprocessor*