1.5-A/2.5-A Dual, Fully-Synchronous Buck Converter With Integrated MOSFET

Check for Samples :TPS54290 TPS54291 TPS54292

FEATURES

- **4.5 V to 18 V Input Range**
- **Output Voltage Range 0.8 V to D_{MAX} × V_{IN}**
- **Fully Integrated Dual Buck, 1.5 A/2.5 A**
- **Three Fixed Switching Frequency Versions:**
  - **TPS54290 – 300 kHz**
  - **TPS54291 – 600 kHz**
  - **TPS54292 – 1.2 MHz**
- **Integrated UVLO**
- **0.8 V_{REF} With 1% Accuracy (0°C to 85°C)**
- **Internal Soft-Start**
  - **TPS54290 – 5.2 ms**
  - **TPS54291 – 2.6 ms**
  - **TPS54292 – 1.3 ms**
- **Dual PWM Outputs 180° Out-of-Phase**
- **Dedicated Enable for Each Channel**
- **Current Mode Control for Simplified Compensation**
- **External Compensation**
- **Pulse-by-Pulse Overcurrent Protection, 2.2 A/3.8 A Overcurrent Limit**
- **Integrated Bootstrap Switch**
- **Thermal Shutdown Protection at 145°C**
- **16-Pin PowerPAD™ HTSSOP Package**

APPLICATIONS

- **Set Top Box**
- **Digital TV**
- **Power for DSP**
- **Consumer Electronics**

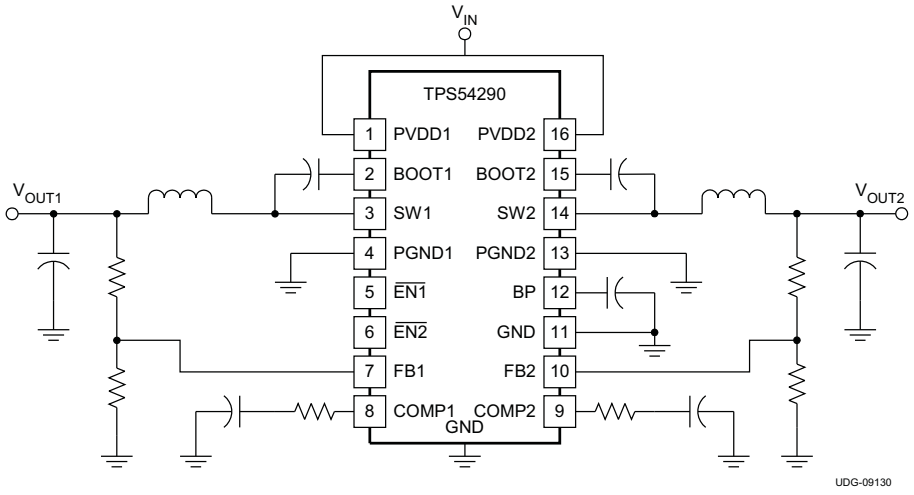
DESCRIPTION

TPS54290/1/2 is a dual output fully synchronous buck converter capable of supporting applications with a minimal number of external components. It operates from a 4.5 V to 18 V input supply voltage, and supports output voltages as low as 0.8 V and as high as 90% of the input voltage.

Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. Channel1 can provide up to 1.5 A of continuous current, meanwhile, Channel2 supports up to 2.5 A.

Current mode control simplifies the compensation. The external compensation adds flexibility for the user to choose different type of output capacitors.

180° out-of-phase operation reduces the ripple current through the input capacitor, providing the benefit of reducing input capacitance, alleviating EMI and increasing capacitor life.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_J	ORDERABLE DEVICE NUMBER	OPERATING FREQUENCY (kHz)	PACKAGE	PACKING MEDIA	PACKING QUANTITY
–40°C to 145°C	TPS54290PWP	300	16-Pin HTTSOP	Tube	90
	TPS54290PWPR			Tape and Reel	2500
	TPS54291PWP	600		Tube	90
	TPS54291PWPR			Tape and Reel	2500
	TPS54292PWP	1200		Tube	90
	TPS54292PWPR			Tape and Reel	2500

ABSOLUTE MAXIMUM RATINGS (operating in a typical application circuit)

over operating free-air temperature range, all voltages are with respect to GND (unless otherwise noted)

	VALUE	UNIT
PVDD1, PVDD2, $\overline{EN1}$, $\overline{EN2}$	–0.3 to 20	V
SW1, SW2	–1 to 20	
BOOT1, BOOT2	–0.3 to SW+7	
SW1, SW2 transient (< 50 ns)	–3 to 20	
BP	7	
FB1, FB2	–0.3 to 3	
Operating junction temperature	–40 to 145	°C
Storage junction temperature	–55 to 155	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	

PACKAGE DISSIPATION RATINGS(1) (2) (3)

PACKAGE	THERMAL IMPEDANCE JUNCTION TO THERMAL PAD	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
16 Pin HTSSOP (PWP)	2.07°/W	1.6 W	1.0 W

(1) For more information on the PWP package, refer to TI technical brief (SLMA002A)
(2) TI device packages are modeled and tested for thermal performance using PWB designs outlined in JEDEC standards JESD 51-3 and JESD 51-7.
(3) For Application information see Power Derating section

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Input voltage	4.5	18	V
T_J	Junction temperature	–40	125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MIN	UNIT
Human Body Model	2k	V
CDM	1.5k	V

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ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, PVDD1 and 2 = 12V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY							
PVDD1, PVDD2	Input voltage range			4.5		18	V
IDD_{SDN}	Shutdown current		$\overline{EN1}$=$\overline{EN2}$ = PVDD2 (4.5-18V)		80	160	µA
IDD_Q	Quiescent, non-switching		FB1 = FB2 = 1 V, Outputs Off		1.65	3.00	mA
IDD_{SW}	Quiescent, while switching		FB1 = FB2 = 0.75V, measured at BP		10		mA
UVLO	Minimum turn-on voltage		PVDD2 only	3.8	4.1	4.4	V
$UVLO_{HYS}$	Hysteresis				460	600	mV
t_{start} (1) (2)	Time from startup to soft start begin		CBP=10µF, $\overline{EN1}$ and $\overline{EN2}$ go low simultaneously		1.5		ms
ENABLE (ACTIVE LOW)							
$V_{\overline{ENx}}$	Enable threshold voltage			0.9	1.2	1.5	V
	Hysteresis				70		mV
$I_{\overline{ENx}}$	Enable pull-up current					10	µA
$t_{\overline{ENx}}$ (1)	Time from enable to soft-start begin		Other enable pin = GND		10		µs
BP REGULATOR							
BP	Regulator voltage		8 V ≤ V_{PVDD2} ≤ 18 V	5.0	5.2	5.6	V
BP_{LDO}	Dropout voltage		V_{PVDD2} = 4.5 V		400		mV
I_{BPS}	Regulator short current		4.5 V ≤ V_{PVDD2} ≤ 18 V		25		mA
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS54290		260	300	360	kHz
		TPS54291		520	600	720	
		TPS54292		1040	1200	1440	kHz
t_{DEAD} (1)	Clock dead time				140		ns
g_M TRANSCONDUCTANCE AMPLIFIER AND VOLTAGE REFERENCE (Applies to both channels)							
V_{FB}	Feedback input voltage		0°C < T_J < 85°C	792	800	808	mV
			–40ºC < T_J < 125°C	786	800	812	mV
I_{FB}	Feedback Input bias current		V_{FB}=0.8 V		5	50	nA
g_M (1)	Transconductance			200	325	450	µS
I_{SOURCE}	Error amplifier source current capability		V_{FB1}=V_{FB2}=0.7 V, V_{COMP}=0 V	15	30	40	µA
I_{SINK}	Error amplifier sink current capability		V_{FB1}=V_{FB2}=0.9 V, V_{COMP}=2 V	15	30	40	µA
SOFT-START (Applies to both channels)							
t_{SS}	Soft-start time	TPS54290	0 V ≤ V_{FB} ≤ 0.8 V	4.0	5.2	6.0	ms
		TPS54291		2.0	2.6	3.0	
		TPS54292		1.0	1.3	1.6	
OVERCURRENT PROTECTION							
I_{CL1}	Current limit CH1			1.8	2.2	2.6	A
I_{CL2}	Current limit CH2			3.2	3.8	4.6	A
T_{HICCUP} (1)	Hiccup timeout	TPS54290			30		ms
		TPS54291			16		
		TPS54292			8		
t_{ONOC} (1)	Minimum overcurrent pulse				150	200	ns

(1) Specified by design. Not tested in production.
(2) When both outputs are started simultaneously, a 20-mA current source charges the BP capacitor. Faster times are possible with a lower BP capacitor value. See *Input UVLO* and *Startup.*

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ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, PVDD1 and 2 = 12V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOTSTRAP (Applied to both channels)							
R_{BOOT}	Bootstrap switch resistance		R(BP to BOOT), I external = 10 mA		33		Ω
PGOOD							
V_{UV}	Feedback voltage limit for PGOOD				660	730	mV
$V_{PG-HYST}$ (3)	PGOOD hysteresis voltage on FB				40		mV
OUTPUT STAGE (Applied to both channels)							
$R_{DS(on1)}$(HS) (3)	On resistance of high-side FET and bondwire on CH1				170	265	mΩ
$R_{DS(on2)}$(HS) (3)	On resistance of high-side FET and bondwire on CH2				120	190	mΩ
$R_{DS(on1)}$(LS) (3)	On resistance of low-side FET and bondwire on CH1				120	190	mΩ
$R_{DS(on2)}$(LS) (3)	On resistance of low-side FET and bondwire on CH2				90	150	mΩ
t_{ON_MIN} (3)	Miimum controllable pulse width				150		ns
Minimum duty cycle			V_{FB} = 0.9 V			0%	
t_{DEAD} (3)	Output driver dead time		HDRV off to LDRV on		20		ns
			LDRV off to HDRV on		20		ns
D_{MAX}	Maximum duty cycle	TPS54290		90%	96%		
		TPS54291		85%	91%		
		TPS54292		78%	82%		
THERMAL SHUTDOWN							
T_{SD} (3)	Shutdown temperature				145		°C
T_{SD_HYS} (3)	Hysteresis				20		°C

(3) Specified by design. Not tested in production.

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TYPICAL PERFORMANCE CHARACTERISTICS

QUIESCENT CURRENT vs TEMPERATURE

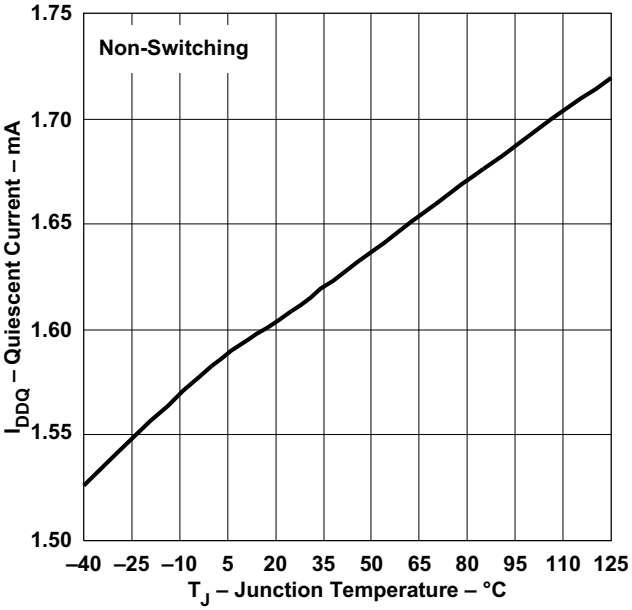


Figure 1.

SHUTDOWN CURRENT vs TEMPERATURE

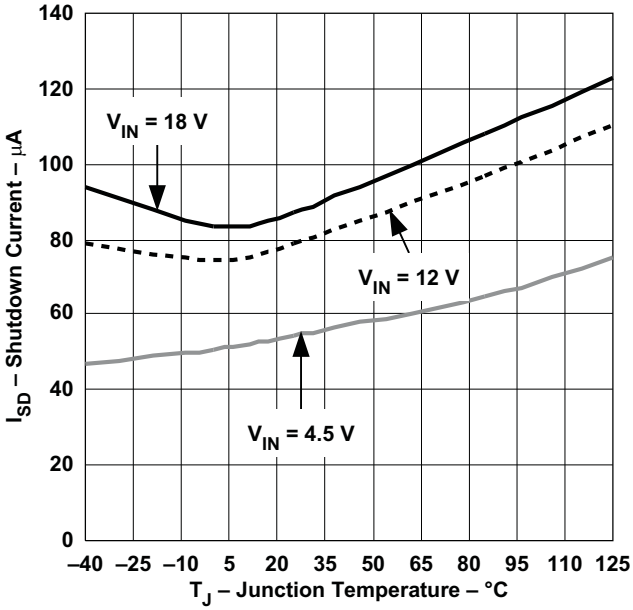


Figure 2.

UVLO TURN-ON AND TURN-OFF THRESHOLDS vs TEMPERATURE

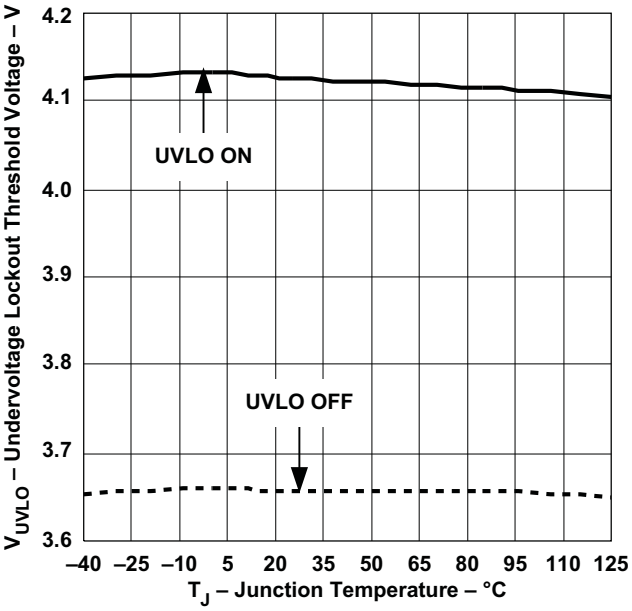


Figure 3.

$\overline{ENx}$ TURN ON AND OFF THRESHOLD vs TEMPERATURE

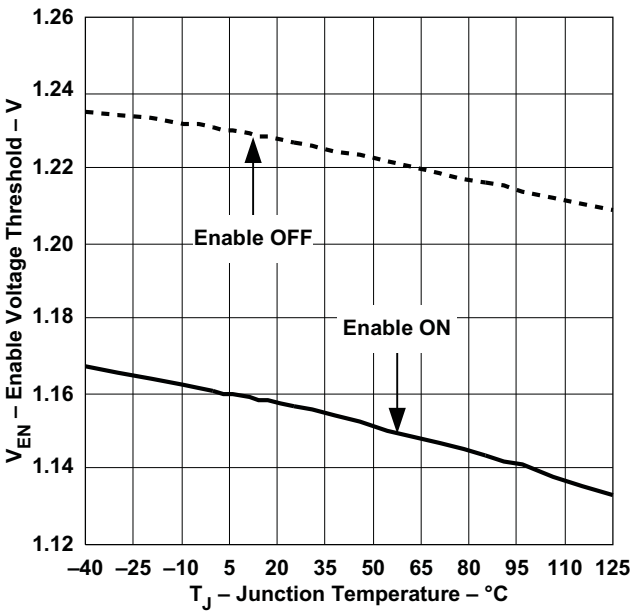


Figure 4.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SOFT START TIME
vs
TEMPERATURE

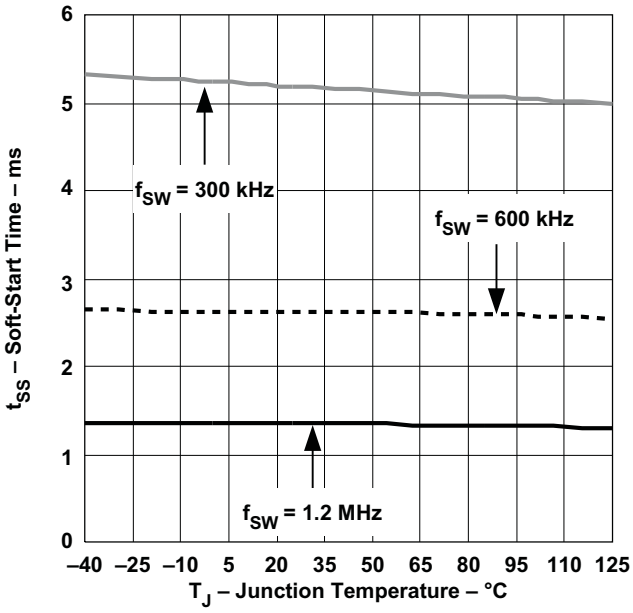


Figure 5.

OSCILLATOR FREQUENCY
vs
TEMPERATURE

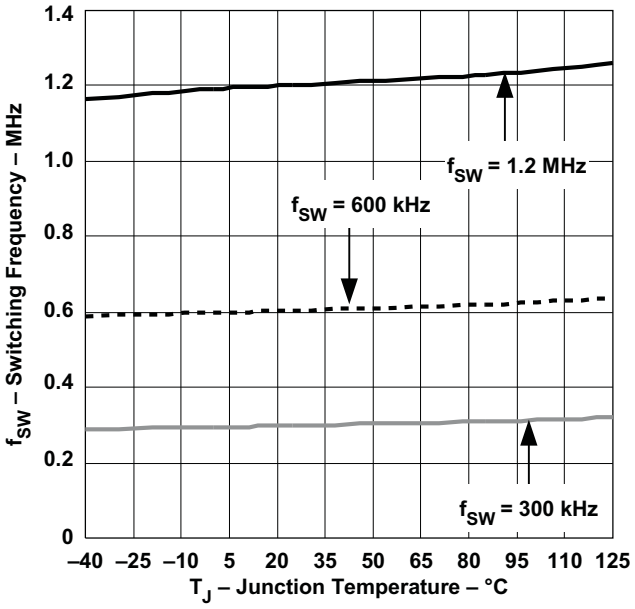


Figure 6.

FEEDBACK VOLTAGE
vs
TEMPERATURE

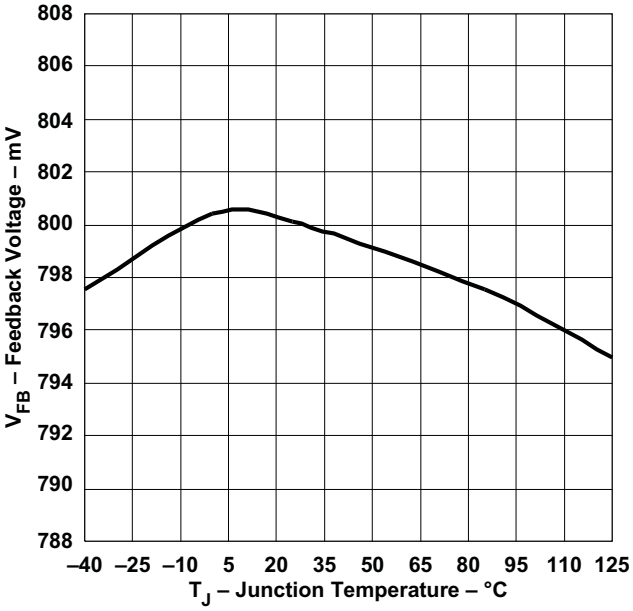


Figure 7.

CURRENT LIMIT
vs
TEMPERATURE

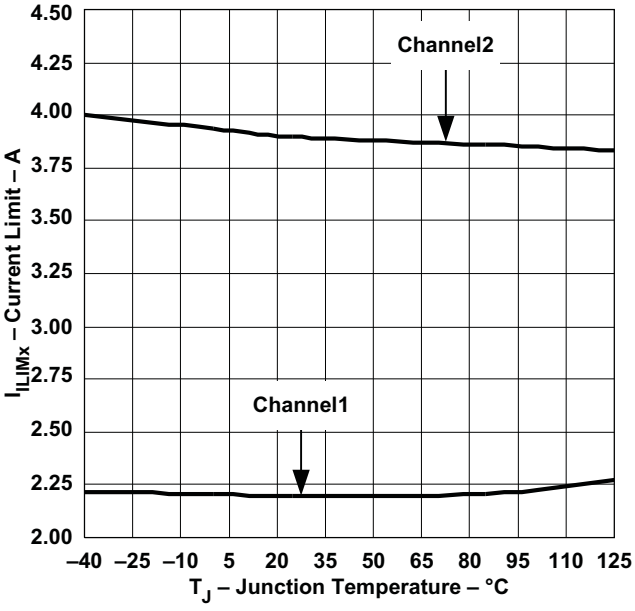


Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

BP VOLTAGE vs TEMPERARURE

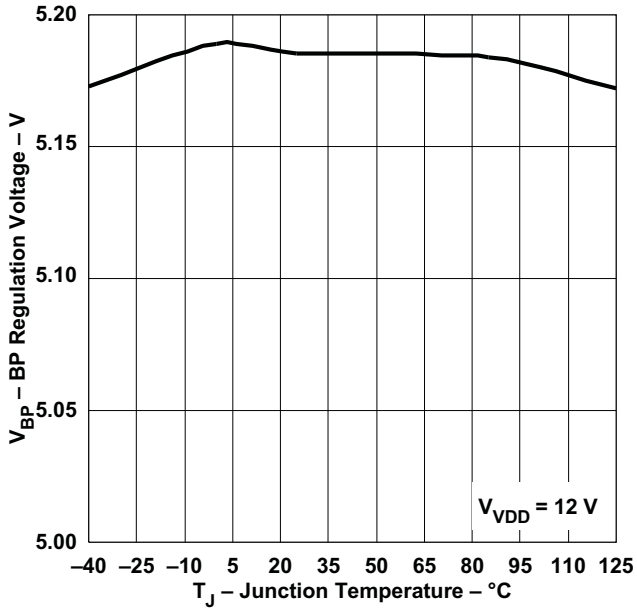


Figure 9.

SW NODE LEAKAGE CURRENT vs TEMPERATURE

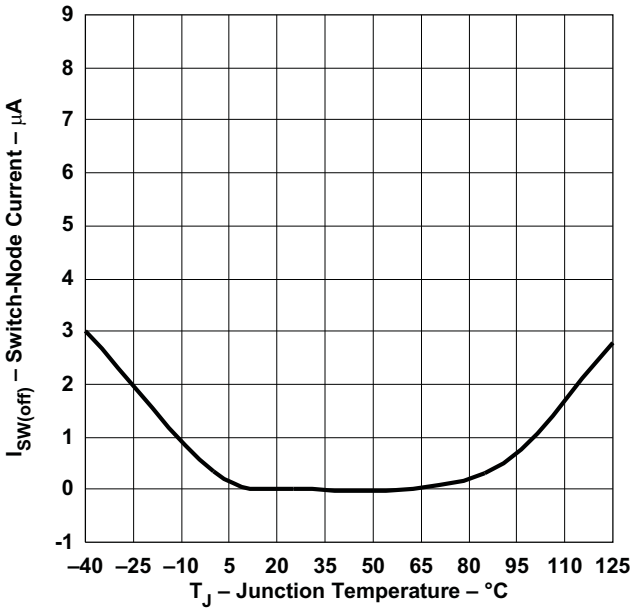
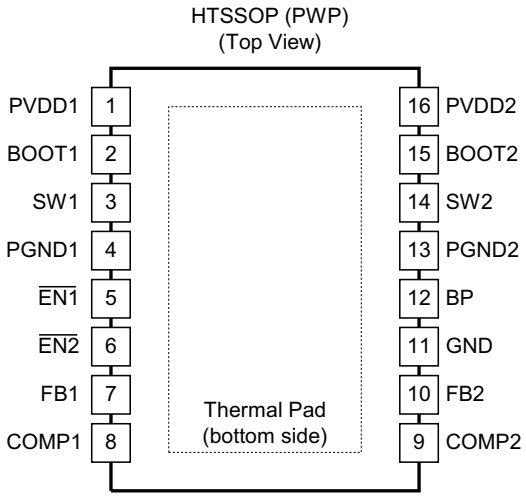


Figure 10.

DEVICE INFORMATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT1	2	I	Input supply to the high-side gate driver for Output1. Connect a 22 nF to 68 nF capacitor from this pin to SW1. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the off time of the converter. To slow down the turn ON of the internal FET, a small resistor (2 Ω to 5 Ω) may be placed in series with the bootstrap capacitor.
BOOT2	15	I	Input supply to the high-side gate driver for Output2. Connect a 22 nF to 68 nF capacitor from this pin to SW2. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the off time of the converter. To slow down the turn ON of the internal FET, a small resistor (2 Ω to 5 Ω) may be placed in series with the bootstrap capacitor.
BP	12	–	Regulated voltage to charge the bootstrap capacitors. Bypass this pin to GND with a low-ESR 4.7-µF (10-µF preferred) ceramic capacitor.
$\overline{EN1}$	5	I	Active-low enable input for Output1. If the voltage on this pin is greater than 1.5 V, Output1 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output1 and allow soft start of Output1 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND to bypass the enable function.
$\overline{EN2}$	6	I	Active-low enable input for Output2. If the voltage on this pin is greater than 1.5 V, Output2 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output2 and allow soft-start of Output2 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND to bypass the enable function.
FB1	7	I	Voltage feedback pin for Outputx. The internal transconductance error amplifier adjusts the PWM for Outputx to regulate the voltage at this pin to the internal 0.8 V reference. A series resistor divider from Outputx to ground, with the center connection tied to this pin, determines the value of the regulated output voltage.
FB2	10	I	
COMP1	8	O	Output of the transconductance (g_M) amplifier. A R-C compensation network is connected from COMPx to GND.
COMP2	9	O	
PGND1	4	–	Power ground for Outputx. It is separated from GND to prevent the switching noise coupled to the internal logic circuits.
PGND2	13	–	
GND	11	–	Analog ground pin for the device.
PVDD1	1	I	Power input to the Output1 high-side MOSFET only. This pin should be locally bypassed to PGND1 with a low ESR ceramic capacitor of 10 µF or greater. PVDD1 and PVDD2 could be tied externally together.
PVDD2	16	I	The PVDD2 pin provides power to the device control circuitry, provides the pull-up for the $\overline{EN1}$ and $\overline{EN2}$ pins and provides power to the Output2 high-side MOSFET. This pin should be locally bypassed to PGND2 with a low ESR ceramic capacitor of 10 µF or greater. The UVLO function monitors PVDD2 and enables the device when PVDD2 is greater than 4.2 V.
SW1	3	O	Source (switching) output for Output1 PWM.
SW2	14	O	Source (switching) output for Output2 PWM.
Thermal Pad		–	This pad must be tied externally to a ground plane.

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BLOCK DIAGRAM

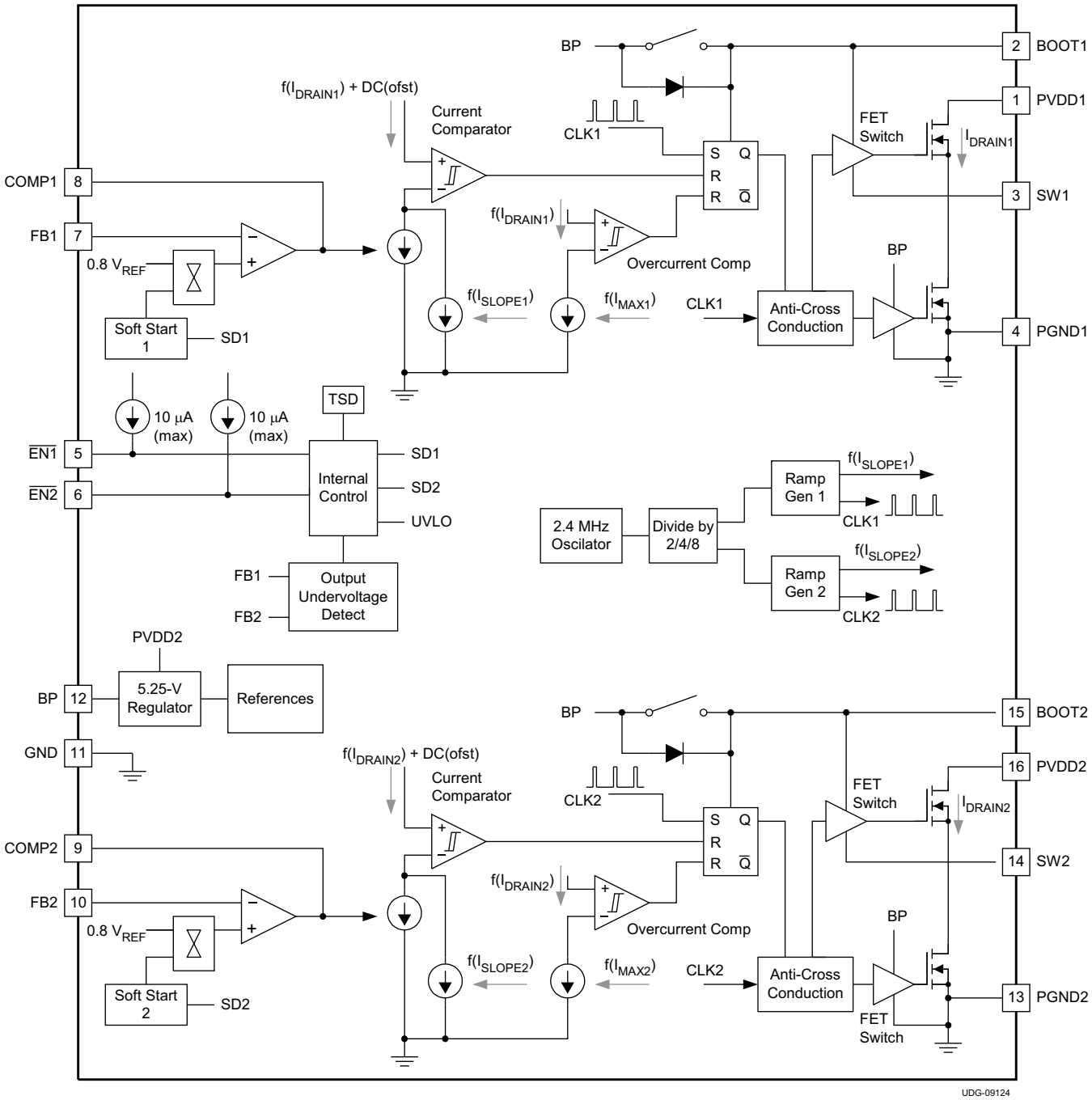


Figure 11. Block Diagram

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The TPS54290/1/2 is a dual output fully synchronous buck converter. Each PWM channel contains an error amplifier, current mode pulse width modulator (PWM), switching and rectifying MOSFETs, enable, and fault protection circuitry. Common to the two channels are the internal voltage regulator, voltage reference, and clock oscillator.

VOLTAGE REFERENCE

The band gap cell common to both outputs, trimmed to 800 mV. The reference voltage is 1% accurate in the temperature range from 0°C to 85°C.

OSCILLATOR

The oscillator frequency is internally fixed at 2.4 MHz which is divided by 8/4/2 to generate the ramps for TPS54290/1/2 respectively. The two outputs are internally configured to operate on alternating switch cycles (i.e., 180° out-of-phase).

INPUT UVLO AND STARTUP

When the voltage at the PVDD2 pin is less than 4.4 V, a portion of the internal bias circuitry is operational, and all other functions are held OFF. All of the internal MOSFETs are also held OFF. When the PVDD2 voltage rises above the UVLO turn on threshold, the state of the enable pins determines the remainder of the internal startup sequence. If either output is enabled ($\overline{ENx}$ pulled low), the BP regulator turns on, charging the BP capacitor with a 20 mA current. When the BP pin is greater than 4 V, PWM is enabled and soft-start commences.

Note that the internal regulator and control circuitry are powered from PVDD2. The voltage on PVDD1 may be higher or lower than PVDD2.

ENABLE AND TIMED TURN ON OF THE OUTPUTS

Each output has a dedicated (active low) enable pin. If left floating, an internal current source pulls the pin to PVDD2. By grounding, or by pulling the $\overline{ENx}$ pin to below approximately 1.25 V with an external circuit, the associated output is enabled and soft-start is initiated.

If both enable pins are left in the “high” state, the device operates in a shutdown mode, where the BP regulator is shut down and minimal house keeping functions are active. The total standby current from both PVDD pins is 80 µA at 12 V input supply.

An R-C connect to an $\overline{ENx}$ pin may be used to delay the turn on of the associated output after power is applied to PVDDx (see Figure 12). After power is applied to PVDD2, the voltage on the $\overline{ENx}$ pin slowly decays towards ground. Once the voltage decays to approximately 1.25 V, then the output is enabled and the startup sequence begins. If it is desired to enable the outputs of the device immediately upon the application of power to the PVDD2 pin, then omit these two components and tie the $\overline{ENx}$ pin to GND directly.

If an R-C circuit is used to delay the turn on of the output, the resistor value must be an order of magnitude less than 1.25 V/10 µA or 120 kΩ. A suggested value is 51 kΩ. This allows the $\overline{ENx}$ voltage to decay below the 1.25 V threshold while the 10-µA bias current flows.

The time to start (after the application of PVDD2) is

$$t_{START} = -R \times C \times \ln\left(\frac{\left(V_{TH} - I_{\overline{ENx}}\right) \times R}{V_{IN} - 2 \times I_{\overline{ENx}} \times R}\right) (s) \quad (1)$$

where

- R and C are the timing components
- V_{TH} is the 1.25 V enable threshold voltage
- I_{EN} is the 10-µA maximum enable pin biasing current

Figure 12 and Figure 13 illustrate startup delay with an R-C filter on the enable pin(s).

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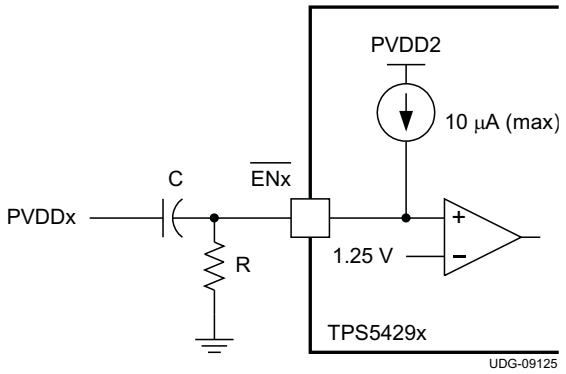


Figure 12. Startup Delay Schematic

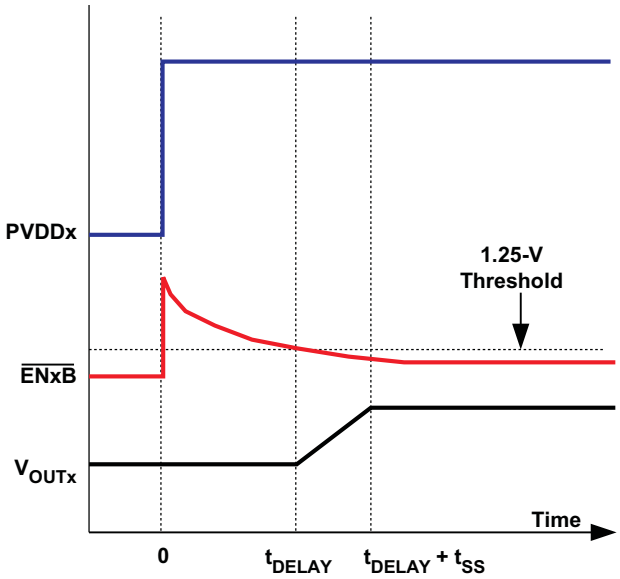


Figure 13. Startup Delay Timing Diagram

NOTE

If delayed output voltage startup is not necessary, simply connect $\overline{EN1}$ and $\overline{EN2}$ to GND. This allows the outputs to "start" immediately on the valid application of PVDD2.

If $\overline{ENx}$ is allowed to go "high" after the outputx has been in regulation, the upper and lower MOSFETs shut off, and the output decays at a rate determined by the output capacitor and the load.

SOFT START

Each output has a dedicated soft start circuit. The soft start voltage is an internal digital reference ramp to one of the two non-inverting inputs of the error amplifier. The other input is the internal precise 0.8-V reference. The total ramp time for the FB voltage to charge from 0 V to 0.8 V is about 5.2 ms, 2.6 ms and 1.3 ms for TPS54190/1/2 respectively. During a soft start interval, the TPS5429x output slowly increases the voltage to the non-inverting input of the error amplifier. In this way, the output voltage slowly ramps up until the voltage on the non-inverting input to the error amplifier reaches the internal 0.8V reference voltage. At that time, the voltage at the non-inverting input to the error amplifier remains at the reference voltage.

During the soft-start interval, pulse-by-pulse current limiting is in effect. If an over-current pulse is detected, six PWM pulses is skipped to allow the inductor current to decay before another PWM pulse is applied (See *Output Overload Protection*). There is no pulse skipping if a current limit pulse is not detected.

If the rate of rise of the input voltage (PVDDx) is such that the input voltage is too low to support the desired regulation voltage by the time soft-start has completed, then the output UV circuit may trip and cause a *hiccup* in the output voltage. In this case, use a timed delay startup from the $\overline{ENx}$ pin to delay the startup of the output until the PVDDx voltage has the capability of supporting the desired regulation voltage.

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OUTPUT VOLTAGE REGULATION

The regulation output voltage is determined by a resistor divider connecting the output node, the FBx pin, and GND (Figure 14). The value of the output voltage is shown in Equation 2.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) (V) \quad (2)$$

where

- V_{REF} is the internal 0.8-V reference voltage

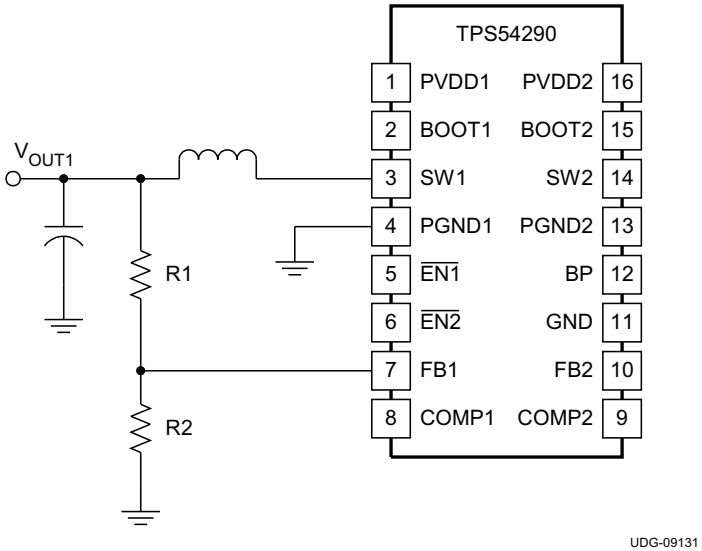


Figure 14. Feedback Network for Channel1

INDUCTOR SELECTION

Equation 3 calculates the inductance value so that the output ripple current falls from 20% to 40% of the full load current.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{OUT}} \quad (3)$$

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MAXIMUM OUTPUT CAPACITANCE

With internal pulse-by-pulse current limiting and a fixed soft-start time, there is a maximum output capacitance which may be used before startup problems begin to occur. If the output capacitance is large enough so that the device enters a current-limit protection mode during startup, then there is a possibility that the output never reaches regulation. Instead, the TPS5429x simply shuts down and attempts a restart as if the output were short-circuited to ground. The maximum output capacitance (including bypass capacitance distributed at the load) is given by

$$C_{OUT(max)} = \frac{t_{SS}}{V_{OUT}} \times \left(ILIM - I_{LOAD} - \left(\frac{I_{RIPPLE}}{2} \right) \right) \quad (4)$$

where

- t_{SS} is the soft start time
- ILIM is the current limit level

FEEDBACK LOOP COMPENSATION

In the feedback signal path, the output voltage setting divider is followed by an internal g_M-type error amplifier with a typical transconductance of 325 µS. An external series connected R-C circuit from the g_M amplifier output (COMPx pin) to ground serves as the compensation network for the converter. The signal from the error amplifier output is then buffered and combined with a slope compensation signal before it is mirrored to be referenced to the SW node. Here, it is compared with the current feedback signal to create a pulse-width-modulated (PWM) signal-fed to drive the upper MOSFET switch. A simplified equivalent circuit of the signal control path is depicted in Figure 15.

NOTE

Noise coupling from the SWx node to internal circuitry of BOOTx may impact narrow pulse width operation, especially at load currents less than 1 A.

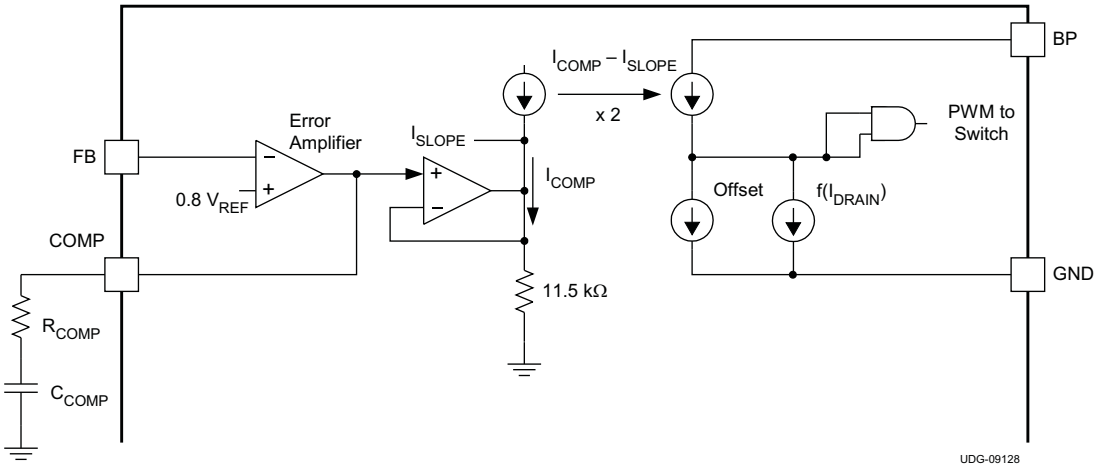


Figure 15. Feedback Loop Equivalent Circuit

A more conventional small-signal equivalent block diagram is shown in Figure 16. Here, the full closed-loop signal path is shown. Because the TPS5429x contains internal slope compensation, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability.

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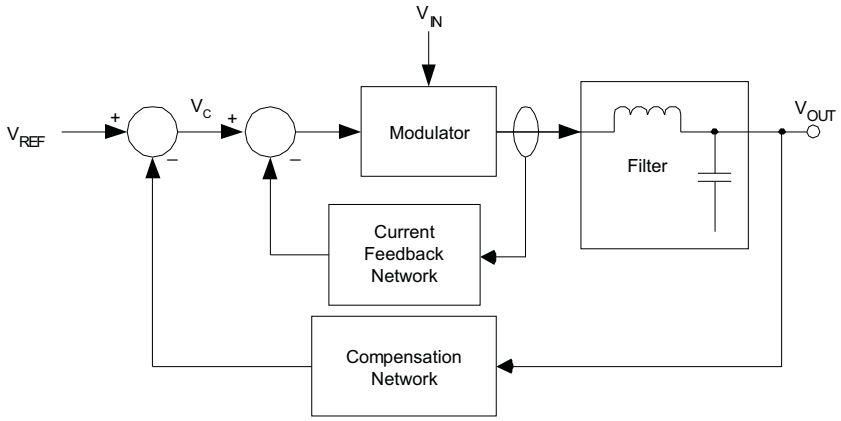


Figure 16. Small Signal Equivalent Block Diagram

To determine the components necessary for compensating the feedback loop, the controller frequency response characteristics must be understood and the desired crossover frequency selected. The best results are obtained if 10% of the switching frequency is used as this closed loop crossover frequency. In some cases, up to 20% of the switching frequency is also possible.

With the output filter components selected, the next step is to calculate the DC gain of the modulator. For TPS5429x:

$$FM_{TPS5429x} = \frac{f_{SW}}{\left(19.7 \times e^{(K \times t_{ON})} + 95 \times 10^{-6} \times \left(\frac{(V_{IN} - V_{OUT})}{L}\right)\right)} \quad (5)$$

where

- K = 5.6 ×10^5 for TPS54290
- K = 1.5 × 10^6 for TPS54291
- K = 3.6 × 10^6 for TPS54292

The overall DC gain of the converter control-to-output transfer function is approximated Equation 6.

$$f_C = \frac{V_{IN} \times FM \times 2 \times 10^{-4}}{\left(1 + \left(\frac{\left(V_{IN} \times FM \times 95 \times 10^{-6}\right)}{2 \times R_{LOAD}}\right)\right)} \quad (6)$$

The next step is to find the desired gain of the error amplifier at the desired crossover frequency. Assuming a single-pole roll-off, us Equation 6 to evaluate the following expression at the desired crossover frequency.

$$K_{EA} = -20 \times \log\left(\frac{f_C}{\left(1 + 2 \times \pi \times f_{CO} \times (2 \times R_{LOAD}) \times C_{OUT}\right)}\right) \quad (7)$$

where

- f_{CO} is the desired crossover frequency

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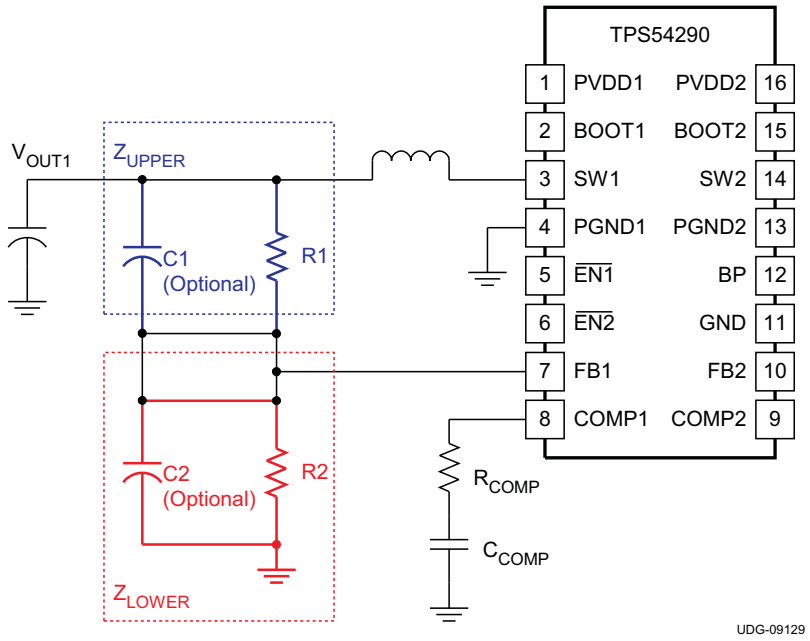


Figure 17. Loop Compensation Network

If operating at wide duty cycles (over 50%), a capacitor may be necessary across the upper resistor of the voltage setting divider. If duty cycles are less than 50%, this capacitor may be omitted.

$$C1 = \frac{\sqrt{L \times C_{OUT}}}{R1} \tag{8}$$

If a high ESR capacitor is used in the output filter, a zero appears in the loop response that could lead to instability. To compensate, a small capacitor is placed in parallel with the lower voltage setting divider resistor. The value of the capacitor is determined such that a pole is placed at the same frequency as the ESR zero. If low ESR capacitors are used, this capacitor may be omitted.

$$C2 = C_{OUT} \times \frac{ESR \times (R1 + R2)}{(R1 \times R2)} \tag{9}$$

Next, calculate the value of the error amplifier gain setting resistor and capacitor using Equation 10.

$$R_{COMP} = \frac{10^{\frac{KEA}{20}} \times (Z_{LOWER} + Z_{UPPER})}{g_M \times Z_{LOWER}} \tag{10}$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{POLE} \times R_{COMP}} \tag{11}$$

where

- $f_{POLE} = \frac{1}{2 \times \pi \times (2 \times R_{LOAD}) \times C_{OUT}}$

NOTE

Once the filter and compensation component values have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

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BOOTSTRAP FOR N-CHANNEL MOSFET

A bootstrap circuit provides a voltage source higher than the input voltage and of sufficient energy to fully enhance the switching MOSFET each switching cycle. The PWM duty cycle is limited to maximum, i.e., 90% for TPS54291, allowing an external bootstrap capacitor to charge through an internal synchronous switch (between BP and BOOTx) during every cycle. When the PWM switch is commanded to turn ON, the energy used to drive the MOSFET gate is derived from the voltage on this capacitor.

Because this is a charge transfer circuit, care must be taken in selecting the value of the bootstrap capacitor. It must be sized such that the energy stored in the capacitor on a per cycle basis is greater than the gate charge requirement of the MOSFET being used. Typically a ceramic capacitor with a value between 22nF and 68nF is selected for the bootstrap capacitor.

OUTPUT OVERLOAD PROTECTION

In the event of an overcurrent on either output after the output reaches regulation, pulse-by-pulse current limit is in effect for that output. In addition, an output under-voltage (UV) comparator monitors the FBx voltage (which follows the output voltage) to declare a fault if the output drops below 85% of regulation. During this fault condition, both PWM outputs are disabled. This ensures that both outputs discharge to GND, in the event that over-current is on one output while the other is not loaded. The converter enters a hiccup mode timeout before attempting to restart.

If an over-current condition exists during soft start, pulse-by-pulse current limiting reduces the pulse width of the affected output's PWM. In addition, if an overcurrent pulse is detected, six clock cycles are skipped before a next PWM pulse is enabled, effectively dividing the PWM frequency by six and preventing excessive current build up in the indictor. At the end of the soft start time, a UV fault is declared and the operation is the same as described above.

The overcurrent threshold for Output1 and Output2 are set nominally 2.2 A and 3.8 A respectively.

> **DESIGN HINT:** The *OCP Threshold* refers to the *peak* current in the internal switch. Be sure to add the 1/2 of the peak inductor ripple current to the DC load current in determining how close the actual operating point is to the *OCP Threshold*.

OPERATING NEAR MAXIMUM DUTY CYCLE

If the TPS5429x is operated at maximum duty cycle, and if the input voltage is insufficient to support the output voltage (at full load or during a load current transient) then there is a possibility that the output voltage falls from regulation and trip the output UV comparator. If this should occur, the TPS5429x protection circuitry declares a fault and enter hiccup mode.

> **DESIGN HINT:** Ensure that under ALL conditions of line and load regulation that there is sufficient duty cycle to maintain output voltage regulation.

DUAL SUPPLY OPERATION

It is possible to operate a TPS5429x from two supply voltages. If this application is desired, then the sequencing of the supplies must be such that PVDD2 is above the UVLO voltage before PVDD1 begins to rise. This is to ensure the internal regulator and the control circuitry is in operation before PVDD1 supplies energy to the output. In addition, Output1 must be held in the disabled state ($\overline{EN1}$ high) until there is sufficient voltage on PVDD1 to support Output1 in regulation. (See *Operating near Maximum Duty Cycle*)

The preferred sequence of events follows:

1. PVDD2 rises above the input UVLO voltage
2. PVDD1 rises with Output1 disabled until PVDD1 rises above level to support Output1 regulation

With the two conditions above satisfied, there is no restriction on PVDD2 to be greater than, or less than PVDD1.

> **DESIGN HINT:** An R-C delay on $\overline{EN1}$ may be used to delay the startup of Output1 for a long enough period of time to ensure PVDD1 can support Output1 load.

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OVER-TEMPERATURE PROTECTION AND JUNCTION TEMPERATURE RISE

The over temperature thermal protection limits the maximum power to be dissipated at a given operating ambient temperature. In other words, at a given device power dissipation, the maximum ambient operating temperature is limited by the maximum allowable junction operating temperature. The device junction temperature is a function of power dissipation, and the thermal impedance from the junction to the ambient. If the internal die temperature should reach the thermal shutdown level, the TPS5429x shuts off both PWMs and remain in this state until the die temperature drops below 125°C, at which time the device restarts.

The first step in determining the device junction temperature is to calculate the power dissipation. The power dissipation is dominated by the two switching MOSFETs and the BP internal regulator. The power dissipated by each MOSFET is composed of conduction losses and switching losses. The total conduction loss in the high side and low side MOSFETs for each channel is given by Equation 12.

$$P_{D(cond)} = \left(R_{DS(on)HS} \times D + R_{DS(on)LS} \times (1-D)\right) \times \left(I_O^2 + \frac{\Delta I_O^2}{12}\right) \quad (12)$$

where

- I_O is the DC output current,
- ΔI_O is the peak-to-peak ripple current in the inductor

Notice the impact of operating duty cycle on the result.

The switching loss for each channal is approximated by Equation 13.

$$P_{D(SW)} = \frac{V_{IN}^2 \times \left(C_{OSS}(HS) + C_{OSS}(LS)\right) \times f_S}{2} \quad (13)$$

where

- $C_{OSS(HS)}$ is the output capacitance of the high-side MOSFET
- $C_{OSS(LS)}$ is the output capacitance of the low-side MOSFET
- f_S is the switching frequency

The total power dissipation is found by summing the power loss for both MOSFETs plus the loss in the internal regulator.

$$P_D = P_{D(cond)output1} + P_{D(SW)output1} + P_{D(cond)output2} + P_{D(SW)output2} + V_{IN} \times Iq \quad (14)$$

The temperature rise of the device junction is dependent on the thermal impedance from junction to the mounting pad (See *Package Dissipation Ratings*), plus the thermal impedance from the thermal pad to ambient. The thermal impedance from the thermal pad to ambient is dependent on the PCB layout (PowerPAD interface to the PCB, the exposed pad area) and airflow (if any). See *PCB Layout Guidelines, Additional References*.

The operating junction temperature is shown in Equation 15.

$$T_J = T_A + P_D \times \left(\theta_{TH(pkg)} + \theta_{TH(pad-amb)}\right) \quad (15)$$

where

- θth is the thermal impedance

BYPASSING AND FILTERING

As with any integrated circuit, supply bypassing is important for jitter free operation. To improve the noise immunity of the converter, ceramic bypass capacitors must be placed as close to the package as possible.

- PVDD1 to GND – Use a 10 µF ceramic capacitor
- PVDD2 to GND – Use a 10 µF ceramic capacitor
- BP to GND – Use a 4.7 µF Ceramic capacitor

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POWER DERATING

The TPS5429x delivers full current at wide duty cycles at ambient temperatures up to 85°C if the thermal impedance from the thermal pad is sufficient to maintain the junction temperature below the thermal shut down level. At higher ambient temperatures, the device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 18 illustrates the power derating for elevated ambient temperature under various air flow conditions. Note that these curves assume the PowerPAD is soldered to the recommended thermal pad. See *References* for further information.

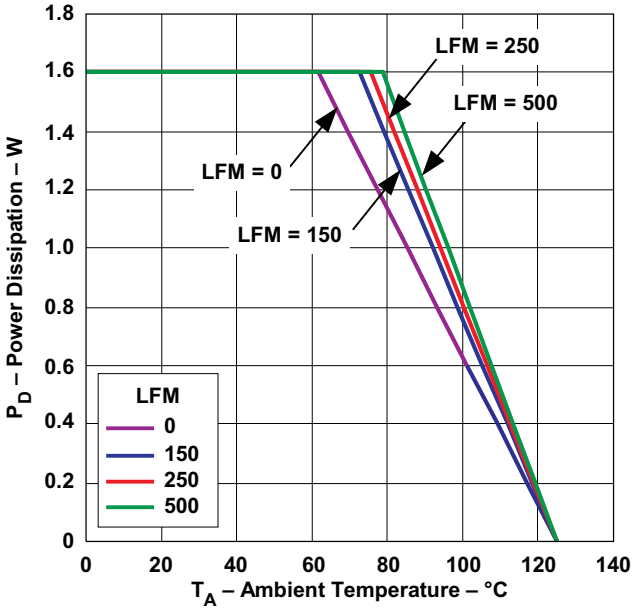


Figure 18. Power Derating Curves

PowerPAD PACKAGE

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD package. Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. (See *Additional References*)

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LAYOUT RECOMMENDATIONS

- The PowerPad must be connected to the low-current ground with available surface copper to dissipate heat. Extending ground land beyond the device package area between PVDD1 (pin 1) and PVDD2 (pin 16) and between COMP1 (pin 8) and COMP2(pin 9) is recommended..
- Connect PGND1 and PGND2 to the PowerPad through a 10-mil wide trace.
- Place the ceramic input capacitors near PVDD1 and PVDD2 and bypass to PGND1 and PGND2 respectively.
- Locate the inductor near the SW1 or SW2 pin.
- Connect the output capacitor grounds to PGND1 or PGND2 with wide, tight loops.
- Use a wide ground connection from input capacitor PGND1 or PGND2 as close to power path as possible. It is recommend they be placed directly underneath.
- Locate the bootstrap capacitor near the BOOT pin to minimize gate drive loop.
- Locate the feedback and compensation components far from switch node and input capacitor ground connection.
- Locate the snubber components from SW1 or SW2 to PGND1 or PGND2 close to the device, minimizing the loop area.
- Locate the BP bypass capacitor very close to device and bypass to PowerPad. Locate output ceramic capacitor close to inductor output terminal and between inductor and electrolytic capacitors if used.

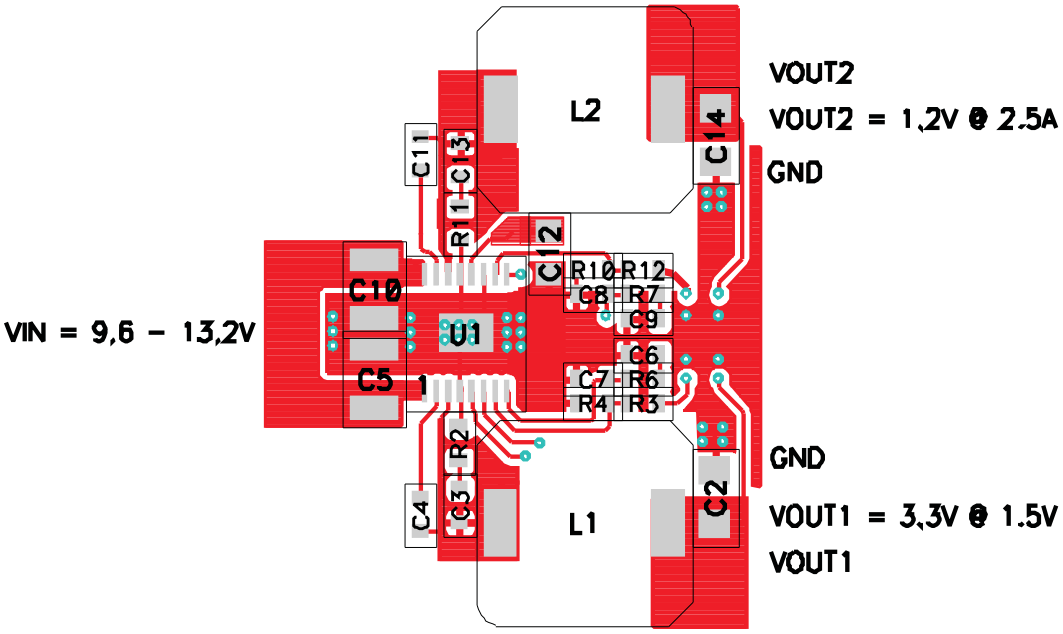


Figure 19. Top Layer

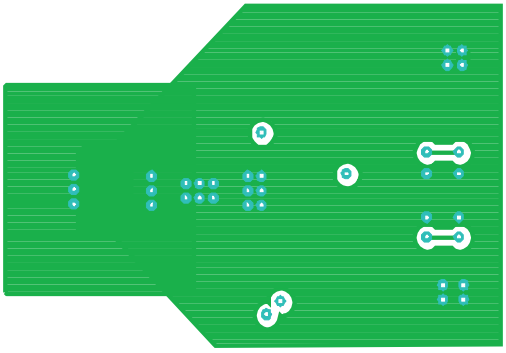


Figure 20. Bottom Layer

DESIGN EXAMPLES

Design Example 1

The following example illustrates the design process and component selection for a 12-V to 5-V and 3.3-V dual non-synchronous buck regulator using the TPS54291 converter. A definition of symbols used can be found in Table 1 of the appendix

Table 1. Design Example Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERSTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = Nom, I_{OUT} = Max				A
	No load input current	V_{IN} = Nom, I_{OUT} = 0 A		12	20	mA
$V_{IN(UVLO)}$	Input UVLO	I_{OUT} = Min to Max	4	4.2	4.4	V
OUTPUT CHARACTERSTICS						
V_{OUT1}	Output voltage 1	V_{IN} = Nom, I_{OUT} = Nom	3.2	3.3	3.4	V
V_{OUT2}	Output voltage 2	V_{IN} = Nom, I_{OUT} = Nom	1.15	1.20	1.25	V
	Line regulation	VIN = Min to Max			1%	
	Load regulation	I_{OUT} = Min to Max			1%	
$V_{OUT1(ripple)}$	Output1 voltage Ripple	V_{IN} = Nom, I_{OUT1} = Max			50	mV_{PP}
$V_{OUT2(ripple)}$	Output2 voltage Ripple	V_{IN} = Nom, I_{OUT2} = Max			24	mV_{PP}
I_{OUT1}	Output current 1	V_{IN} = Min to Max	0		1.5	A
I_{OUT2}	Output current 2	V_{IN} = Min to Max	0		2.5	A
I_{OCP1}	Output overcurrent Channel 1	V_{IN} = Nom, V_{OUT} = (V_{OUT1} – 5%)	1.8	2.2	2.6	A
I_{OCP2}	Output overcurrent Channel 2	V_{IN} = Nom, V_{OUT} = (V_{OUT2} – 5%)	3.2	3.8	4.6	A
TRANSIENT RESPONSE						
ΔV_{OUT}	Change from load transient	ΔI_{OUT} = 1 A @ 3 µA/s		200		mV
	Settling time	to 1% of V_{OUT}		1		ms
SYSTEMS CHARACTERSTICS						
f_{SW}	Switching frequency		500	600	700	kHz
η_{PEAK}	Peak efficiency	V_{IN} = Nom		90%		
η	Full load efficiency	V_{IN} = Nom, I_{OUT} = Max		80%		
T_{OP}	Operating temperature range	V_{IN} = Min to Max, I_{OUT} = Min to Max	0	25	60	°C

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The list of materials for this application is shown below in Table 2. The efficiency, line regulation and load regulation from printed circuit boards built using this design are shown in Figure 23 and Figure 24.

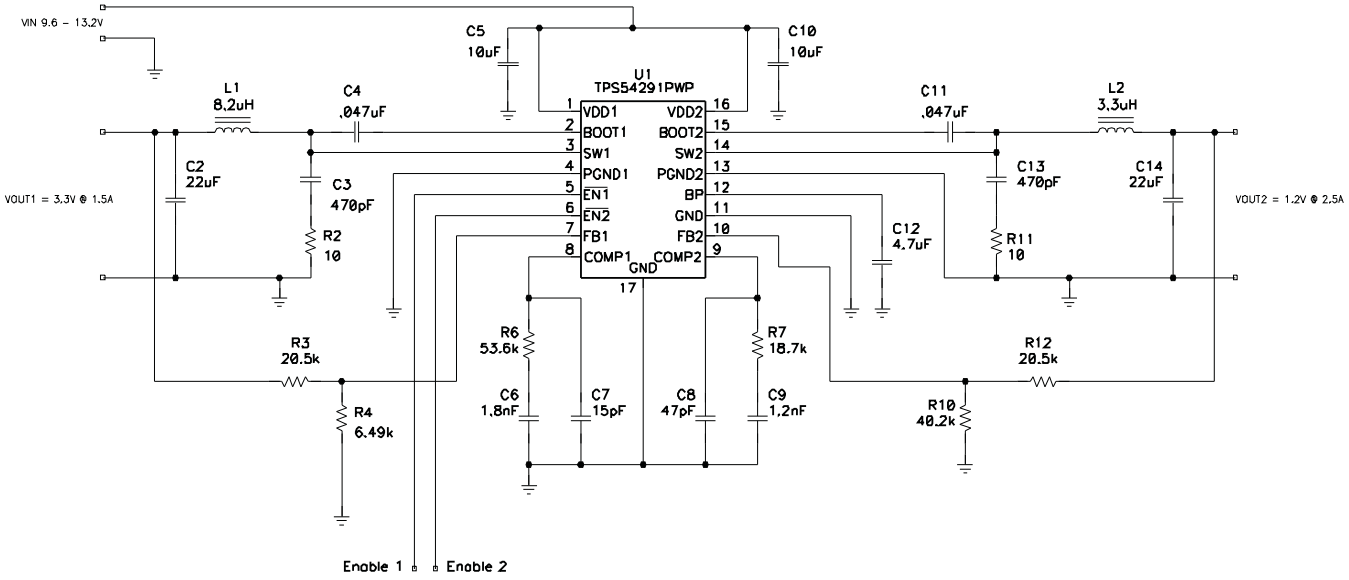


Figure 21. TPS54291 Design Example 1 Schematic

Step by Step Design Procedure

Duty Cycle Estimation

The duty cycle of the main switching FET is estimated by Equation 16 and Equation 17.

$$D_{MAX1} \approx \frac{V_{OUT}}{V_{IN(min)}} = \frac{3.3}{8.0} = 0.413 \longrightarrow D_{MAX2} \approx \frac{V_{OUT}}{V_{IN(min)}} = \frac{1.2}{8.0} = 0.15 \quad (16)$$

$$D_{MIN1} \approx \frac{V_{OUT}}{V_{IN(max)}} = \frac{3.3}{14} = 0.236 \longrightarrow D_{MIN2} \approx \frac{V_{OUT}}{V_{IN(max)}} = \frac{1.2}{14} = 0.086 \quad (17)$$

Inductor Selection

The peak to peak ripple should be limited to between 20% and 30% of the maximum output current.

$$I_{Lrip1(max)} = 0.30 \times I_{OUT(max)} = 0.3 \times 1.5\,A = 0.450\,A \quad (18)$$

$$I_{Lrip2(max)} = 0.30 \times I_{OUT(max)} = 0.3 \times 2.5\,A = 0.750\,A \quad (19)$$

The minimum inductor size can be estimated by Equation 20 and Equation 21.

$$L_{MIN1} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14 - 3.3}{0.45\,A} \times 0.236 \times \frac{1}{600\,kHz} = 9.35\,\mu H \quad (20)$$

$$L_{MIN2} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14 - 1.2}{0.75\,A} \times 0.086 \times \frac{1}{600\,kHz} = 2.45\,\mu H \quad (21)$$

The standard inductor values of 8.2 µH and 3.3 µH are selected for Channel 1 and Channel 2 respectively. The actual ripple currents are estimated by Equation 22 and Equation 23.

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$$I_{RIPPLE1} \approx \frac{V_{IN(max)} - V_{OUT}}{L1} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14 - 3.3}{8.2\,\mu H} \times 0.236 \times \frac{1}{600\,kHz} = 0.513\,A \quad (22)$$

$$I_{RIPPLE2} \approx \frac{V_{IN(max)} - V_{OUT}}{L2} \times D_{MIN} \times \frac{1}{f_{SW}} = \frac{14 - 1.2}{3.3\,\mu H} \times 0.086 \times \frac{1}{600\,kHz} = 0.556A \quad (23)$$

The RMS current through the inductor is approximated by Equation 24 and Equation 25.

$$I_{L(rms)} = \sqrt{I_{L(avg)}^2 + \tfrac{1}{12} I_{RIPPLE}^2} \approx \sqrt{I_{OUT(max)}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{(1.5)^2 + \tfrac{1}{12}(0.513)^2}\,A = 1.51A \quad (24)$$

$$I_{L(rms)} = \sqrt{I_{L(avg)}^2 + \tfrac{1}{12} I_{RIPPLE}^2} \approx \sqrt{I_{OUT(max)}^2 + \tfrac{1}{12} I_{RIPPLE}^2} = \sqrt{(2.5)^2 + \tfrac{1}{12}(0.556)^2}\,A = 2.51A \quad (25)$$

A DC current with 30% peak-to-peak ripple has an RMS current approximately 0.4% above the average current.

The peak inductor current is estimated by Equation 26 and Equation 27.

$$I_{L(peak)} \approx I_{OUT(max)} + \tfrac{1}{2} I_{RIPPLE} = 1.5\,A + \tfrac{1}{2}\,0.513A = 1.76\,A \quad (26)$$

$$I_{L(peak)} \approx I_{OUT(max)} + \tfrac{1}{2} I_{RIPPLE} = 2.5\,A + \tfrac{1}{2}\,0.556A = 2.78\,A \quad (27)$$

A 8.2-µH inductor with a minimum RMS current rating of 1.51 A and minimum saturation current rating of 3.7 A must be selected. A Coilcraft MSS1048-822ML 8.2-µH, 4.38-A inductor is chosen for Channel 1 and a Coilcraft MSS1048-332 3.3-µH inductor is chosen for Channel 2.

Output Capacitor Selection

Output capacitors are selected to support load transients and output ripple current. The minimum output capacitance to meet the transient specification is given by Equation 28 and Equation 29.

$$C_{OUT1(min)} = \frac{I_{TRAN(max)}^2 \times L}{(V_{OUT}) \times V_{OVER}} = \frac{1A^2 \times 8.2\,\mu H}{3.3\,V \times 0.2\,V} = 12.4\,\mu F \quad (28)$$

$$C_{OUT2(min)} = \frac{I_{TRAN(max)}^2 \times L}{(V_{OUT}) \times V_{OVER}} = \frac{1A^2 \times 3.3\,\mu H}{1.2\,V \times 0.2\,V} = 13.7\,\mu F \quad (29)$$

The maximum ESR to meet the ripple specification is given by Equation 30 and Equation 31.

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{0.050\,V - \left(\frac{0.513\,A}{8 \times 12.4\,\mu F \times 600\,kHz}\right)}{0.513\,A} = 0.081\,\Omega \quad (30)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{0.024\,V - \left(\frac{0.556\,A}{8 \times 13.7\,\mu F \times 600\,kHz}\right)}{0.556\,A} = 0.028\,\Omega \quad (31)$$

A single 22-µF ceramic capacitor with approximately 2.5 mΩ of ESR is selected to provide sufficient margin for capacitance loss due to DC voltage bias.

Input Capacitor Selection

A minimum 10-µF ceramic input capacitor on each PVDD pin is recommended. The ceramic capacitor must handle the RMS ripple current in the input capacitor.

The RMS current in the input capacitors is estimated by Equation 32 and Equation 33.

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$$I_{RMS(CIN1)} = I_{OUT1} \times \sqrt{D_1 \times (1 - D_1)} = 1.5\,A \times \sqrt{0.413 \times (1 - 0.413)} = 0.74\,A \quad (32)$$

$$I_{RMS(CIN2)} = I_{OUT1} \times \sqrt{D_2 \times (1 - D_2)} = 2.5\,A \times \sqrt{0.15 \times (1 - 0.15)} = 0.89\,A \quad (33)$$

One 1210 10-µF, 25-V, X5R, ceramic capacitor with 2-mΩ ESR and a 2-A RMS current rating are selected for each PVDD input. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors will have sufficient capacitance at the working voltage.

Feedback

The primary feedback divider resistor (R_{FB}) from VOUT to FB should be selected between 10-kΩ and 100-kΩ to maintain a balance between power dissipation and noise sensitivity. For a 3.3-V and 5-V output, 20.5 kΩ is selected and the lower resistor is given by Equation 34.

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{V_{OUT} - V_{FB}} \quad (34)$$

For R_{FB} = 20.5kΩ and V_{FB} = 0.80 V, R_{BIAS} = 6.56 kΩ and 41.0 kΩ (6.49 kΩ and 40.2 kΩ selected) for 3.3 V and 1.2 V respectively. It is common to select the next lower available resistor value for the bias resistor. This biases the nominal output voltage slightly higher, allowing additional tolerance for load regulation.

Compensation Components

The TPS54291 controller uses a transconductance error amplifier, which is compensated with a series capacitor and resistor to ground plus a high-frequency capacitor to reduce the gain at high frequency. To select the component, the following equations define the control loop and power stage gain and transfer function:

$$FM_{TPS5429x} = \frac{f_{SW}}{\left[19.7 \times e^{(K \times t_{ON})} + 95 \times 10^{-6} \times \left(\frac{V_{IN} - V_{OUT}}{L}\right)\right]} = \frac{600\,kHz}{\left[19.7 \times e^{(1.5 \times 10^6 \times 393ns)} + 95 \times 10^{-6} \times \left(\frac{14 - 3.3}{8.2\,\mu H}\right)\right]} = 3762 \quad (35)$$

where

- K = 5.6 × 10^5 for TPS54290
- K = 1.5 × 10^6 for TPS54291
- K = 3.6 × 10^6 for TPS54292

The overall DC gain of the converter control-to-output transfer function is approximated by Equation 36.

$$f_C = \frac{V_{IN} \times FM \times 2 \times 10^{-4}}{\left[1 + \left(\frac{V_{IN} \times FM \times 95 \times 10^{-6}}{2 \times R_{LOAD}}\right)\right]} = \frac{14\,V \times 3762 \times 2 \times 10^{-4}}{\left[1 + \left(\frac{14\,V \times 3762 \times 95 \times 10^{-6}}{4.4\,\Omega}\right)\right]} = 4.293 \quad (36)$$

With the power stage DC gain, it is possible to estimate the required mid-band gain to program a desired cross-over frequency.

$$K_{EA} = -20 \times \log\left(\frac{f_C}{1 + 2 \times \pi \times f_{CO} \times (2 \times R_{LOAD}) \times C_{OUT}}\right) = -20 \times \log\left(\frac{3.22}{1 + 2 \times \pi \times 30\,kHz \times 4.4\,\Omega \times 22\,\mu F}\right) = 11.83\,dB \quad (37)$$

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Compensation Gain Setting Resistor

R_{COMP} programs the mid-band error amplifier gain to set the desired cross-over frequency in Equation 38.

$$R_{COMP} = \frac{10^{\frac{KEA}{20}} \times (Z_{LOWER} + Z_{UPPER})}{g_M \times Z_{LOWER}} = \frac{10^{\frac{11.83dB}{20}} \times (6.49k\Omega + 20.5k\Omega)}{325\mu S \times 6.49k\Omega} = 50.42k\Omega \approx 53.6k\Omega \quad (38)$$

Compensation Integrator Capacitor

An integrator capacitor provides maximum DC gain for the best possible DC regulation while programming the compensation zero to match the natural pole of the output filter. C_{COMP} is selected by Equation 40.

$$f_{POLE} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} = \frac{1}{2 \times \pi \times 4.4\Omega \times 22\mu F} = 1.644kHz \quad (39)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{POLE} \times R_{COMP}} = \frac{1}{2 \times \pi \times 1.644kHz \times 53.6k\Omega} = 1.80nF \quad (40)$$

Bootstap Capacitor

To ensure proper charging of the high-side FET gate and limit the ripple voltage on the boost capacitor, a 47-nF boot strap capacitor is recommended.

Power Dissipation

The power dissipation in the TPS54291 is made from FET conduction losses, switching losses and regulator losses.

Conduction losses are estimated by Equation 41 and Equation 42.

$$P_{CON1} = \left(R_{DS(on)HS} \times D_1 + R_{DS(on)LS} \times (1 - D_1)\right) \times \left(I_{SW1(RMS)}\right)^2 = (150m\Omega \times 0.413 + 100m\Omega \times 0.587) \times (1.51)^2 = 0.275W \quad (41)$$

$$P_{CON2} = \left(R_{DS(on)HS} \times D_1 + R_{DS(on)LS} \times (1 - D_1)\right) \times \left(I_{SW1(RMS)}\right)^2 = (105m\Omega \times 0.15 + 75m\Omega \times 0.85) \times (2.51)^2 = 0.501W \quad (42)$$

The switching losses are estimated by Equation 43 and Equation 44.

$$P_{SW1} \approx \frac{V_{IN(max)}^2 \times (C_{OSS(HS)} + C_{OSS(LS)}) \times f_{SW}}{2} = \frac{14^2 \times (140pF + 200pF) \times 600kHz}{2} = 20mW \quad (43)$$

$$P_{SW2} \approx \frac{V_{IN(max)}^2 \times (C_{OSS(HS)} + C_{OSS(LS)}) \times f_{SW}}{2} = \frac{14^2 \times (200pF + 280pF) \times 600kHz}{2} = 28mW \quad (44)$$

The regulator losses are estimated by Equation 45.

$$P_{REG} \approx I_{DD} \times V_{IN(max)} + I_{BP} \times \left(V_{IN(max)} - V_{BP}\right) = 10mA \times 14V = 140mW \quad (45)$$

Total power dissipation in the device is the sum of conduction losses and switching losses for both channels plus regulator losses, which is estimated to be 1.01 W.

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Design Example Test Results

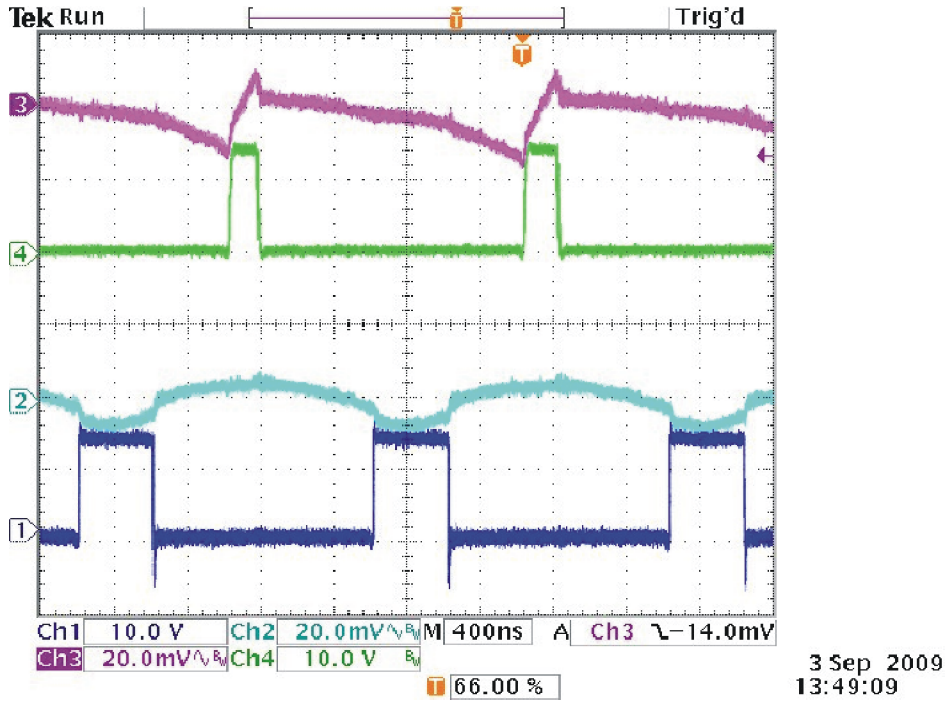


Figure 22. TPS54291 Design Example Switching Waveforms

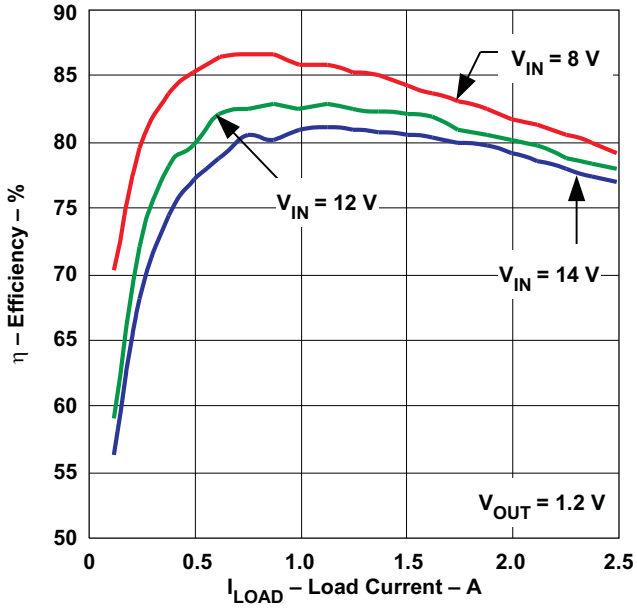


Figure 23. Design Efficiency for 1.2-V Output

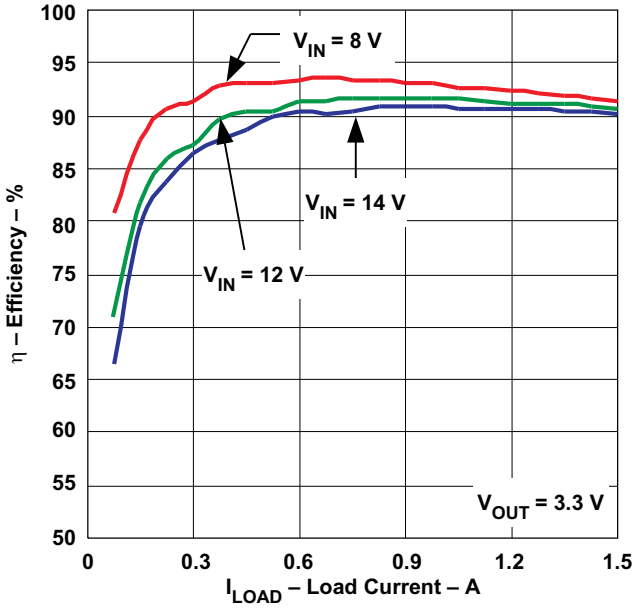


Figure 24. Design Efficiency for 3.3-V Output

Table 2. Design Example List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C12	1	4.7 µF	Capacitor, Ceramic, 10 V, X5R, 20%	0805	Std	Std
C2, C14	2	22 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1206	C3216X5R0J226M	TDK
C3, C13	2	470 pF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
C4, C11	2	0.047 µF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
C5, C10	2	10 µF	Capacitor, Ceramic, 25 V, X5R, 20%	1210	C3225X5R1E106 M	TDK
C6	2	1.8 nF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
C7	1	15 pF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
C8	1	47 pF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
C9	1	1.2 nF	Capacitor, Ceramic, 25 V, X7R, 20%	0603	Std	Std
L1	1	8.2 µH	Inductor, SMT, 4.38 A, 20 mΩ	0.402 x 0.394 inch	MSS1048-822L	Coilcraft
L2	1	3.3 µH	Inductor, SMT, 5.04 A, 10 mΩ	0.402 x 0.394 inch	MSS1048-332L	Coilcraft
R10	1	40.2 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2, R11	2	10 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
R3, R12	2	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	1	6.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	1	7.87 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R7	1	4.64 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
U1	1	2.5 A/1.5 A, 600 Hz	Dual Output Fully Synchronous Buck Converter w/Integrated FET	CSP	TPS54291PWP	TI

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Design Example 2 (Cascading Operation)

TPS5429x can be configured as cascaded operation as shown in Figure 25. The 12-V input supply is applied to PVDD2 and the the channel 2 output is tied to PVDD1. The channel 2 output is 3.3 V and capable of supporting 1.5 A to the load while generating power for the 1.2-V input for channel 1.

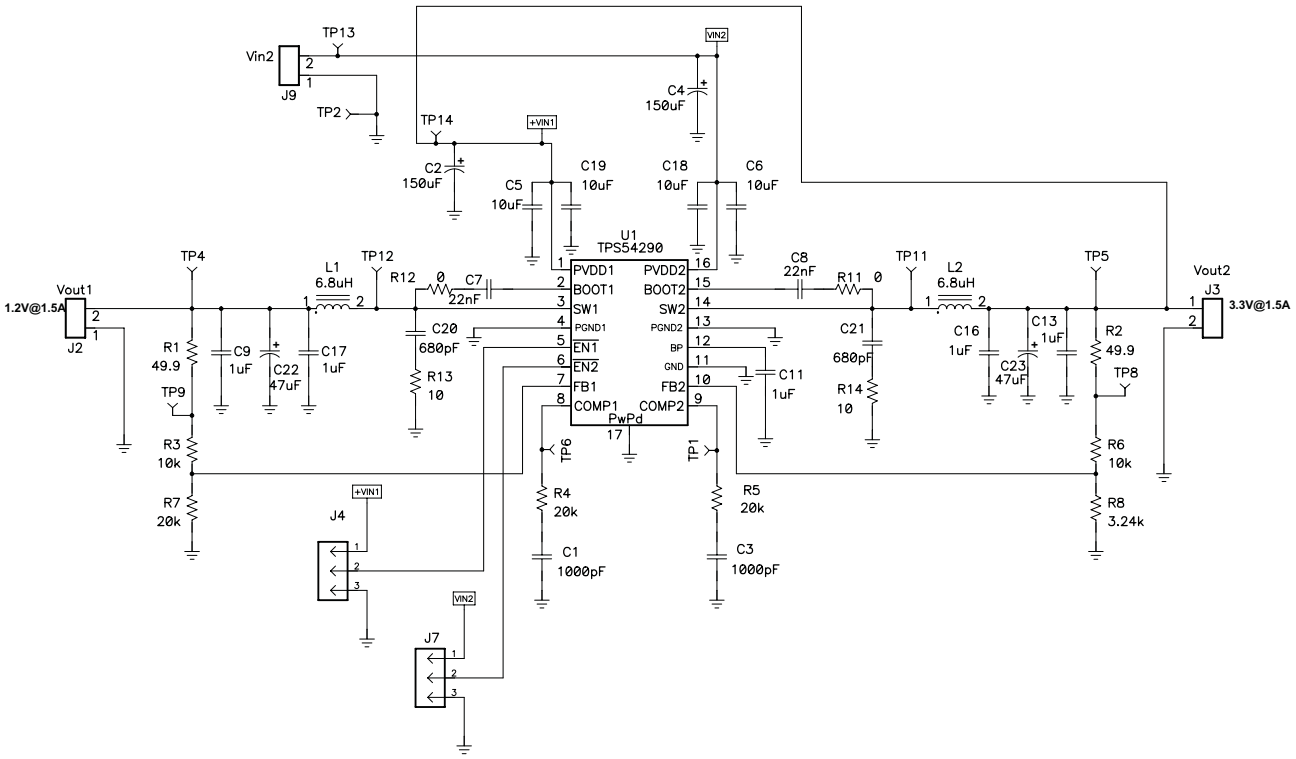


Figure 25. Cascading Operation

Design Example 2 Test Results

For Figure 26, Ch1: 12-V supply; Ch2: V_{OUT1} (1.2 V); Ch3: V_{OUT2}(3.3 V). For Figure 27, Ch1: Channel 1 SW node; Ch2: Channel 1 output ripple Ch3: Channel 2 output ripple; Ch2: Channel 2 SW node.

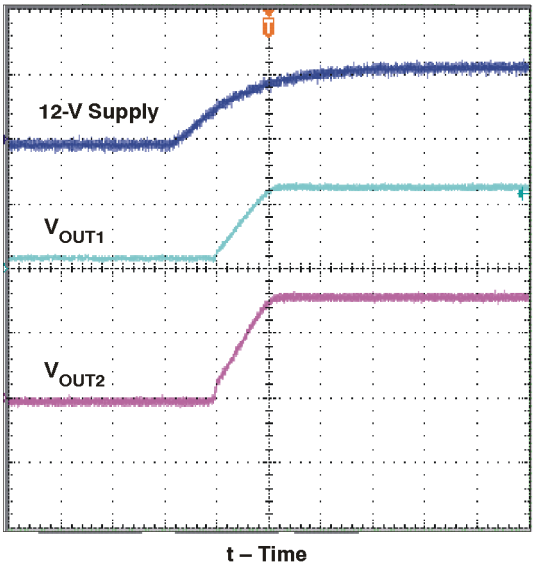


Figure 26. Start-Up Waveforms

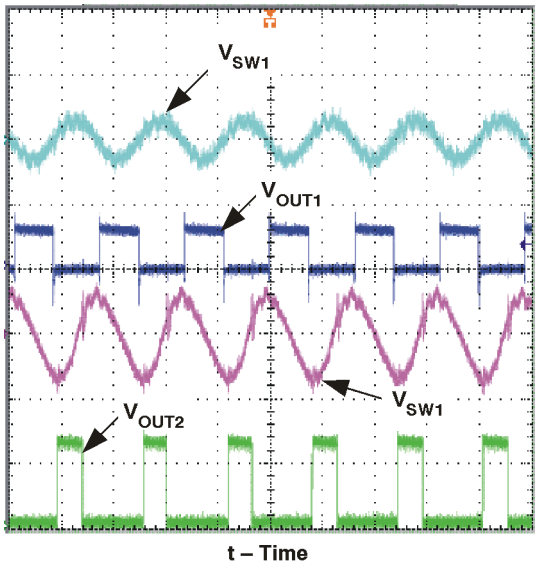


Figure 27. Output Ripple and SW Nodes

ADDITIONAL REFERENCES

RELATED DEVICES

The following devices have characteristics similar to the TPS54290/1/2 and may be of interest.

DEVICE	DESCRIPTION
TPS40222	5-V input, 1.5-A, Non-Synchronous Buck Converter
TPS54283/TPS54286	2-A DUAL NON-SYNCHRONOUS CONVERTER WITH INTEGRATED HIGH-SIDE FET
TPS55383/TPS55386	3-A DUAL NON-SYNCHRONOUS CONVERTER WITH INTEGRATED HIGH-SIDE FET

REFERENCES

These references, design tools and links to additional references, including design software, may be found at www.power.ti.com.

1. Additional PowerPAD™ information may be found in Applications Briefs (SLMA002A) and (SLMA004).
2. *Under The Hood Of Low Voltage DC/DC Converters* – SEM1500 Topic 5 – 2002 Seminar Series
3. *Understanding Buck Power Stages in Switchmode Power Supplies*, (SLVA057), March 1999
4. *Designing Stable Control Loops* – SEM 1400 – 2001 Seminar Series

Package Outline and Recommended PCB Footprint

The following pages outline the mechanical dimensions of the 16-pin PWP package and provide recommendations for PCB layout.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS54290PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54290PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54291PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54291PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54292PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54292PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

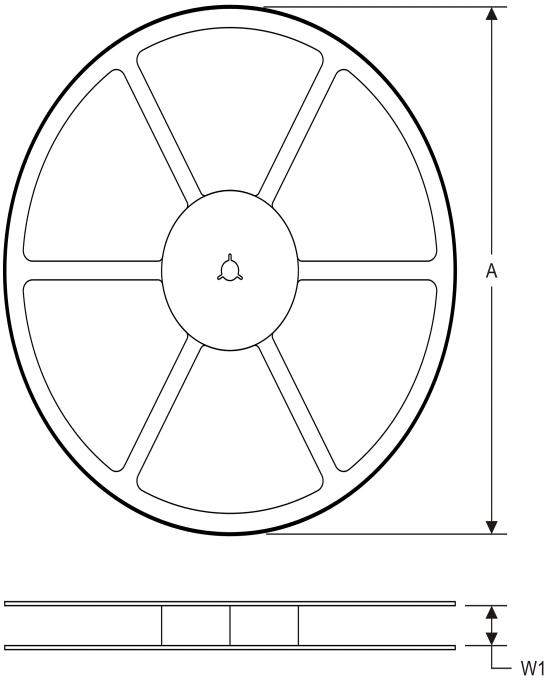
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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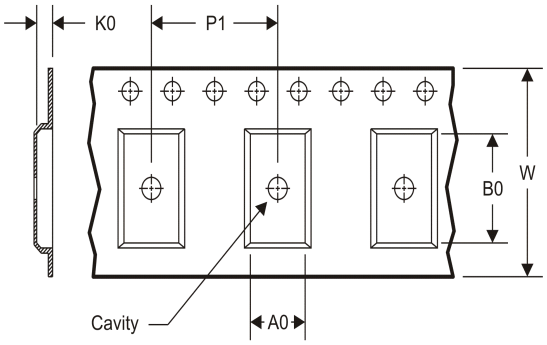
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



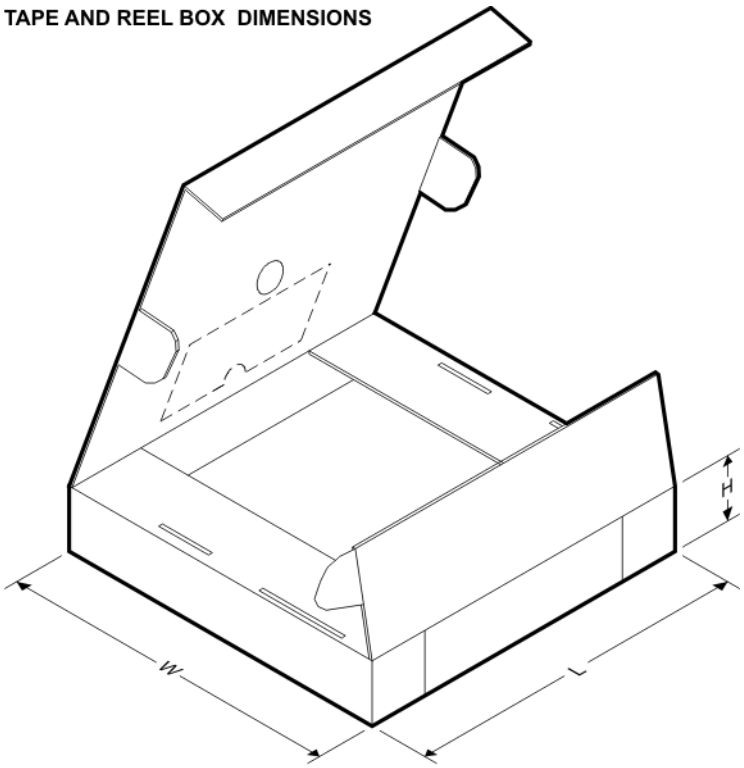
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54290PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54292PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

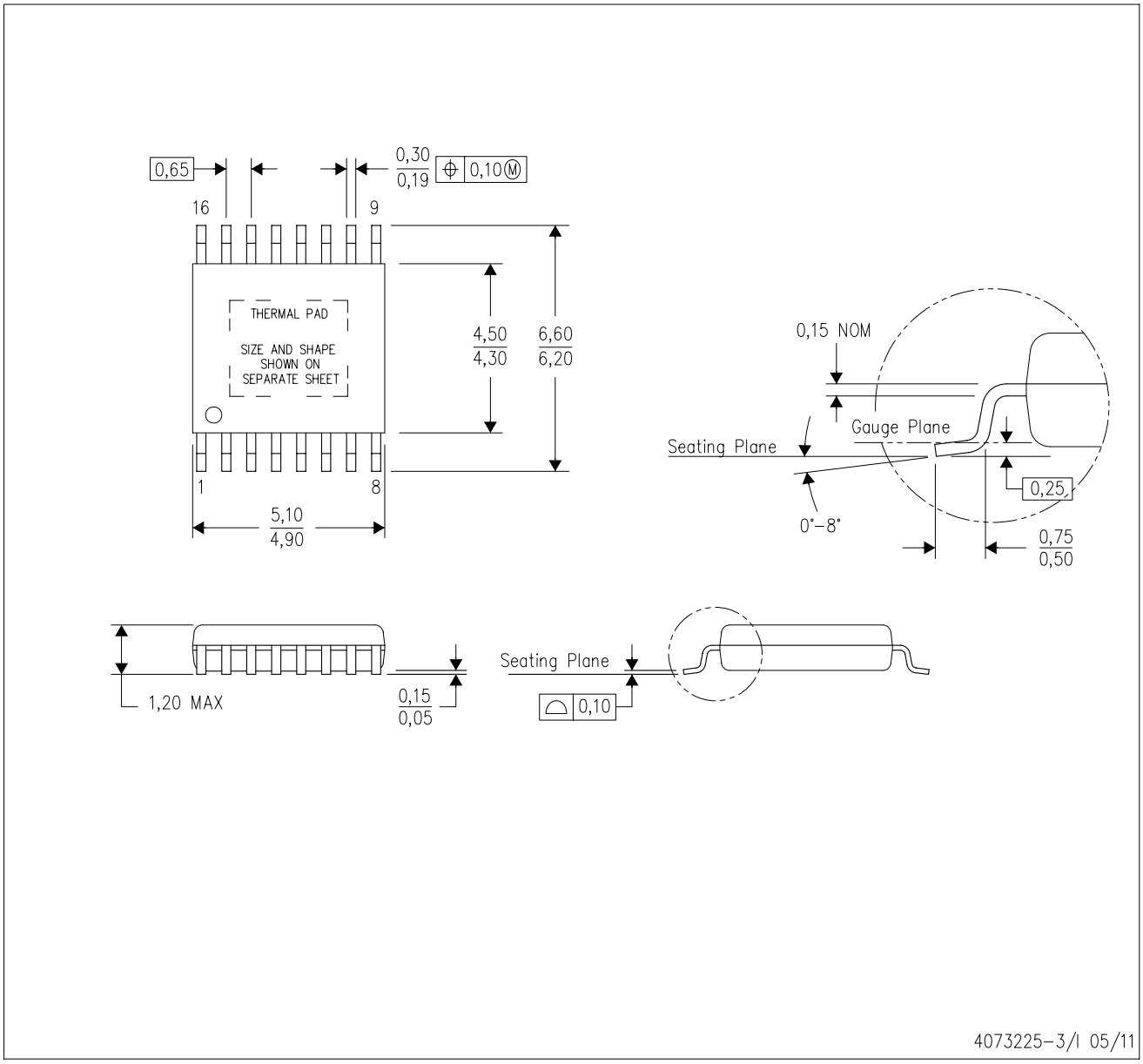
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54290PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0
TPS54292PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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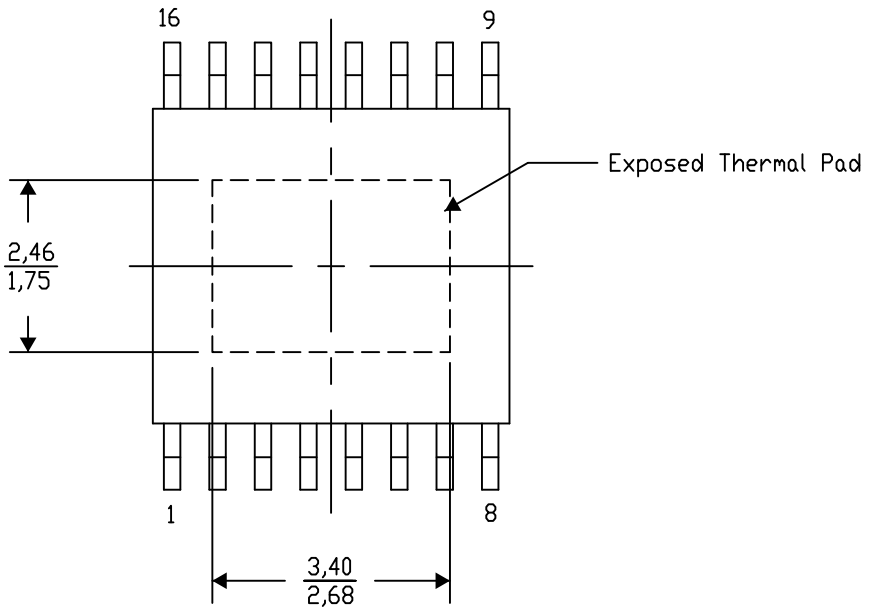
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

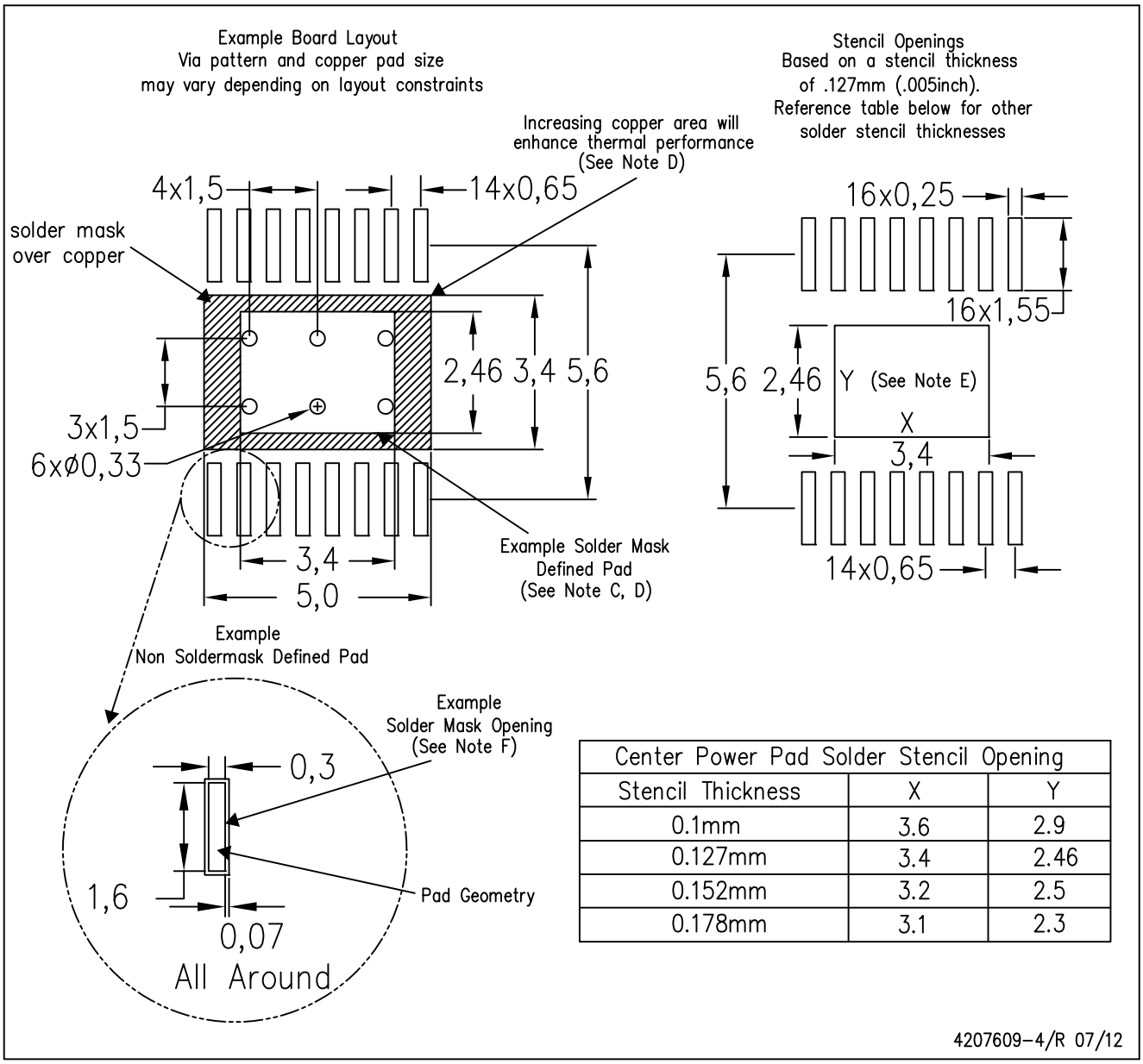
Exposed Thermal Pad Dimensions

4206332–7/AC 07/12

NOTE: A. All linear dimensions are in millimeters

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PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.9
0.127mm	3.4	2.46
0.152mm	3.2	2.5
0.178mm	3.1	2.3

4207609–4/R 07/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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