

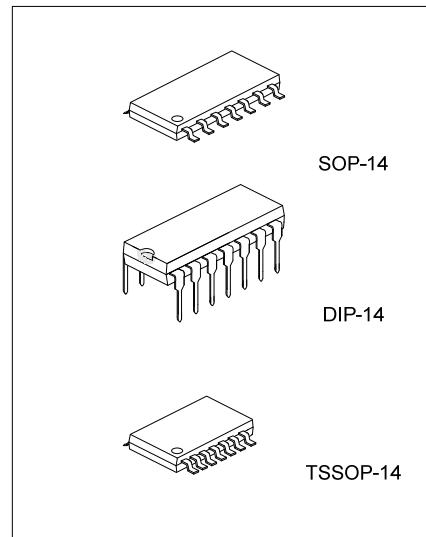
## QUAD BILATERAL SWITCH

## ■ DESCRIPTION

The UTC **4066** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals.

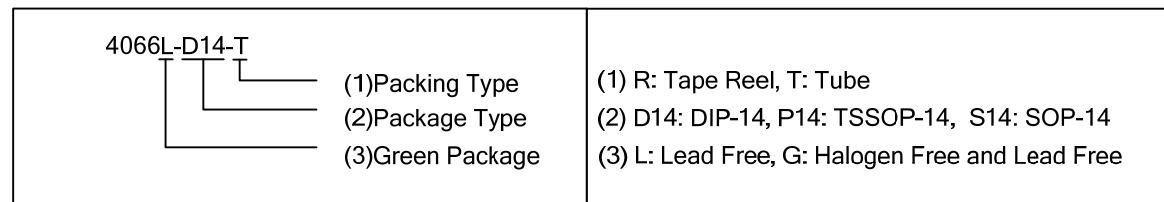
## ■ FEATURES

- \* Wide supply voltage range: 3V ~ 15V.
- \* High noise immunity : 0.45V<sub>DD</sub> (typ.)
- \* Wide range of digital and  $\pm 7.5V_{PEAK}$  analog switching
- \* "ON" resistance for 15V operation : 80Ω
- \* Matched "ON" resistance :  $\Delta R_{ON}=5\Omega$  (typ.) over 15V signal input
- \* "ON" resistance flat over peak-to-peak signal range
- \* High "ON" / "OFF" : 65 dB (typ.) output voltage ratio @  $f_{IS}=10\text{kHz}$ ,  $R_L=10\text{k}\Omega$
- \* High degree linearity: 0.1% distortion (typ.). @  $f_{IS}=1\text{kHz}$ ,  $V_{IS}=5\text{Vp-p}$ .
- \*  $V_{DD}-V_{SS}=10\text{V}$ ,  $R_L=10\text{k}\Omega$
- \* Extremely low "OFF" : 0.1nA (typ.)
- \* switch leakage @  $V_{DD}-V_{SS}=10\text{V}$ ,  $T_A=25^\circ\text{C}$
- \* Extremely high control input impedance :  $10^{12}\Omega$  (typ.)
- \* Low crosstalk : -50dB (typ.)
- \* between switches @  $f_{IS}=0.9\text{MHz}$ ,  $R_L=1\text{k}\Omega$
- \* Frequency response, switch "ON" : 40MHz (typ.)



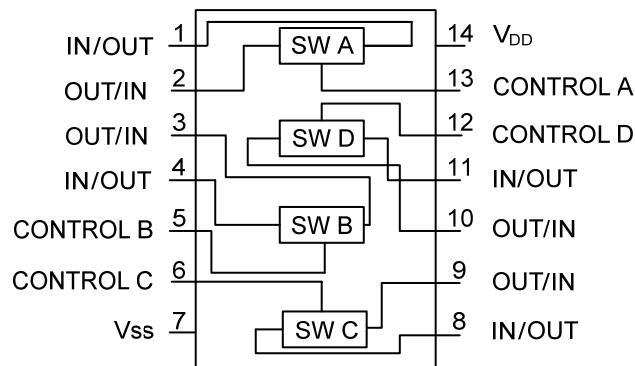
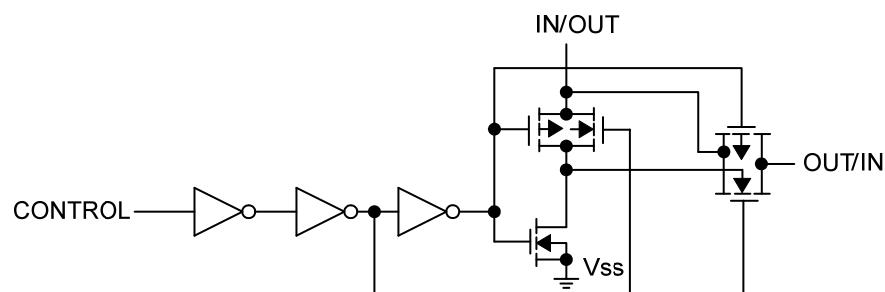
## ■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
4066L-D14-T	4066G-D14-T	DIP-14	Tube
-	4066G-S14-R	SOP-14	Tape Reel
-	4066G-P14-R	TSSOP-14	Tape Reel



## ■ MARKING

DIP-14	SOP-14 / TSSOP-14
<p>Pinout diagram for DIP-14 package. Pins are numbered 1 through 14. Internal markings include "UTC" at the top, followed by four small squares, "4066" in the center, and two small squares at the bottom. Arrows point to specific markings with labels:         <ul style="list-style-type: none"> <li>Date Code</li> <li>L: Lead Free</li> <li>G: Halogen Free</li> <li>Lot Code</li> </ul> </p>	<p>Pinout diagram for SOP-14 / TSSOP-14 package. Pins are numbered 1 through 14. Internal markings include "UTC" at the top, followed by four small squares, "4066G" in the center, and two small squares at the bottom. Arrows point to specific markings with labels:         <ul style="list-style-type: none"> <li>Date Code</li> <li>Lot Code</li> </ul> </p>

**■ PIN CONFIGURATION****■ SCHEMATIC DIAGRAM**

■ ABSOLUTE MAXIMUM RATINGS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		$V_{DD}$	-0.5 ~ +18	V
Input Voltage		$V_{IN}$	-0.5 ~ $V_{CC}+0.5$	V
Power Dissipation	DIP-14	$P_D$	700	mW
	SOP-14/TSSOP-14		500	
Junction Temperature		$T_J$	+125	°C
Storage Temperature		$T_{STG}$	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		$V_{DD}$	3 ~ 15	V
Input Voltage		$V_{IN}$	0 ~ $V_{DD}$	V
Operating Temperature Range		$T_{OPR}$	-40 ~ +85	°C

■ DC ELECTRICAL CHARACTERISTICS ( $V_{SS}=0V$ , unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
Quiescent Device Current	$I_{DD}$	$V_{DD}=5V$		0.01	1.0	μA	
		$V_{DD}=10V$		0.01	2.0		
		$V_{DD}=15V$		0.01	4.0		
SIGNAL INPUTS AND OUTPUTS							
Input or Output Leakage Switch "OFF"	$I_{IS}$	$V_C=0$		±0.1	±50	nA	
"ON" Resistance	$R_{ON}$	$R_L=10k\Omega \sim (V_{DD}-V_{SS}/2)$ $V_C=V_{DD}, V_{SS} \sim V_{DD}$	$V_{DD}=5V$	270	1050	Ω	
			$V_{DD}=10V$	120	400		
			$V_{DD}=15V$	80	240		
$\Delta$ "ON" Resistance Between Any 2 of 4 Switches	$\Delta R_{ON}$	$R_L=10k\Omega \sim (V_{DD}-V_{SS}/2)$ $V_C=V_{DD}, V_{IS}=V_{SS} \sim V_{DD}$	$V_{DD}=10V$	10		Ω	
			$V_{DD}=15V$	5			
CONTROL INPUTS							
Low Level Input Voltage	$V_{ILC}$	$V_{IS}=V_{SS}$ and $V_{DD}$ $V_{OS}=V_{DD}$ and $V_{SS}$ $I_{IS}=\pm 10\mu A$	$V_{DD}=5V$		2.25	1.5	V
			$V_{DD}=10V$		4.5	3.0	
			$V_{DD}=15V$		6.75	4.0	
HIGH Level Input Voltage	$V_{IHC}$	$V_{DD}=5V$		3.5	2.75		V
		$V_{DD}=10V$ (Note)		7.0	5.5		
		$V_{DD}=15V$		11.0	8.25		
Input Current	$I_{IN}$	$V_{DD}-V_{SS}=15V, V_{DD} \geq V_{IS} \geq V_{SS},$ $V_{DD} \geq V_C \geq V_{SS}$		$\pm 10^{-5}$	±0.3	μA	

Note: Conditions for  $V_{IHC}$ : (a)  $V_{IS}=V_{DD}$ ,  $I_{OS}$ =standard B series  $I_{OH}$ . (b)  $V_{IS}=0V$ ,  $I_{OL}$ =standard B series  $I_{OL}$

## ■ AC ELECTRICAL CHARACTERISTICS (AC Parameters are guaranteed by DC correlated testing)

(T<sub>A</sub>=25°C, t<sub>R</sub>=t<sub>F</sub>=20 ns and V<sub>SS</sub>=0V unless otherwise)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time Signal Input to Signal Output	T <sub>PHL</sub> , T <sub>PLH</sub>	V <sub>C</sub> =V <sub>DD</sub> , C <sub>L</sub> =50pF (Figure1) R <sub>L</sub> =200k	V <sub>DD</sub> =5V	25	55	ns
			V <sub>DD</sub> =10V	15	35	
			V <sub>DD</sub> =15V	10	25	
Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	t <sub>PZH</sub> , t <sub>PLZ</sub>	R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =50pF (Fig. 2, 3)	V <sub>DD</sub> =5V		125	ns
			V <sub>DD</sub> =10V		60	
			V <sub>DD</sub> =15V		50	
Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	t <sub>PHZ</sub> , t <sub>PLZ</sub>	R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =50pF (Fig. 2, 3)	V <sub>DD</sub> =5V		125	ns
			V <sub>DD</sub> =10V		60	
			V <sub>DD</sub> =15V		50	
Sine Wave Distortion		V <sub>C</sub> =V <sub>DD</sub> =5V, V <sub>SS</sub> = -5V R <sub>L</sub> =10kΩ, V <sub>IS</sub> =5V <sub>p-p</sub> , f=1kHz, (Fig. 4)		0.1		%
Frequency Response -Switch "ON" (Frequency at-3dB)		V <sub>C</sub> =V <sub>DD</sub> =5V, V <sub>SS</sub> = -5V R <sub>L</sub> =1kΩ, V <sub>IS</sub> =5V <sub>p-p</sub> 20 Log <sub>10</sub> V <sub>OS</sub> /V <sub>OS</sub> (1kHz)-dB (Fig. 4)		40		MHz
Feedthrough - Switch "OFF" (Frequency at -50 dB)		V <sub>DD</sub> =5.0V, V <sub>CC</sub> =V <sub>SS</sub> = -5.0V, R <sub>L</sub> =1kΩ, V <sub>IS</sub> =5.0V <sub>p-p</sub> , 20Log <sub>10</sub> , V <sub>OS</sub> /V <sub>IS</sub> = -50dB, (Fig. 4)		1.25		MHz
Crosstalk Between Any Two Switches(Frequency at-50dB)		V <sub>DD</sub> =V <sub>C</sub> (A)=5.0V; V <sub>SS</sub> =V <sub>C</sub> (B)=5.0V, R <sub>L</sub> =1kΩ, V <sub>IS</sub> (A)=5.0V <sub>p-p</sub> , 20Log <sub>10</sub> , V <sub>OS</sub> (B)/V <sub>IS</sub> (A)= -50dB (Fig. 5)		0.9		MHz
Crosstalk; Control Input to Signal Output		V <sub>DD</sub> =10V, R <sub>L</sub> =10kΩ, R <sub>IN</sub> =1.0kΩ, V <sub>CC</sub> =10V Square Wave, C <sub>L</sub> =50pF (Fig. 6)		150		mV <sub>p-p</sub>
Maximum Control Input		R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =50pF (Fig. 7) V <sub>OS</sub> (f) =1/2V <sub>OS</sub> (1.0kHz)	V <sub>DD</sub> =5.0V	6.0		MHz
			V <sub>DD</sub> =10V	8.0		
			V <sub>DD</sub> =15V	8.5		
Signal Input Capacitance	C <sub>IS</sub>			8.0		pF
Signal Output Capacitance	C <sub>OS</sub>	V <sub>DD</sub> =10V		8.0		pF
Feedthrough Capacitance	C <sub>IOS</sub>	V <sub>C</sub> =0V		0.5		pF
Control Input Capacitance	C <sub>IN</sub>			5.0	7.5	pF

## ■ SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive  $V_{DD}$  and the signal input, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$ =effective external load of the UTC 4066 bilateral switches). This provision avoids any permanent current flow or clamp action of the  $V_{DD}$  supply when power is applied or removed from UTC 4066.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and Signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into terminals 1,4,8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at  $T_A \leq 25^\circ\text{C}$ , or 0.4V at  $T_A > 25^\circ\text{C}$  (calculated from  $R_{ON}$  values shown).

NO  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9 or 10.

## ■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS

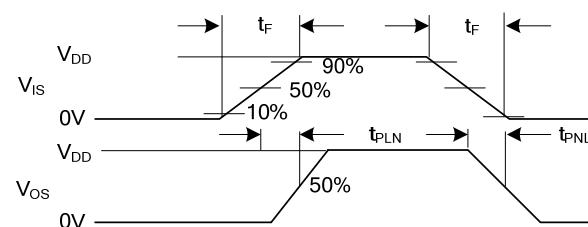
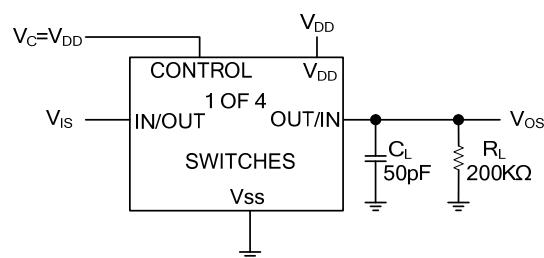


Fig. 1  $t_{PHL}, t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

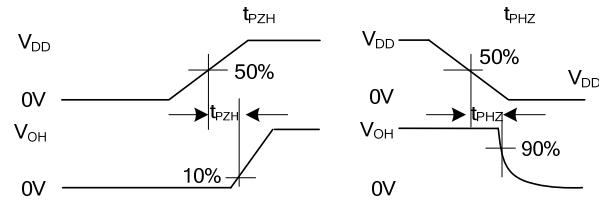
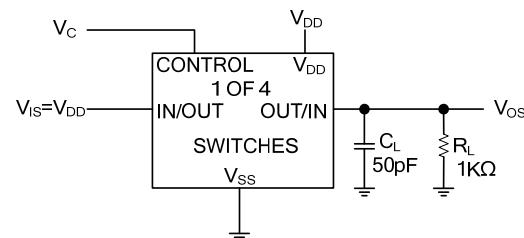


Fig. 2  $t_{PZH}, t_{PHZ}$  Propagation Delay Time Control to Signal Output

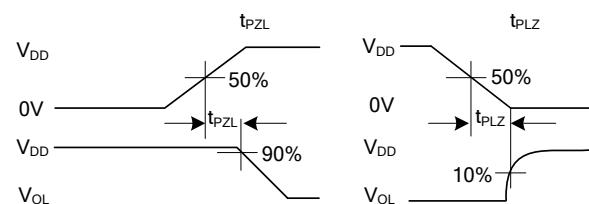
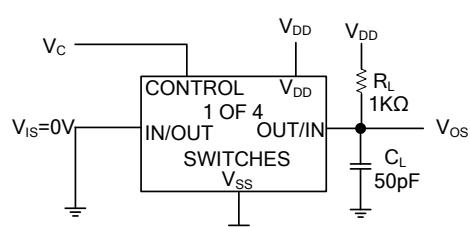
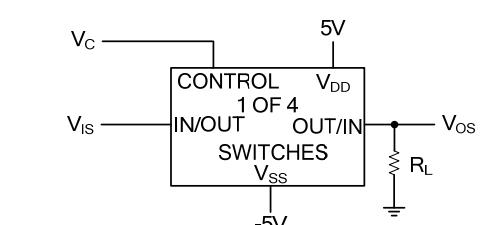


Fig. 3  $t_{PZL}, t_{PLZ}$  Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$  for distortion and frequency response tests  
 $V_C = V_{SS}$  for feedthrough test

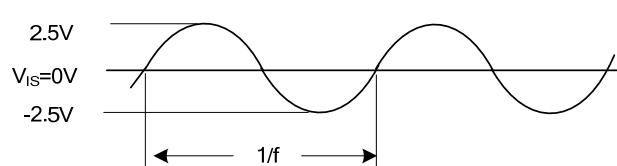


Fig. 4 Sine Wave Distortion, Frequency Response and Feedthrough

■ AC TEST CIRCUITS AND SWITCHING TIME WAVEFORMS(Cont.)

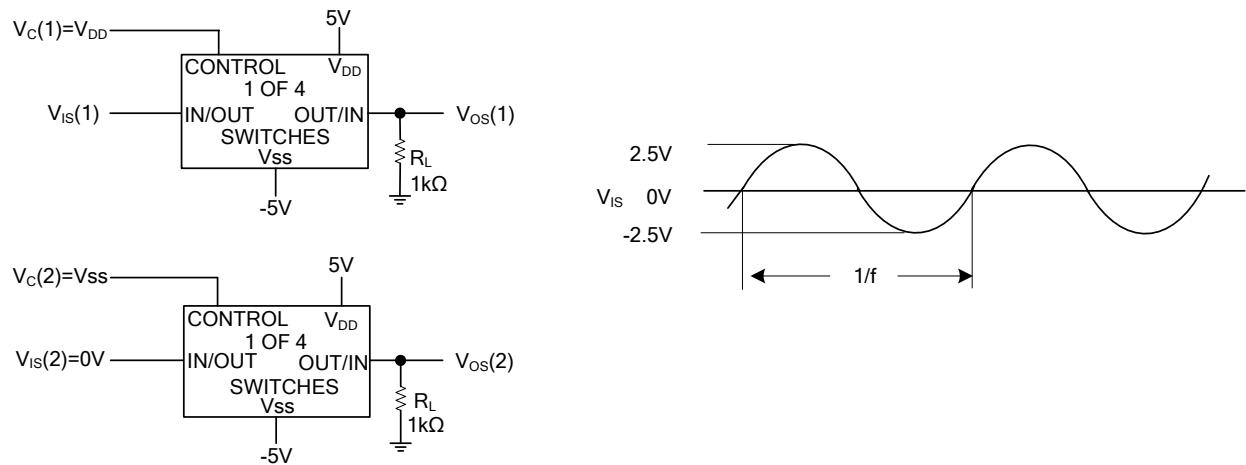


Fig. 5 Crosstalk Between Any Two Switches

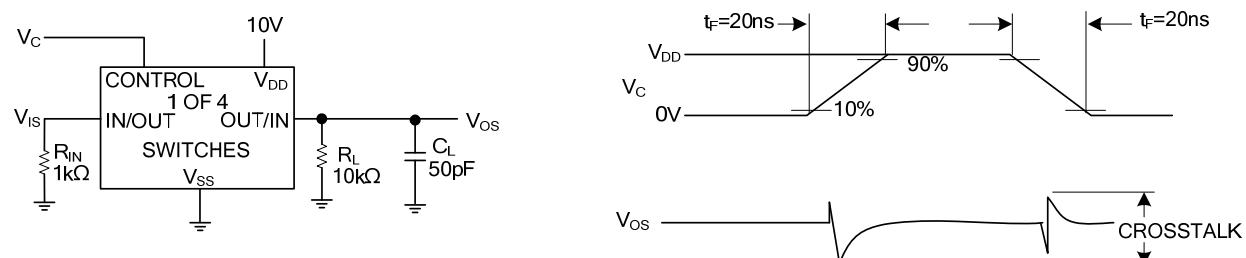


Fig.6 Crosstalk: Control Input to Signal Output

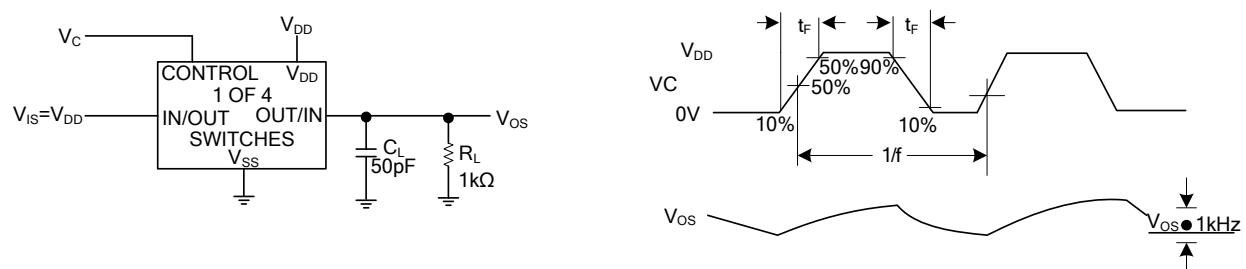
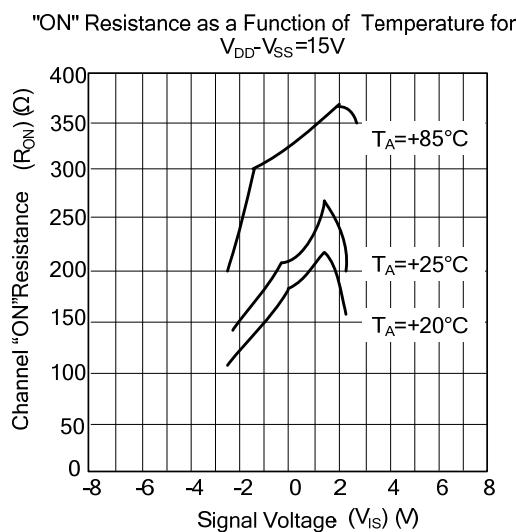
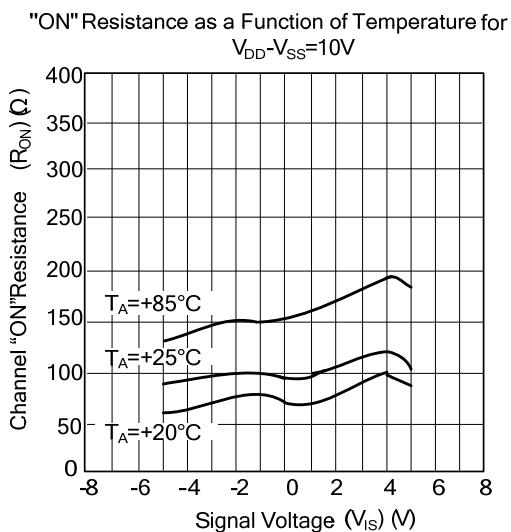
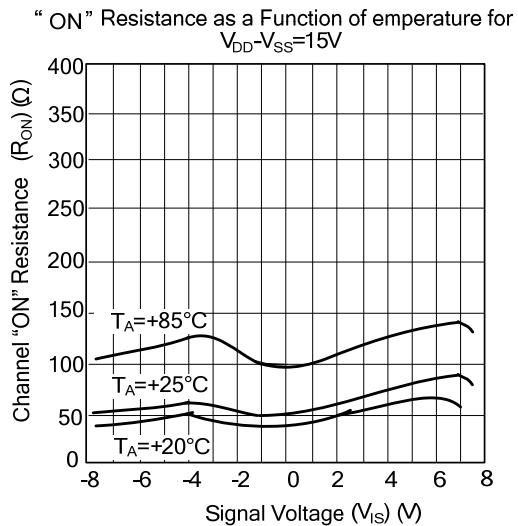
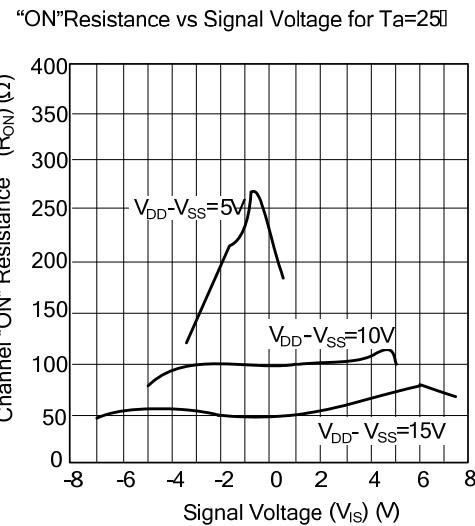


Fig. 7 Maximum Control Input Frequency

■ TYPICAL PERFORMANCE CHARACTERISTICS



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