Ordering number : ENA2331

LV5762QA

Bi-CMOS IC

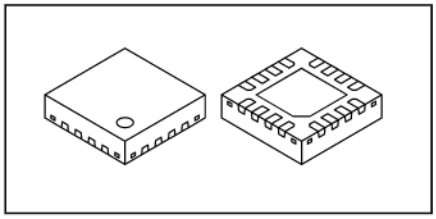
Step-down Switching Regulator

ON Semiconductor®

http://onsemi.com

Overview

LV5762QA is a 1ch step-down voltage switching regulator.



VQFN16J (3.0 × 3.0)

Function

- 1ch step-down switching regulator controller
- Load-independent soft start circuit
- Frequency fold back function
- ON/OFF function
- Built-in pulse-by-pulse OCP circuit.
  It is detected by using ON resistance of an external MOS.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{IN} max		45	V
Allowable power dissipation	Pd max	*)	0.65	W
Operating temperature	Topr		–40 to 85	°C
Storage temperature	Tstg		–55 to 150	°C

* Specified board: 24.0mm × 15.0mm ×1.6mm, glass epoxy board (2-layer).

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{IN}		8 to 42	V
Error amplifier input coltage	V_{FB}		0 to 1.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

Electrical Characteristics at Ta = 25°C, V_{IN} = 24V

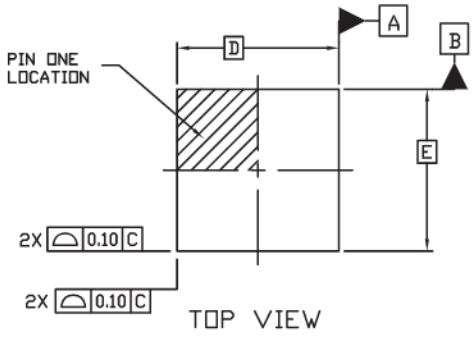
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A	0.695	0.705	0.715	V
5V power supply	V_{DD}	I_{OUT}=0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	f_{OSC}		870	1000	1130	kHz
Frequency variation	f_{OSC}_DV	V_{IN}=8 to 42V		1		%
Oscillatory frequency fold back detection voltage	V_{OSC}_FB	Detect IN voltage after the end of SS		0.5		V
Oscillatory frequency after fold back	f_{OSC}_FB		100	150	200	kHz
ON/OFF circuit block						
IC start-up voltage	V_{EN}_on	V_{IN}=8 to 42V		3.4	4.3	V
IC off voltage	V_{EN}_off	V_{IN}=8 to 42V	1.1	1.3		V
Soft start circuit block						
Soft start source current	I_{SS}_SC	EN > 5V, SS=0V	3.4	4.3	5.2	µA
Soft start sink current	I_{SS}_SK	EN < 1V, V_{DD}=5V, SS=1V		2		mA
Voltage to end the soft start function	V_{SS}_END		0.7	0.9	1.1	V
UVLO circuit block						
UVLO lock release voltage	V_{UVLO}		7.0	7.4	7.8	V
UVLO hysteresis	V_{UVLO}_H			0.6		V
Error amplifier						
Input bias current	I_{EA}_IN				100	nA
Error amplifier transconductance	GEA		1000	1400	1800	µA/V
Common mode input voltage range	V_{EA}_R	V_{IN}=8 to 42V	0.0		1.6	V
Sink output current	I_{EA}_OSK	FB=1.0V		–100		µA
Source output current	I_{EA}_OSC	FB=0V		100		µA
Current detection amplifier gain	GISNS			1.3		
Over current limiter circuit block						
Reference current	I_{LIM}		–10%	20	+10%	µA
Over current detection comparator offset voltage	V_{LIM}_OFS		–5		+5	mV
Over current detection comparator common mode input range			V_{IN}_0.45		V_{IN}	V
PWM comparator						
Input threshold voltage	Vtmax	Duty cycle=DMAX	0.95	1.1	1.25	V
	Vt0	Duty cycle=0%	0.35	0.45	0.55	V
Maximum ON duty	DMAX		75	80		%
Output block						
Output stage ON resistance (the upper side)	R_{ON}H			5		Ω
Output stage ON resistance (the under side)	R_{ON}L			5		Ω
Output stage ON current (the upper side)	I_{ON}H		240			mA
Output stage ON current (the under side)	I_{ON}L		240			mA
The whole device						
Standby current	I_{CC}S	EN < 1V			60	µA
Mean consumption current	I_{CC}A	EN > 5V		3.6		mA

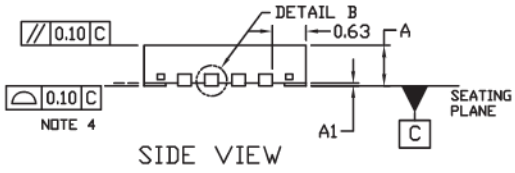
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Package Dimensions

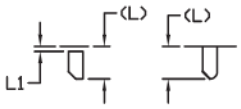
unit : mm

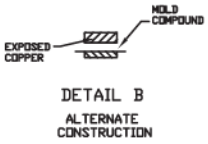
WQFN16 3x3, 0.5P / VQFN16J
CASE 510AX
ISSUE A



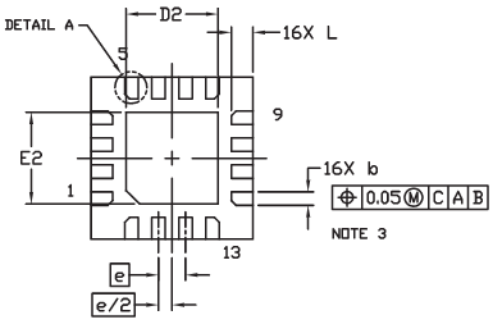


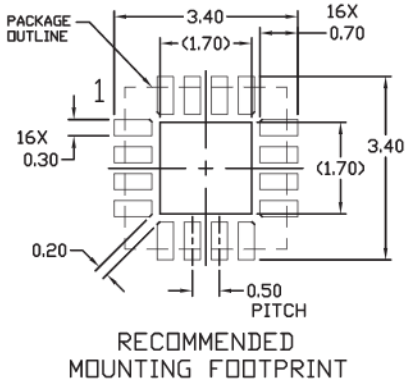
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.





DIM	MILLIMETERS	
	MIN.	MAX.
A	---	0.80
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	1.70 REF	
E	3.00 BSC	
E2	1.70 REF	
e	0.50 BSC	
L	0.30	0.50
L1	0.00	0.15



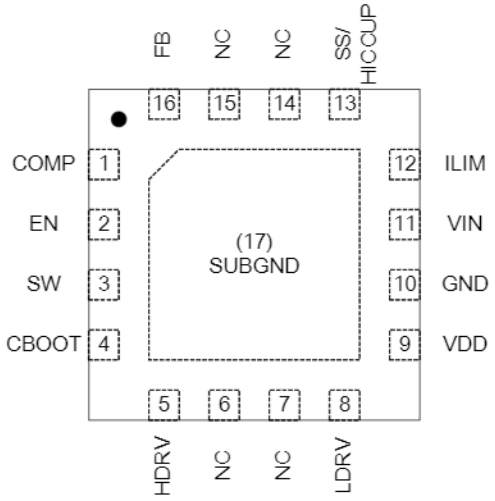


GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

Pin Assignment

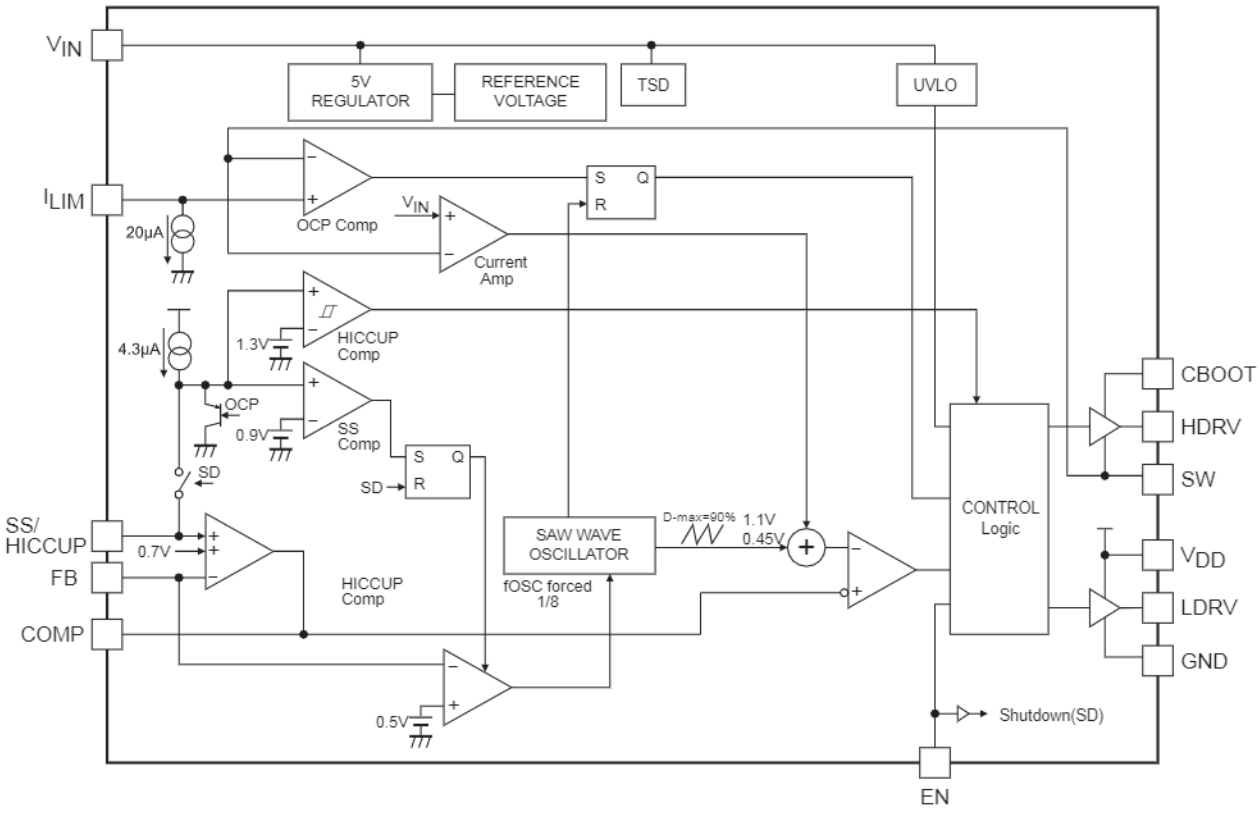


(TOP VIEW)

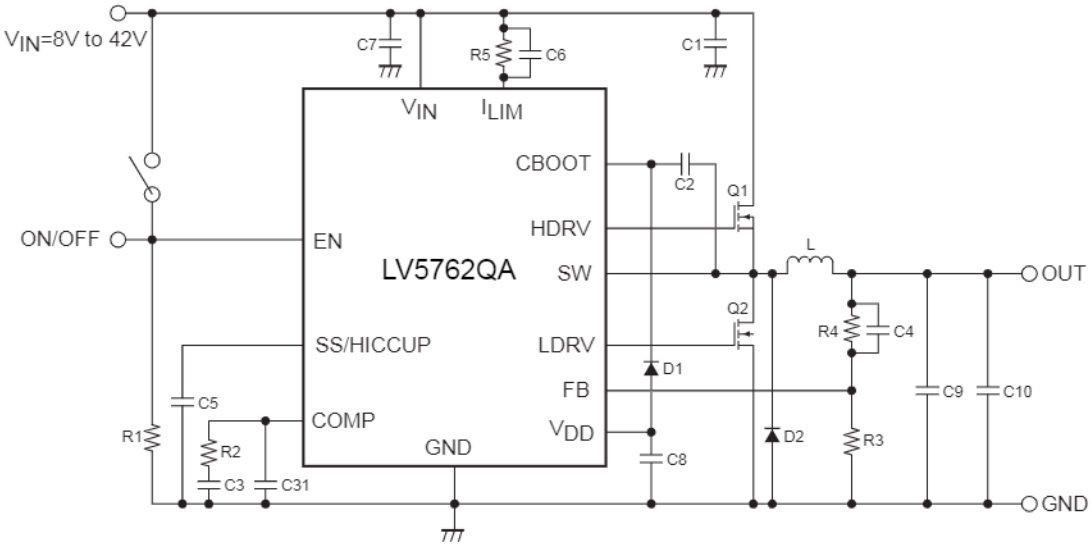
Pin Function

Pin No.	Pin name	Function
1	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
2	EN	ON/OFF pin.
3	SW	Pin to connect with switching node. The source of Nch MOSFET connects to this pin.
4	CBOOT	Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external Nch MOSFET. Connect a bypath capacitor between CBOOT and SW.
5	HDRV	An external the upper MOSFET gate drive pin.
6 7 14 15	NC	No connection
8	LDRV	An external the lower MOSFET gate drive pin.
9	V_{DD}	Power supply pin for an external the MOS-FET gate drive.
10	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
11	V_{IN}	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.8V or more by UVLO function, The IC starts and the soft start function operates.
12	I_{LIM}	Reference current pin for current detection. The sink current of about 20μA flows to this pin. When a resistance is connected between this pin and V_{IN} outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper Nch MOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWN pulse.
13	SS/HICCUP	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 4.3μA. This pin ends the soft start period by using the voltage of about 0.9V and the frequency fold back function becomes active.
16	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.7V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Also, the oscillation frequency become one-eighth when the voltage of this pin becomes 0.4V or less after soft start function.
17	SUBGND	Connect to GND

Block Diagram



Sample Application Circuit



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5762QA-NH	VQFN16J (Pb-Free / Halogen Free)	2000 / Tape & Reel