SDRAM

2M x 32 SDRAM

512K x 32bit x 4Banks Synchronous DRAM

FEATURES

- 3.3V power supply
- Clock cycle time : 5 / 5.5 / 6 / 7 / 8 / 10 ns
- Internal four banks operation
- LVTTL compatible with multiplexed address
- All inputs are sampled at the positive going edge of system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto refresh and self refresh
- 64ms refresh period (4K cycle)
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length :
    1 , 2 , 4 , 8 or full page for Sequential Burst
    1 , 2 , 4 or 8 for Interleave Burst
- Available package type :
  - 86 pin 400mil TSOP(II) and Lead free
- Operating temperature :
  - 0 ~ +70 °C

GRNERAL DESCRIPTION

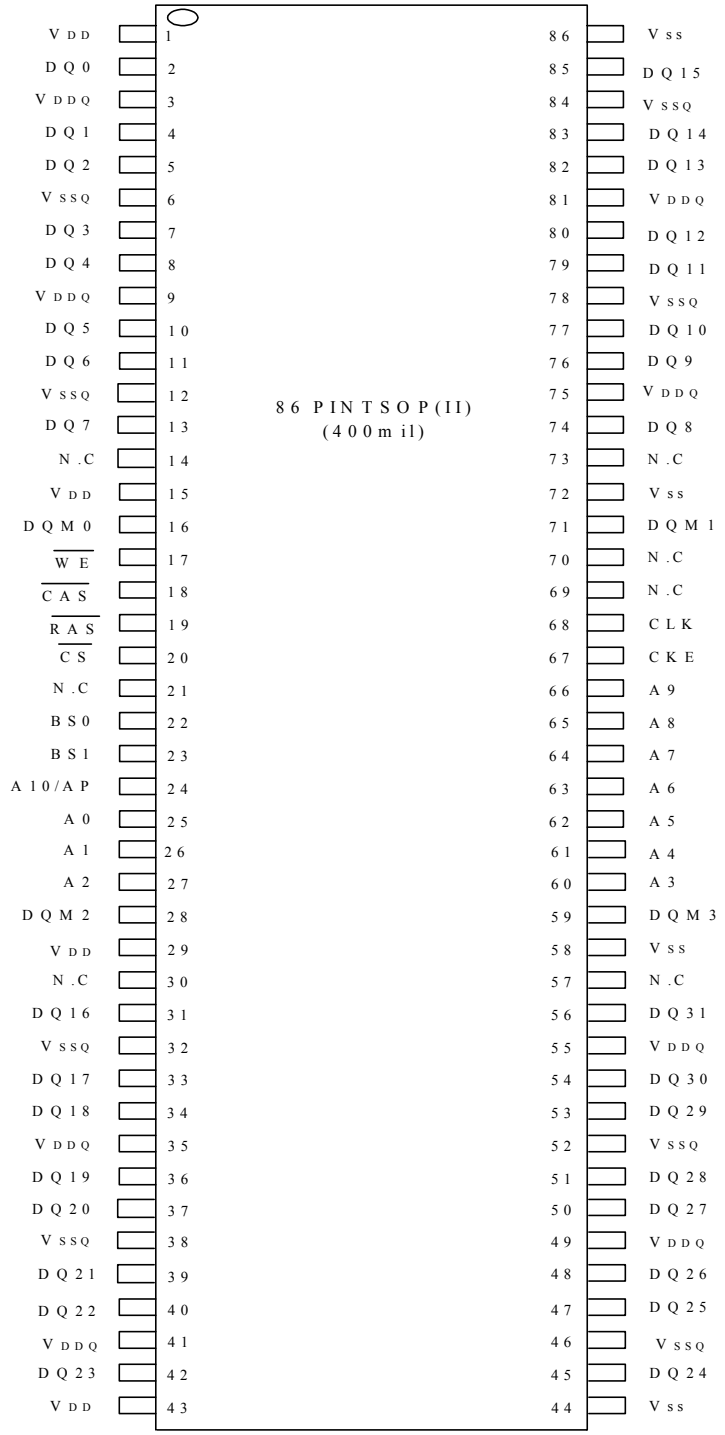
The T436432B is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits , fabricated with high performance CMOS technology . Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle . Range of operating frequencies , programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth , high performance memory system applications.

PART NUMBER EXAMPLES

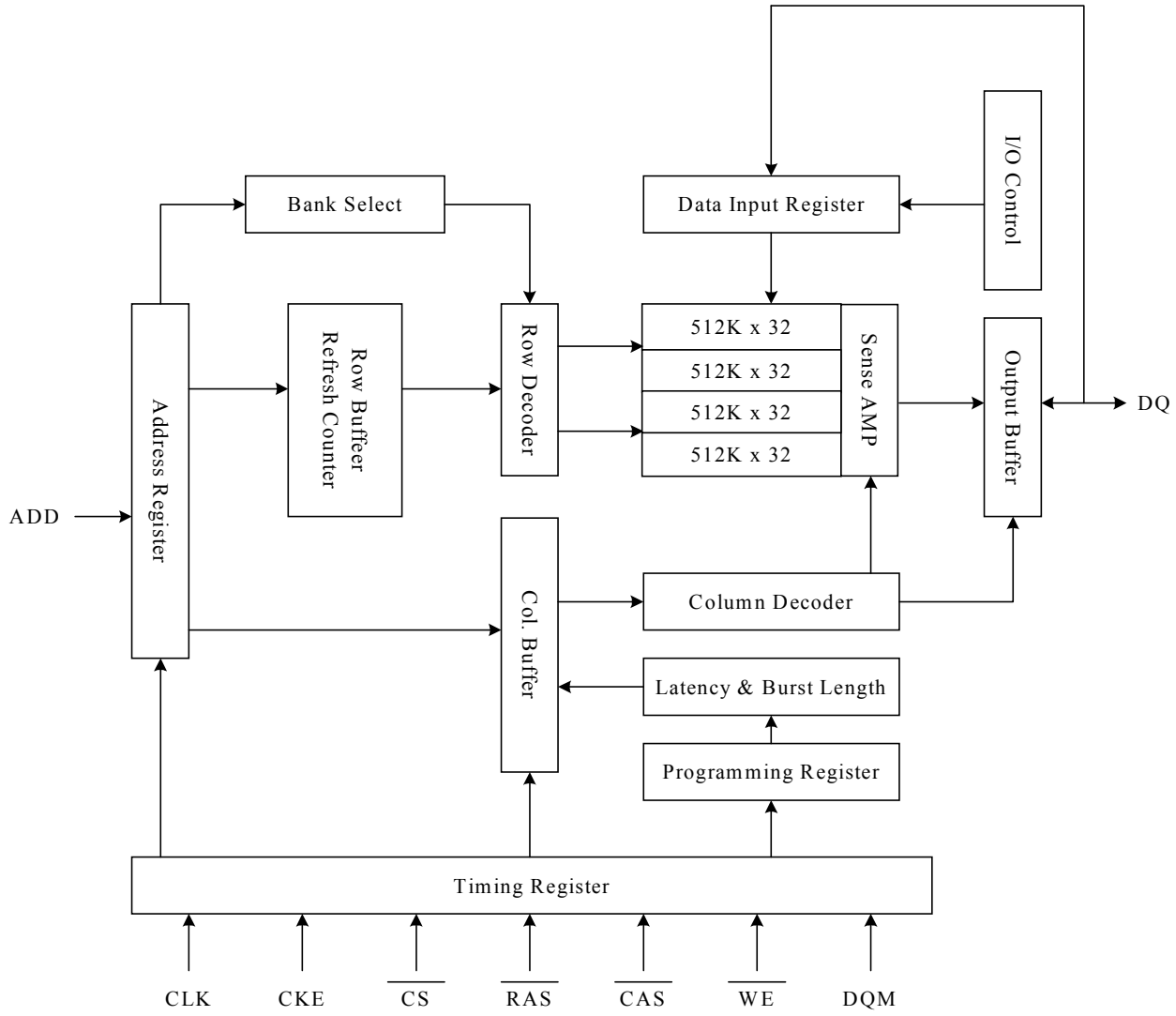
PART NO.	CLOCK CYCLE TIME	MAX FREQUENCY	PACKAGE	OPERATING TEMPERATURE
T436432B-5SG	5ns	200 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-5S	5ns	200 MHz	TSOP-II	0 ~ +70 °C
T436432B-55SG	5.5ns	183 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-55S	5.5ns	183 MHz	TSOP-II	0 ~ +70 °C
T436432B-6SG	6ns	166 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-6S	6ns	166 MHz	TSOP-II	0 ~ +70 °C
T436432B-7SG	7ns	143 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-7S	7ns	143 MHz	TSOP-II	0 ~ +70 °C
T436432B-8SG	8ns	125 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-8S	8ns	125 MHz	TSOP-II	0 ~ +70 °C
T436432B-10SG	10ns	100 MHz	TSOP-II Lead free	0 ~ +70 °C
T436432B-10S	10ns	100 MHz	TSOP-II	0 ~ +70 °C

PIN ARRANGEMENT

(TSOP-II Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all input.
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all input except CLK,CKE and DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10,column address : CA0 ~ CA7 Auot-precharge flag : A10/AP
BS0~1	Bank Select Address	Selects bank to be activated during row address latch time. Select bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access .
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0~3	Data Input/Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ DQ31	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C	No Connection	No Connection.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DQM(6)	BS0,1	A10	A9-0	CS#	RAS#	CAS#	WE#
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	H	X	X	X
	(SelfRefresh)							L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any	L	H	X	X	X	X	H	X	X	X
	(PowerDown)							L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

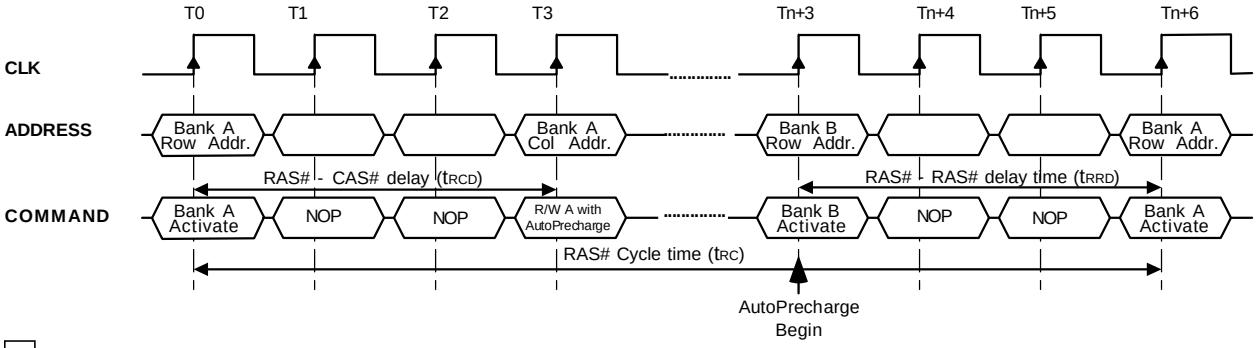
Note: 1. V = Valid, X = Don't care, L = Logic low, H = Logic high
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.
6. DQM0-3

Commands

1 BankActivate

(RAS# = "L", CAS# = "H", WE# = "H", BS = Bank, A0-A10 = Row Address)

The BankActivate command activates the idle bank designated by the BS0,1 (Bank Select) signal. By latching the row address on A0 to A10 at the time of this command, the selected row access is initiated. The read or write operation in the same bank can occur after a time delay of t_{RCD}(min.) from the time of bank activation. A subsequent BankActivate command to a different row in the same bank can only be issued after the previous active row has been precharged (refer to the following figure). The minimum time interval between successive BankActivate commands to the same bank is defined by t_{RC}(min.). The SDRAM has four internal banks on the same chip and shares part of the internal circuitry to reduce chip area; therefore it restricts the back-to-back activation of the four banks. t_{RRD}(min.) specifies the minimum time required between activating different banks. After this command is used, the Write command and the Block Write command perform the no mask write operation.



: "H" or "L"

BankActivate Command Cycle (Burst Length = n, CAS# Latency = 3)

2 BankPrecharge command

(RAS# = "L", CAS# = "H", WE# = "L", BS = Bank, A10 = "L", A0-A9 = Don't care)

The BankPrecharge command precharges the bank disignated by BS0,1 signal. The precharged bank is switched from the active state to the idle state. This command can be asserted anytime after t_{RAS}(min.) is satisfied from the BankActivate command in the desired bank. The maximum time any bank can be active is specified by t_{RAS}(max.). Therefore, the precharge function must be performed in any active bank within t_{RAS}(max.). At the end of precharge, the precharged bank is still in the idle state and is ready to be activated again.

3 PrechargeAll command

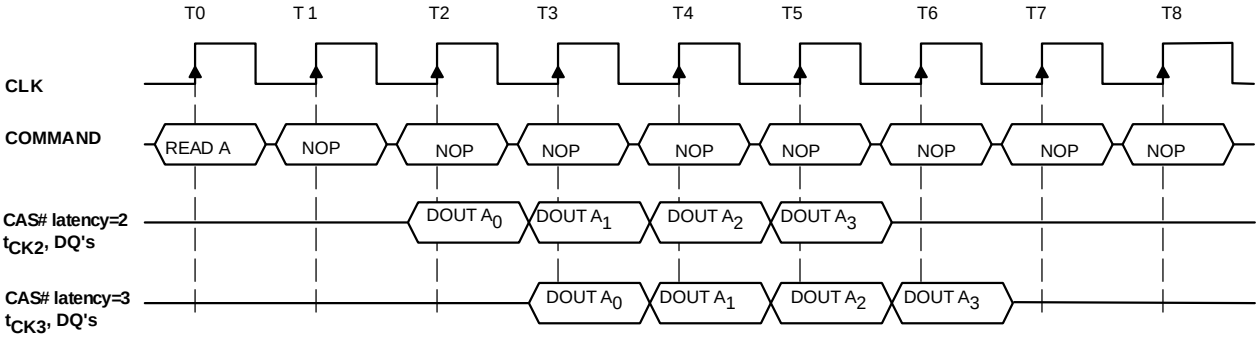
(RAS# = "L", CAS# = "H", WE# = "L", BS = Don't care, A10 = "H", A0-A9 = Don't care)

The PrechargeAll command precharges all the four banks simultaneously and can be issued even if all banks are not in the active state. All banks are then switched to the idle state.

4 Read command

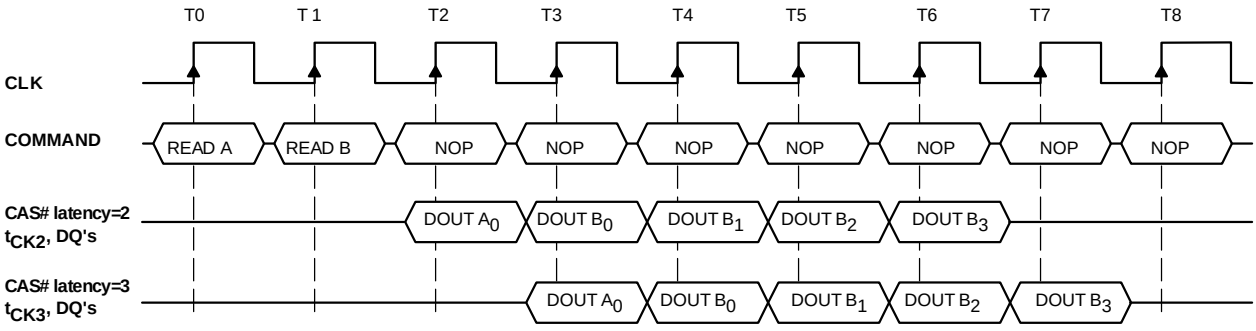
(RAS# = "H", CAS# = "L", WE# = "H", BS = Bank, A10 = "L", A0-A7 = Column Address)

The Read command is used to read a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before the Read command is issued. During read bursts, the valid data-out element from the starting column address will be available following the CAS# latency after the issue of the Read command. Each subsequent data-out element will be valid by the next positive clock edge (refer to the following figure). The DQs go into high-impedance at the end of the burst unless other command is initiated. The burst length, burst sequence, and CAS# latency are determined by the mode register which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



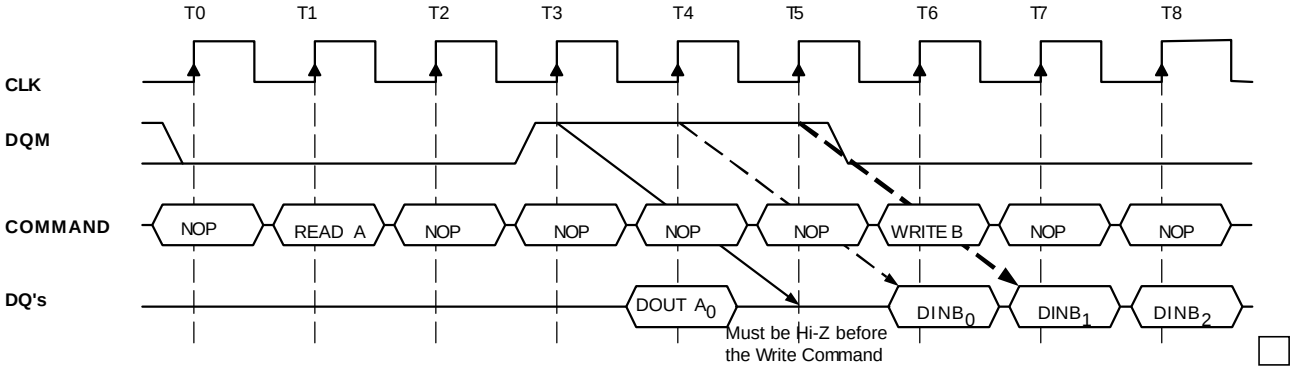
Burst Read Operation(Burst Length = 4, CAS# Latency = 2, 3)

The read data appears on the DQs subject to the values on the DQM inputs two clocks earlier (i.e. DQM latency is two clocks for output buffers). A read burst without the auto precharge function may be interrupted by a subsequent Read or Write command to the same bank or the other active bank before the end of the burst length. It may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank too. The interrupt coming from the Read command can occur on any clock cycle following a previous Read command (refer to the following figure).

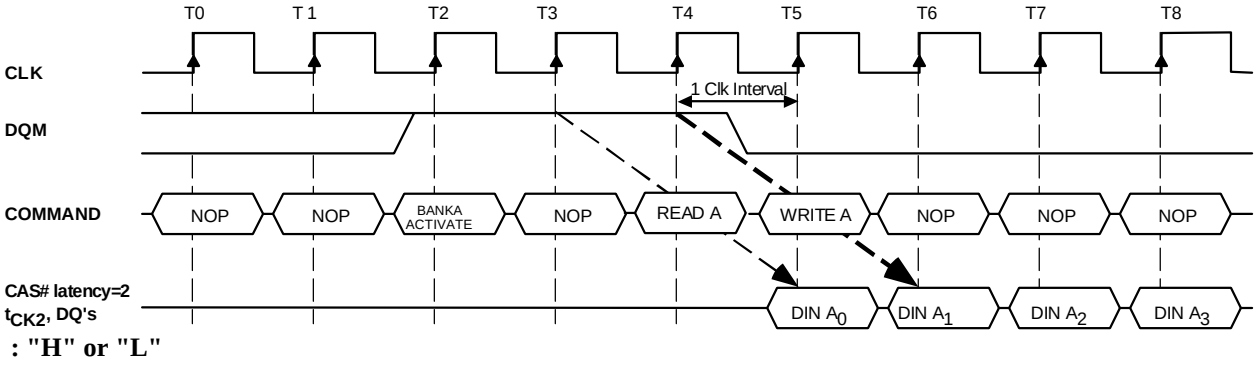


Read Interrupted by a Read (Burst Length = 4, CAS# Latency = 2, 3)

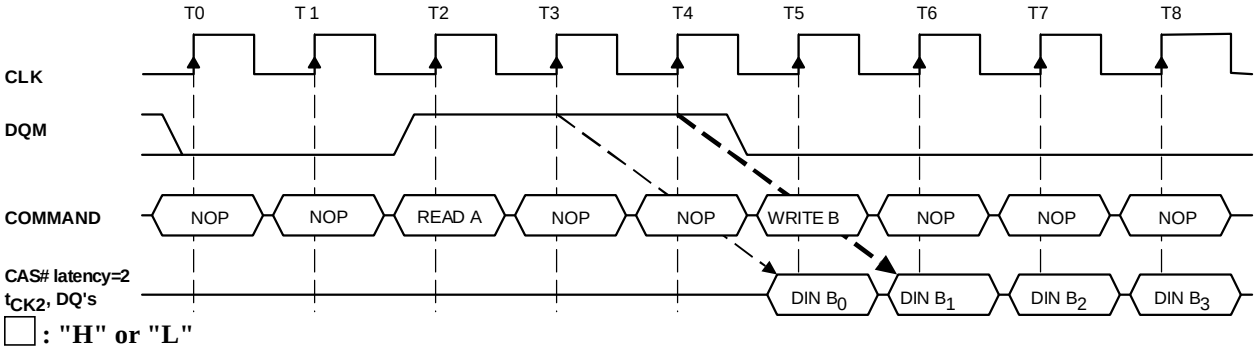
The DQM inputs are used to avoid I/O contention on the DQ pins when the interrupt comes from a Write command. The DQMs must be asserted (HIGH) at least two clocks prior to the Write command to suppress data-out on the DQ pins. To guarantee the DQ pins against I/O contention, a single cycle with high-impedance on the DQ pins must occur between the last read data and the Write command (refer to the following three figures). If the data output of the burst read occurs at the second clock of the burst write, the DQMs must be asserted (HIGH) at least one clock prior to the Write command to avoid internal bus contention.



Read to Write Interval (Burst Length • 4, CAS# Latency = 3)

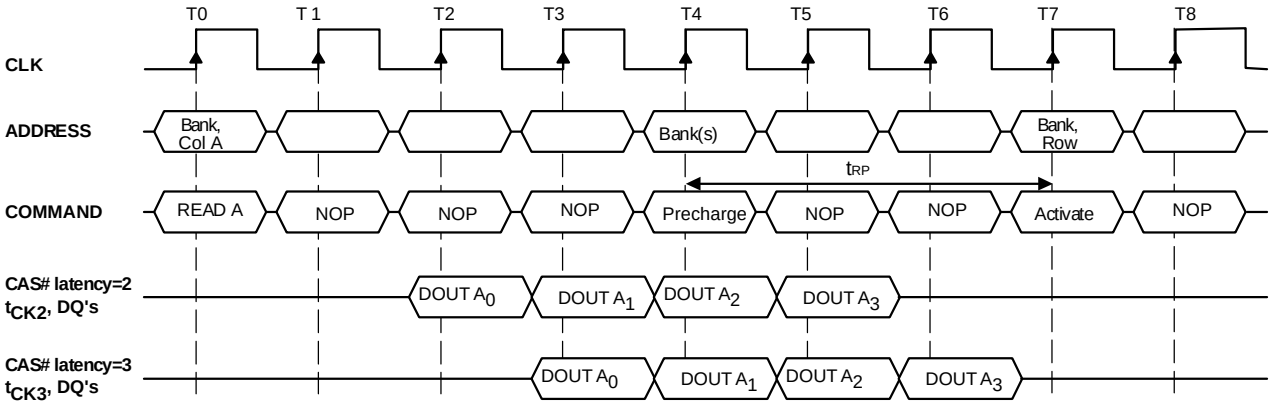


Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 2)



Read to Write Interval (Burst Length ≥ 4, CAS# Latency = 2)

A read burst without the auto precharge function may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank. The following figure shows the optimum time that BankPrecharge/ PrechargeAll command is issued in different CAS# latency.



Read to Precharge (CAS# Latency = 2, 3)

5 Read and AutoPrecharge command

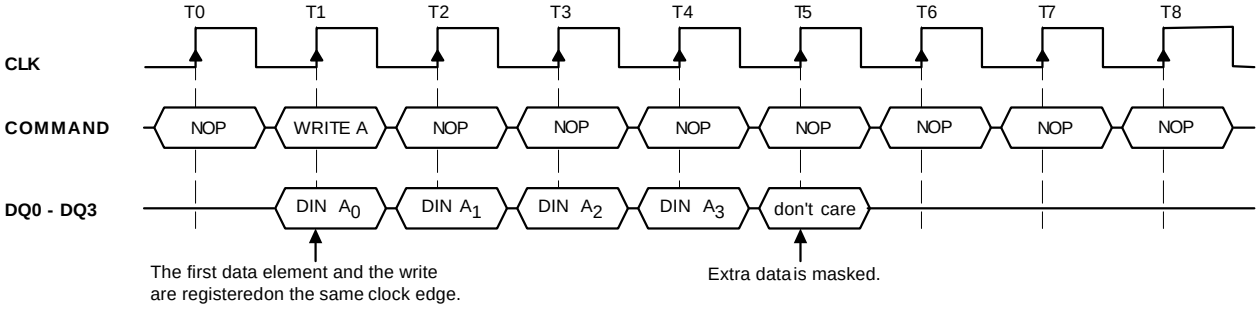
(RAS# = "H", CAS# = "L", WE# = "H", BS = Bank, A10 = "H", A0-A7 = Column Address)

The Read and AutoPrecharge command automatically performs the precharge operation after the read operation. Once this command is given, any subsequent command cannot occur within a time delay of {t_{RP}(min.) + burst length}. At full-page burst, only the read operation is performed in this command and the auto precharge function is ignored.

6 Write command

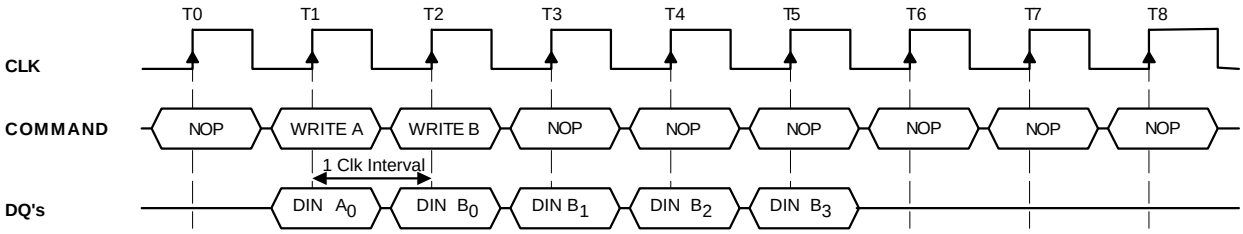
(RAS# = "H", CAS# = "L", WE# = "L", BS = Bank, A10 = "L", A0-A7 = Column Address)

The Write command is used to write a burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before the Write command is issued. During write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge (refer to the following figure). The DQs remain with high-impedance at the end of the burst unless another command is initiated. The burst length and burst sequence are determined by the mode register, which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



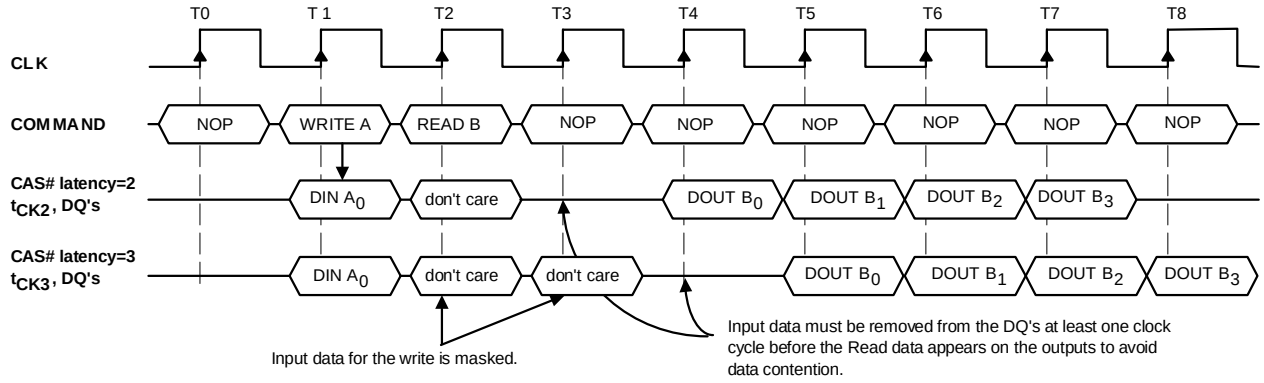
Burst Write Operation (Burst Length = 4, CAS# Latency = 1, 2, 3)

A write burst without the AutoPrecharge function may be interrupted by a subsequent Write, BankPrecharge/PrechargeAll, or Read command before the end of the burst length. An interrupt coming from Write command can occur on any clock cycle following the previous Write command (refer to the following figure).



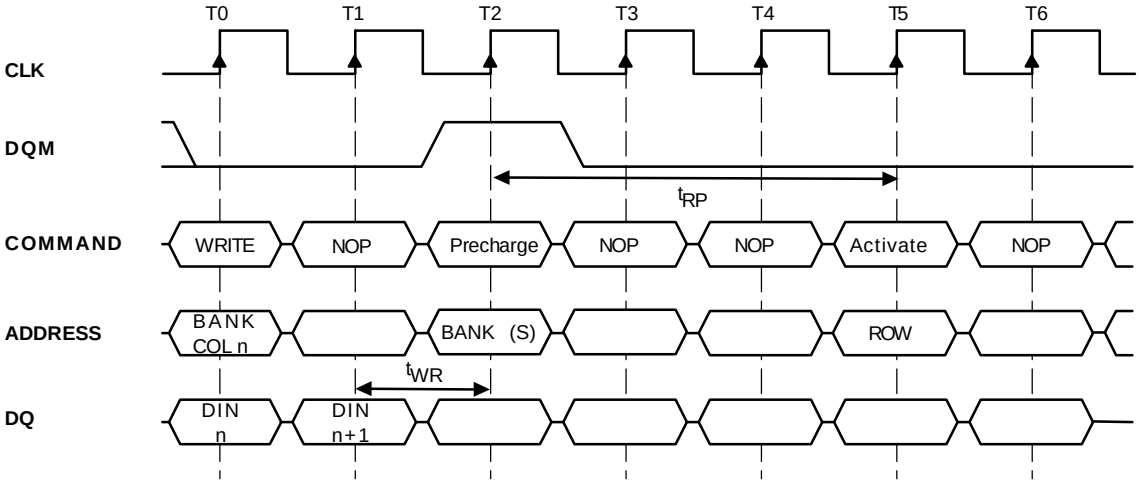
Write Interrupted by a Write (Burst Length = 4, CAS# Latency = 1, 2, 3)

The Read command that interrupts a write burst without auto precharge function should be issued one cycle after the clock edge in which the last data-in element is registered. In order to avoid data contention, input data must be removed from the DQs at least one clock cycle before the first read data appears on the outputs (refer to the following figure). Once the Read command is registered, the data inputs will be ignored and writes will not be executed.



Write Interrupted by a Read (Burst Length = 4, CAS# Latency = 2, 3)

The BankPrecharge/PrechargeAll command that interrupts a write burst without the auto precharge function should be issued *m* cycles after the clock edge in which the last data-in element is registered, where *m* equals t_{WR}/t_{CK} rounded up to the next whole number. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last data-in element and ending with the clock edge on which the BankPrecharge/PrechargeAll command is entered (refer to the following figure).



: don't care

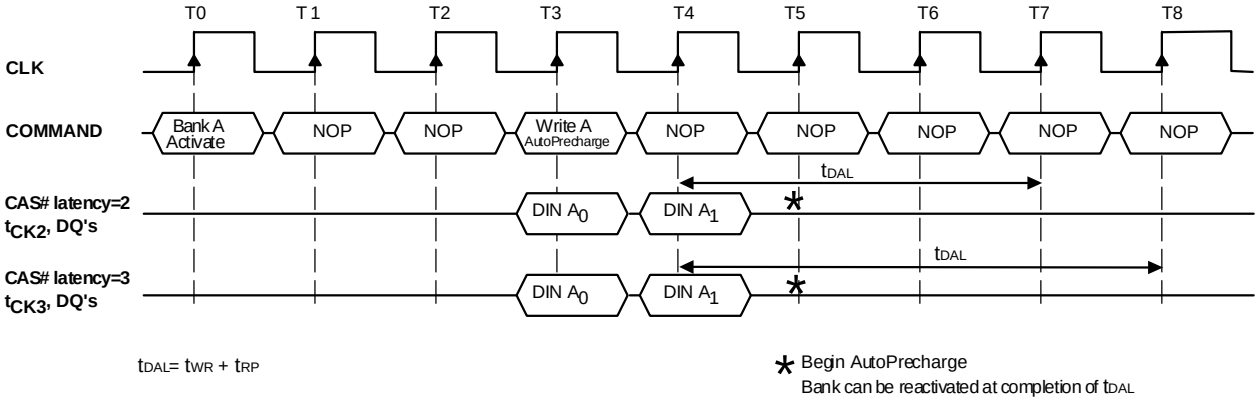
Note: The DQMs can remain low in this example if the length of the write burst is 1 or 2.

Write to Precharge

7 Write and AutoPrecharge command (refer to the following figure)

(RAS# = "H", CAS# = "L", WE# = "L", BS = Bank, A10 = "H", A0-A7 = Column Address)

The Write and AutoPrecharge command performs the precharge operation automatically after the write operation. Once this command is given, any subsequent command can not occur within a time delay of {(burst length -1) + t_{WR} + t_{RP}(min.)}. At full-page burst, only the write operation is performed in this command and the auto precharge function is ignored.

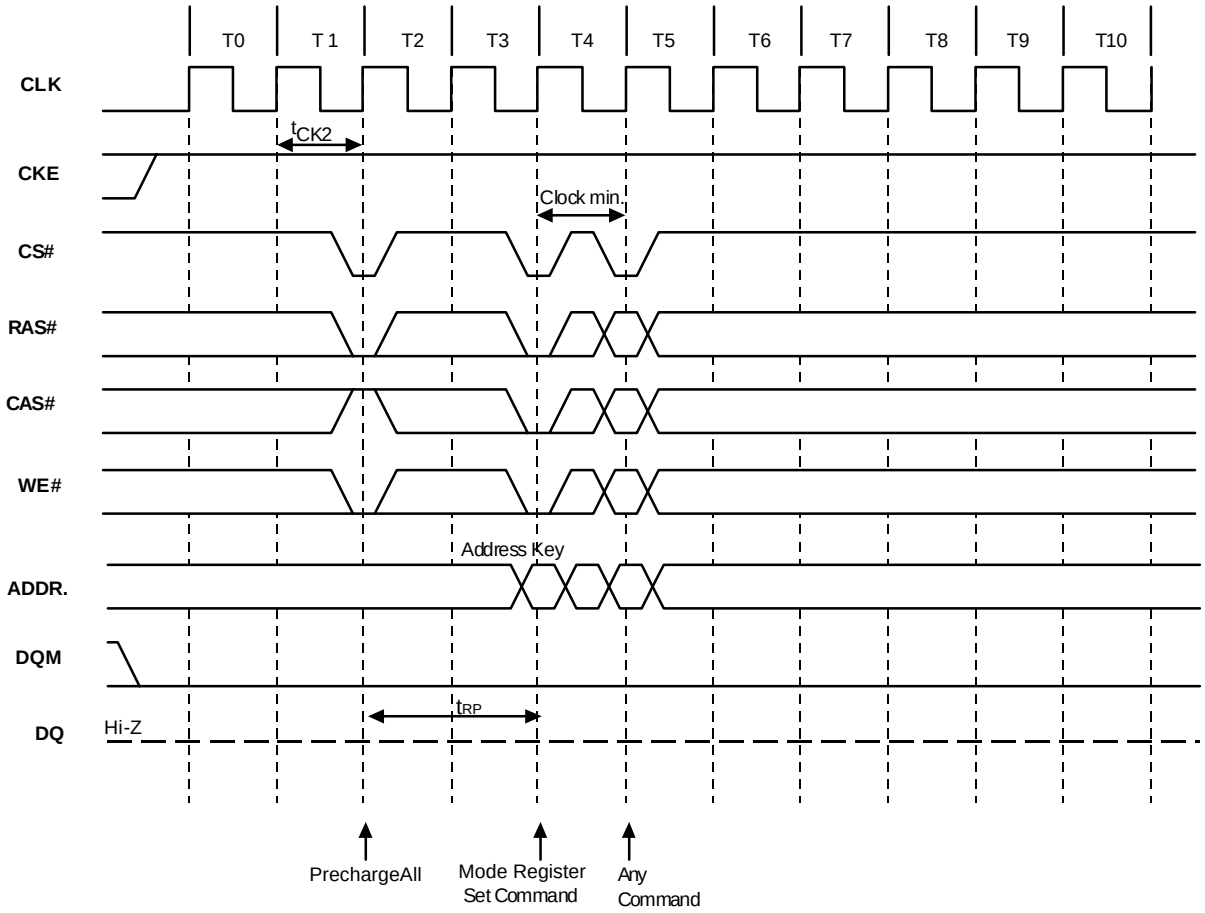


Burst Write with Auto-Precharge (Burst Length = 2, CAS# Latency = 2, 3)

8 Mode Register Set command

(RAS# = "L", CAS# = "L", WE# = "L", BS0,1 and A10-A0 = Register Data)

The mode register stores the data for controlling the various operating modes of SDRAM. The Mode Register Set command programs the values of CAS# latency, Addressing Mode and Burst Length in the Mode register to make SDRAM useful for a variety of different applications. The default values of the Mode Register after power-up are undefined; therefore this command must be issued at the power-up sequence. The state of pins BS0,1 and A10~A0 in the same cycle is the data written to the mode register. One clock cycle is required to complete the write in the mode register (refer to the following figure). The contents of the mode register can be changed using the same command and the clock cycle requirements during operation as long as all banks are in the idle state.



Mode Register Set Cycle (CAS# Latency = 2, 3)

The mode register is divided into various fields depending on functionality.

Address	BS0,1	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU*	RFU*	WBL	Test Mode		CAS Latency			BT	Burst Length		

*Note: RFU (Reserved for future use) should stay "0" during MRS cycle.

- Burst Length Field (A2~A0)

This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8, or full page.

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

- Burst Type Field (A3)

The Burst Type can be one of two modes, Interleave Mode or Sequential Mode.

A3	Burst Type
0	Sequential
1	Interleave

--- Addressing Sequence of Sequential Mode

An internal column address is performed by increasing the address from the column address which is input to the device. The internal column address is varied by the Burst Length as shown in the following table. When the value of column address, (n + m), in the table is larger than 255, only the least significant 8 bits are effective.

Data n	0	1	2	3	4	5	6	7	-	255	256	257	-
Column Address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	-	N+255	n	n+1	-
Burst Length	2 words:												
	4 words:												
	8 words:												
	Full Page: Column address is repeated until terminated.												

--- Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bits in the sequence shown in the following table.

Data n	Column Address								Burst Length	
Data 0	A7	A6	A5	A4	A3	A2	A1	A0	4 words	8 words
Data 1	A7	A6	A5	A4	A3	A2	A1	A0#		
Data 2	A7	A6	A5	A4	A3	A2	A1#	A0		
Data 3	A7	A6	A5	A4	A3	A2	A1#	A0#		
Data 4	A7	A6	A5	A4	A3	A2#	A1	A0		
Data 5	A7	A6	A5	A4	A3	A2#	A1	A0#		
Data 6	A7	A6	A5	A4	A3	A2#	A1#	A0		
Data 7	A7	A6	A5	A4	A3	A2#	A1#	A0#		

- CAS# Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CLK. The minimum whole value satisfying the following formula must be programmed into this field.

$t_{CAC}(min) \leq$ CAS# Latency X t_{CK}

A6	A5	A4	CAS# Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	X	X	Reserved

- Test Mode field (A8~A7)

These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

A8	A7	Test Mode
0	0	normal mode
0	1	Vendor Use Only
1	X	Vendor Use Only

- Write Burst Length (A9)

This bit is used to select the burst write length.

A9	Write Burst Length
0	Burst
1	Single Bit

9 No-Operation command

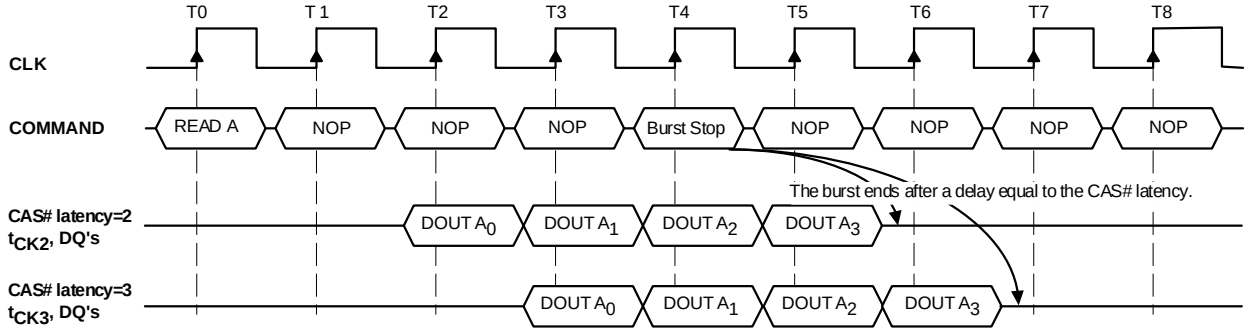
(RAS# = "H", CAS# = "H", WE# = "H")

The No-Operation command is used to perform a NOP to the SDRAM which is selected (CS# is Low). This prevents unwanted commands from being registered during idle or wait states.

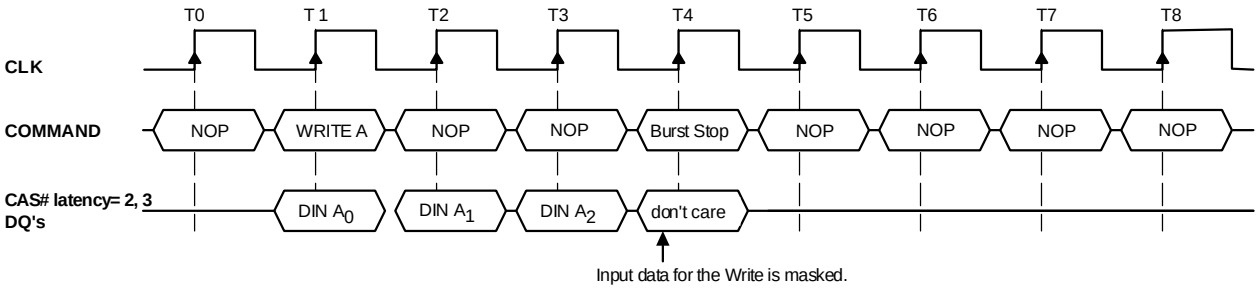
10 Burst Stop command

(RAS# = "H", CAS# = "H", WE# = "L")

The Burst Stop command is used to terminate either fixed-length or full-page bursts. This command is only effective in a read/write burst without the auto precharge function. The terminated read burst ends after a delay equal to the CAS# latency (refer to the following figure). The termination of a write burst is shown in the following figure.



Termination of a Burst Read Operation (Burst Length • 4, CAS# Latency = 2, 3)



Termination of a Burst Write Operation (Burst Length = X, CAS# Latency = 1, 2, 3)

11 Device Deselect command (CS# = "H")

The Device Deselect command disables the command decoder so that the RAS#, CAS#, WE# and Address inputs are ignored, regardless of whether the CLK is enabled. This command is similar to the No Operation command.

12 AutoRefresh command

(RAS# = "L", CAS# = "L", WE# = "H",CKE = "H", BS0,1 = "Don't care, A0-A10 = Don't care)

The AutoRefresh command is used during normal operation of the SDRAM and is analogous to CAS#-before-RAS# (CBR) Refresh in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AutoRefresh command. The internal refresh counter increments automatically on every auto refresh cycle to all of the rows. The refresh operation must be performed 4096 times within 64ms. The time required to complete the auto refresh operation is specified by t_{RC}(min.). To provide the AutoRefresh command, all banks need to be in the idle state and the device must not be in power down mode (CKE is high in the previous cycle). This command must be followed by NOPs until the auto refresh operation is completed. The precharge time requirement, t_{RP}(min), must be met before successive auto refresh operations are performed.

13 SelfRefresh Entry command

(RAS# = "L", CAS# = "L", WE# = "H", CKE = "L", A0-A10 = Don't care)

The SelfRefresh is another refresh mode available in the SDRAM. It is the preferred refresh mode for data retention and low power operation. Once the SelfRefresh command is registered, all the inputs to the SDRAM become "don't care" with the exception of CKE, which must remain LOW. The refresh addressing and timing is internally generated to reduce power consumption. The SDRAM may remain in SelfRefresh mode for an indefinite period. The SelfRefresh mode is exited by restarting the external clock and then asserting HIGH on CKE (SelfRefresh Exit command).

14 SelfRefresh Exit command

(CKE = "H", CS# = "H" or CKE = "H", RAS# = "H", CAS# = "H", WE# = "H")

This command is used to exit from the SelfRefresh mode. Once this command is registered, NOP or Device Deselect commands must be issued for t_{RC}(min.) because time is required for the completion of any bank currently being internally refreshed. If auto refresh cycles in bursts are performed during normal operation, a burst of 4096 auto refresh cycles should be completed just prior to entering and just after exiting the SelfRefresh mode.

15 Clock Suspend Mode Entry / PowerDown Mode Entry command (CKE = "L")

When the SDRAM is operating the burst cycle, the internal CLK is suspended(masked) from the subsequent cycle by issuing this command (asserting CKE "LOW"). The device operation is held intact while CLK is suspended. On the other hand, when all banks are in the idle state, this command performs entry into the PowerDown mode. All input and output buffers (except the CKE buffer) are turned off in the PowerDown mode. The device may not remain in the Clock Suspend or PowerDown state longer than the refresh period (64ms) since the command does not perform any refresh operations.

16 Clock Suspend Mode Exit / PowerDown Mode Exit command

When the internal CLK has been suspended, the operation of the internal CLK is reinitiated from the subsequent cycle by providing this command (asserting CKE "HIGH"). When the device is in the PowerDown mode, the device exits this mode and all disabled buffers are turned on to the active state. t_{PDE}(min.) is required when the device exits from the PowerDown mode. Any subsequent commands can be issued after one clock cycle from the end of this command.

17 Data Write / Output Enable, Data Mask / Output Disable command (DQM = "L", "H")

During a write cycle, the DQM signal functions as a Data Mask and can control every word of the input data. During a read cycle, the DQM functions as the controller of output buffers. DQM is also used for device selection, byte selection and bus control in a memory system.

Absolute Maximum Rating

Symbol	Item	Leaded Package	Lead Free Package	Unit	Note
V_{IN}, V_{OUT}	Input, Output Voltage	-1~4.6		V	1
V_{DD}, V_{DDQ}	Power Supply Voltage	- 1~4.6		V	1
T_{OPR}	Operating Temperature	0~70		°C	1
T_{STG}	Storage Temperature	- 55~150		°C	1
T_{SOLDER}	Soldering Temperature (10s)	240	260	°C	1
P_D	Power Dissipation	1		W	1
I_{OUT}	Short Circuit Output Current	50		mA	1

Recommended D.C. Operating Conditions (Ta = 0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{DDQ}	Power Supply Voltage(for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	-	V_{DDQ} + 0.3	V	2
V_{IL}	LVTTL Input Low Voltage	- 0.3	-	0.8	V	2

Capacitance (V_{DD} = 3.3V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance	-	4.5	pF
$C_{I/O}$	Input/Output Capacitance	-	6.5	pF

Note: These parameters are periodically sampled and are not 100%

Recommended D.C. Operating Conditions (V_{DD} = 3.3V ± 0.3V, Ta = 0~70°C)

Description/Test condition		Symbol	- 5/5.5/6/7/8/10 Max.	Unit	Note
Operating Current $t_{RC} \geq t_{RC}$(min), Outputs Open, Input signal one transition per one cycle	1 bank operation	I_{CC1}	200/190/180/155/135/120	mA	3
Precharge Standby Current in power down mode t_{CK} = 15ns, CKE ≤ V_{IL}(max)		I_{CC2P}	3		3
Precharge Standby Current in power down mode t_{CK} = ∞, CKE ≤ V_{IL}(max)		I_{CC2PS}	3		
Precharge Standby Current in non-power down mode t_{CK} = 15ns, CS# ≥ V_{IH}(min), CKE ≥ V_{IH} Input signals are changed once during 30ns.		I_{CC2N}	25		3
Precharge Standby Current in non-power down mode t_{CK} = ∞, CLK ≤ V_{IL}(max), CKE ≥ V_{IH}		I_{CC2NS}	15		
Active Standby Current in power down mode CKE ≤ V_{IL}(max), t_{CK} = 15ns		I_{CC3P}	5		3
Active Standby Current in power down mode CKE & CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3PS}	5		3
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), t_{CK} = 15ns		I_{CC3N}	40		
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3NS}	30		
Operating Current (Burst mode) t_{CK} =t_{CK}(min), Outputs Open, Multi-bank interleave		I_{CC4}	225/215//200/180/150/130		3, 4
Refresh Current $t_{RC} \geq T_{rC}$(min)		I_{CC5}	260/240/220/210/190/180		3
Self Refresh Current CKE ≤ 0.2V		I_{CC6}	2		

Parameter	Description	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current (0V • V_{IN} • V_{DD}, All other pins not under test = 0V)	- 1.5	1.5	uA	
V_{OH}	LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)	2.4	-	V	
V_{OL}	LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)	-	0.4	V	

Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 3.3V ± 0.3V, Ta = 0~70°C) (Note: 5, 6, 7, 8)

Symbol	A.C. Parameter		- 5/5.5/6/7/8/10		Unit	Note
			Min.	Max.		
t_{RC}	Row cycle time (same bank)		55/55/60/70/80/100		ns	9
t_{RRD}	Row activate to row activate delay (different banks)		10/11/12/14/16/20			9
t_{RCD}	RAS# to CAS# delay (same bank)		18/18/18/21/24/30			9
t_{RP}	Precharge to refresh/row activate command (same bank)		15/16.5/18/21/24/30			9
t_{RAS}	Row activate to precharge time (same bank)		35/38.5/42/49/56/70	100,000		9
t_{CK2}	Clock cycle time	CL* = 2	-/-/10/10/ - / -			
t_{CK3}		CL* = 3	5/5.5/6/7/8/10			
t_{AC2}	Access time from CLK	CL* = 2		-/-/6/6/-/-		9
t_{AC3}	(positive edge)	CL* = 3		4.5/5/5.5/5.5/6/6		
t_{OH}	Data output hold time		2/2/2/2.5/2.5/2.5			9
t_{CH}	Clock high time		2/2/2.5/3/3/3.5			10
t_{CL}	Clock low time		2/2/2.5/3/3/3.5			10
t_{IS}	Data/Address/Control Input set-up time		1.5/1.5/1.5/1.75/2/2.5			10
t_{IH}	Data/Address/Control Input hold time		1			10
t_{LZ}	Data output low impedance		1			9
t_{HZ2}	Data output high impedance	CL* = 2		-/-/6/6/-/-		
t_{HZ3}		CL* = 3		4.5/5/5.5/5.5/6/6		8
t_{WR}	Write recovery time		2		CLK	
t_{CCD}	CAS# to CAS# Delay time		2/1/1/1/1/1			
t_{MRS}	Mode Register Set cycle time		2			

* CL is CAS# Latency.

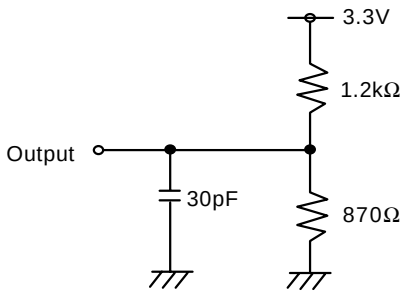
Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}. VIL(Max) = VDDQ+1.0V for pulse width ≤ 2ns. VIL(Min) = -1.0V for pulse width ≤ 2.0ns
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power-up sequence is described in Note 11.

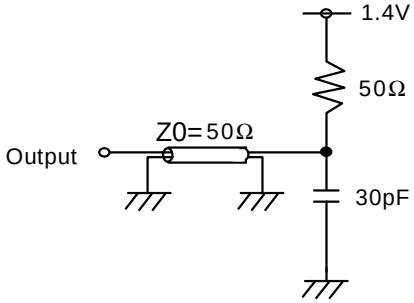
6. A.C. Test Conditions

LVTTL Interface

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V / 0.4V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

7. Transition times are measured between V_{IH} and V_{IL}. Transition(rise and fall) of input signals are in a fixed slope (1 ns).
8. t_{HZ} defines the time in which the outputs achieve the open circuit condition and are not at reference levels.
9. If clock rising time is longer than 1 ns, (t_R / 2 -0.5) ns should be added to the parameter.
10. Assumed input rise and fall time t_T (t_R & t_F) = 1 ns

    If t_R or t_F is longer than 1 ns, transient time compensation should be considered, i.e., [(tr + tf)/2 - 1] ns should be added to the parameter.
11. Power up Sequence

    Power up must be performed in the following sequence.

    1) Power must be applied to V_{DD} and V_{DDQ}(simultaneously) when all input signals are held "NOP" state and both CKE = "H" and DQM = "H." The CLK signals must be started at the same time.
    2) After power-up, a pause of 200□seconds minimum is required. Then, it is recommended that DQM is held "HIGH" (V_{DD} levels) to ensure DQ output is in high impedance.
    3) All banks must be precharged.
    4) Mode Register Set command must be asserted to initialize the Mode register.
    5) A minimum of 2 Auto-Refresh dummy cycles must be required to stabilize the internal circuitry of the device.

Timing Waveforms

Figure 1. AC Parameters for Write Timing (Burst Length=4, CAS# Latency=2)

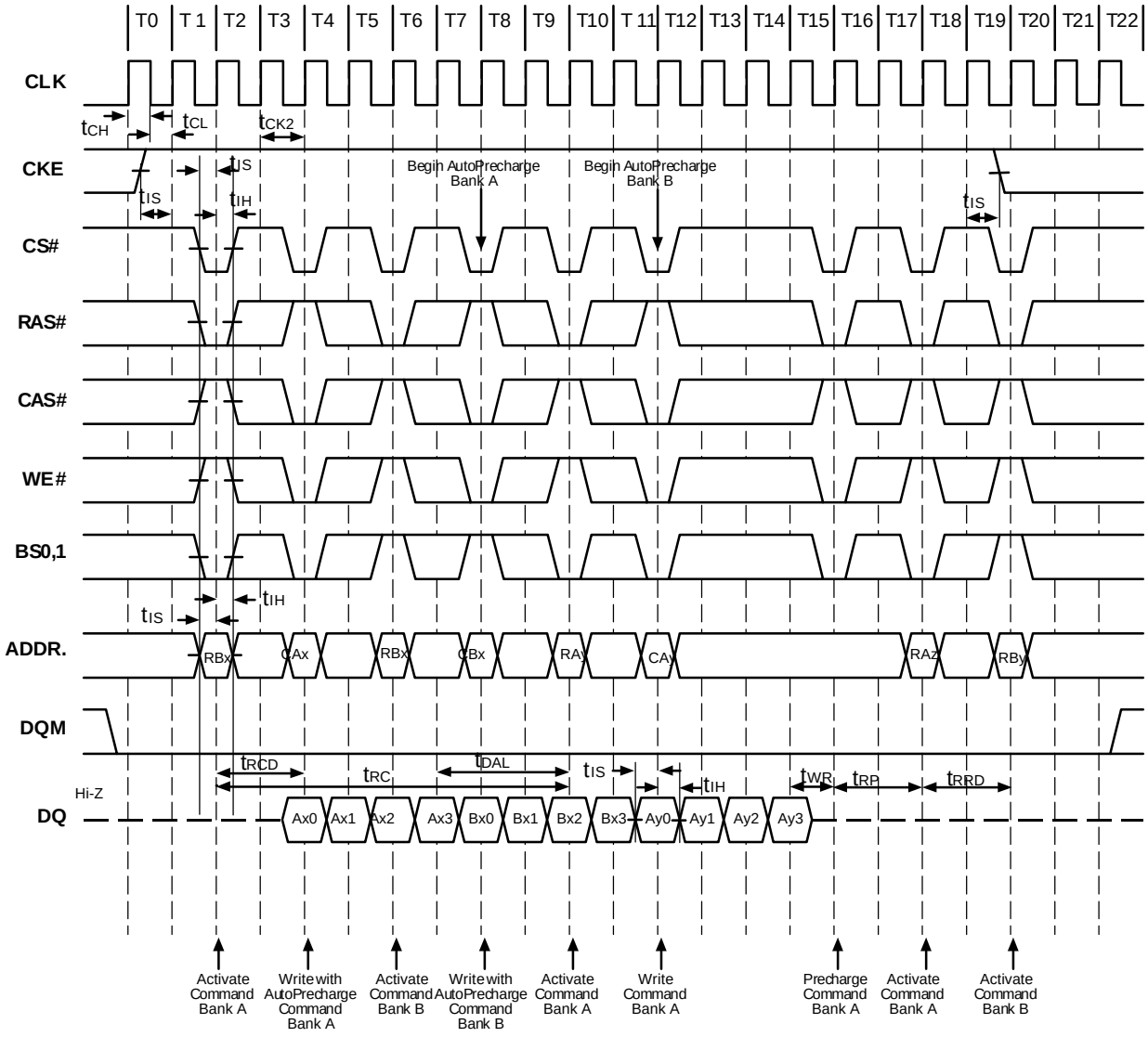


Figure 2. AC Parameters for Read Timing (Burst Length=2, CAS# Latency=2)

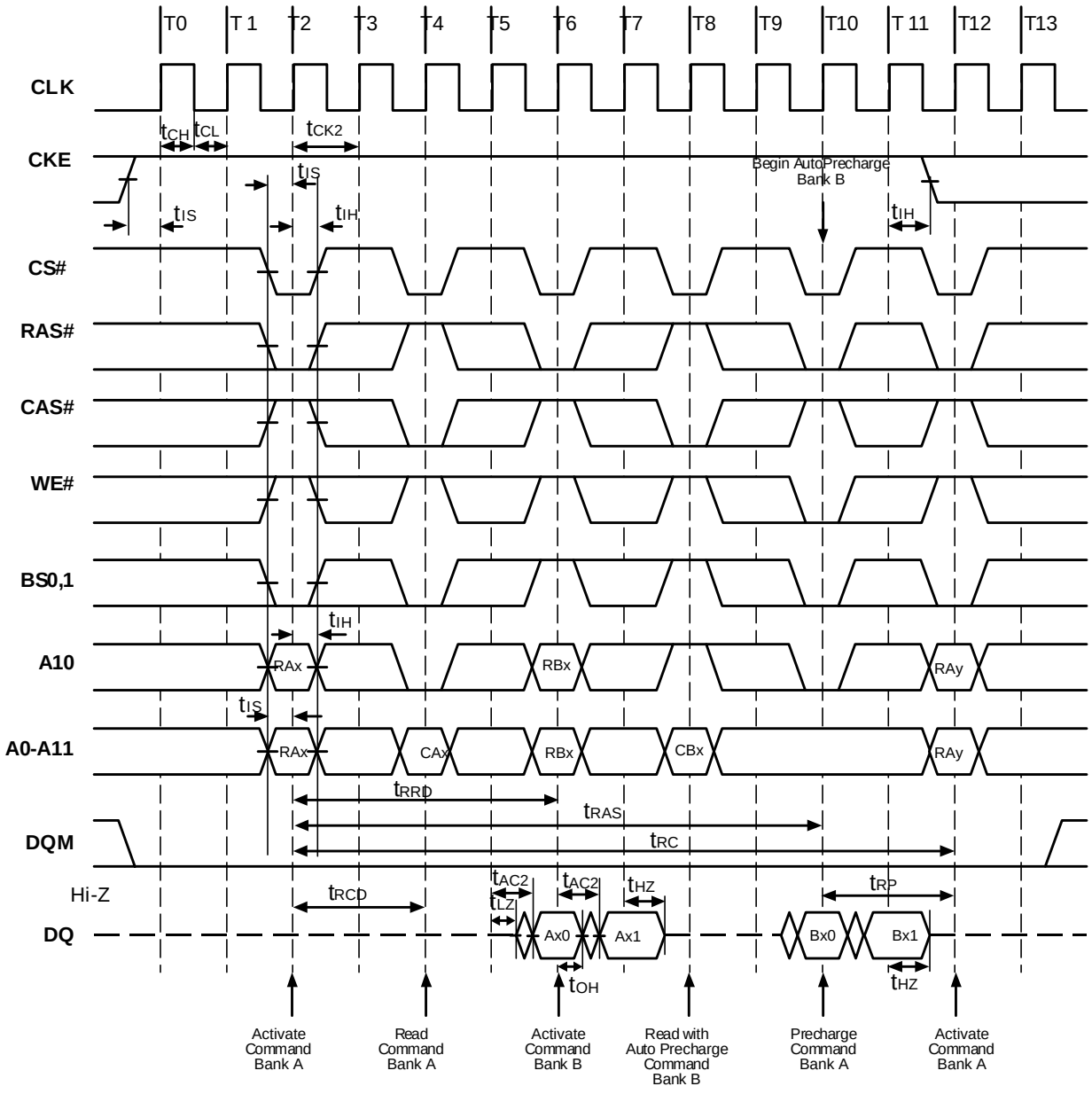


Figure 3. Auto Refresh (CBR) (Burst Length=4, CAS# Latency=2)

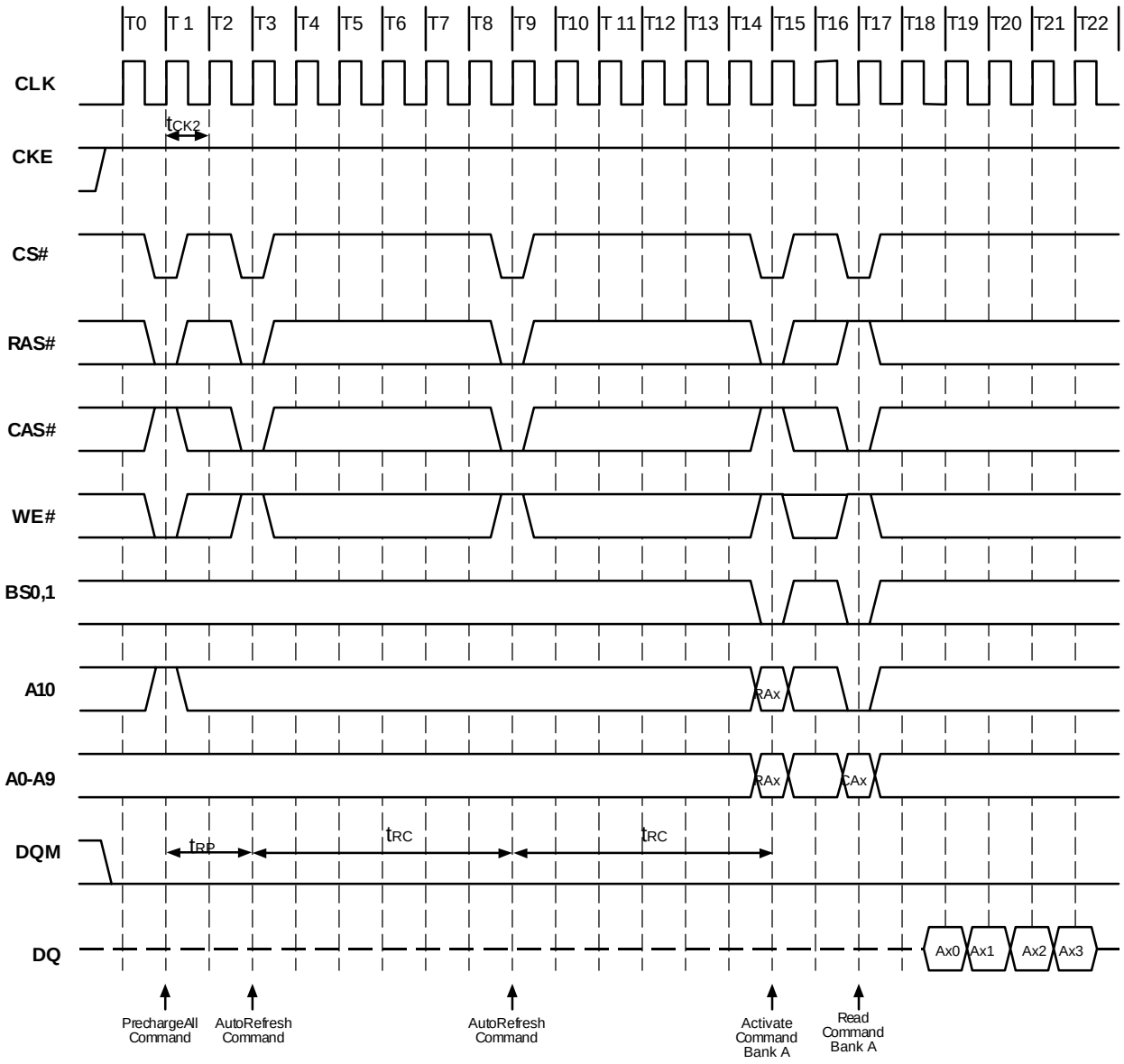


Figure 4. Power on Sequence and Auto Refresh (CBR)

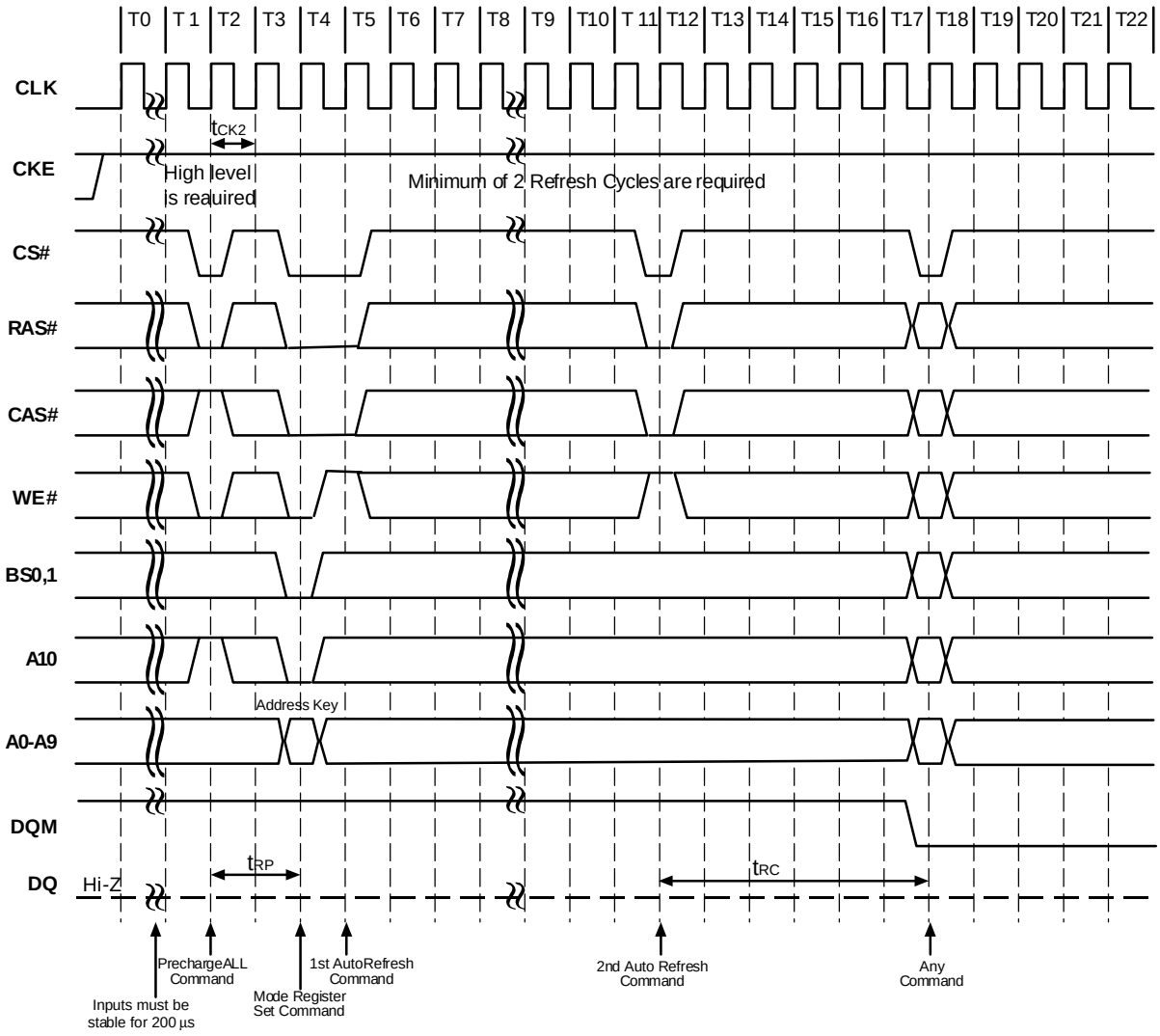
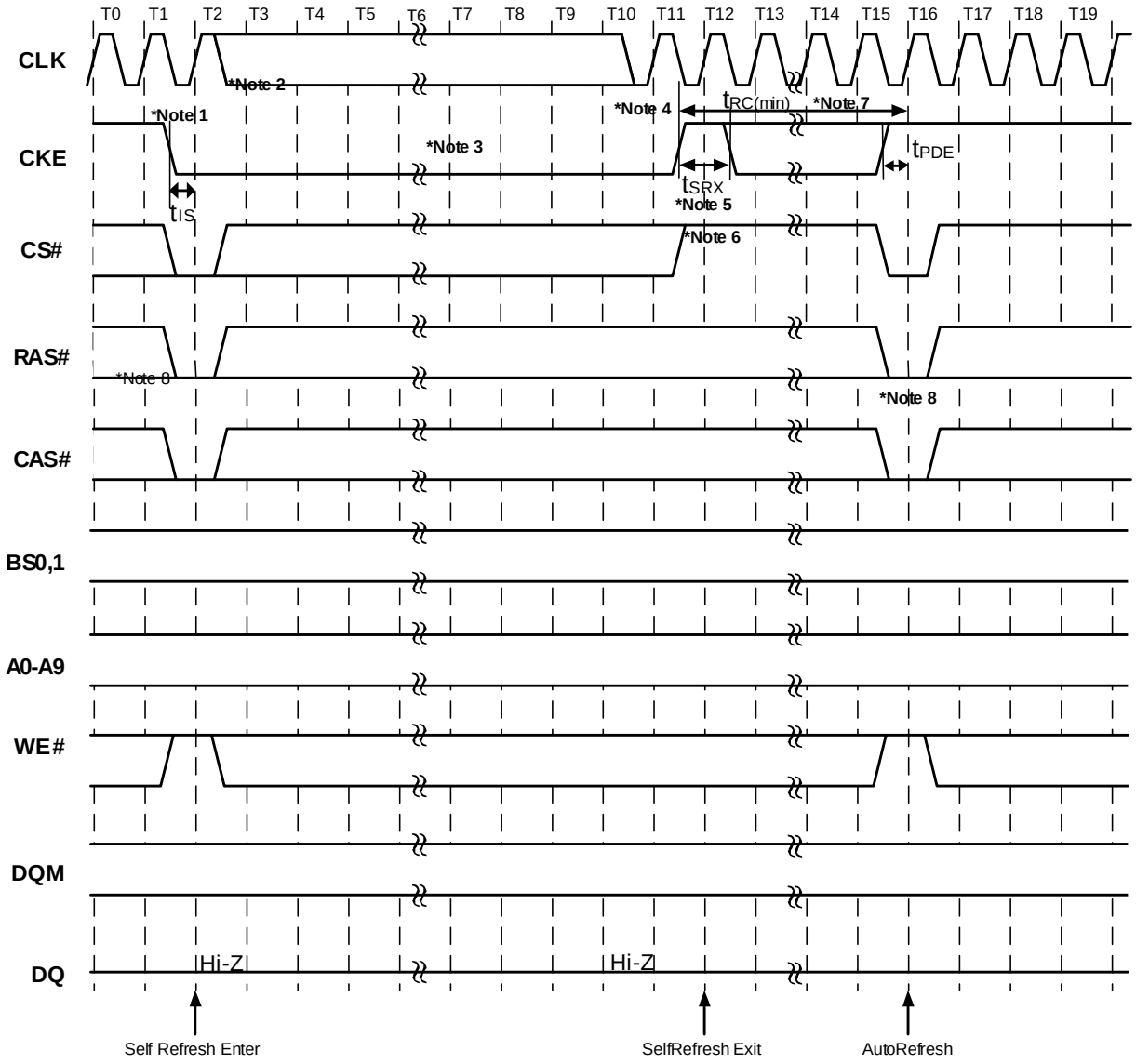


Figure 5. Self Refresh Entry & Exit Cycle



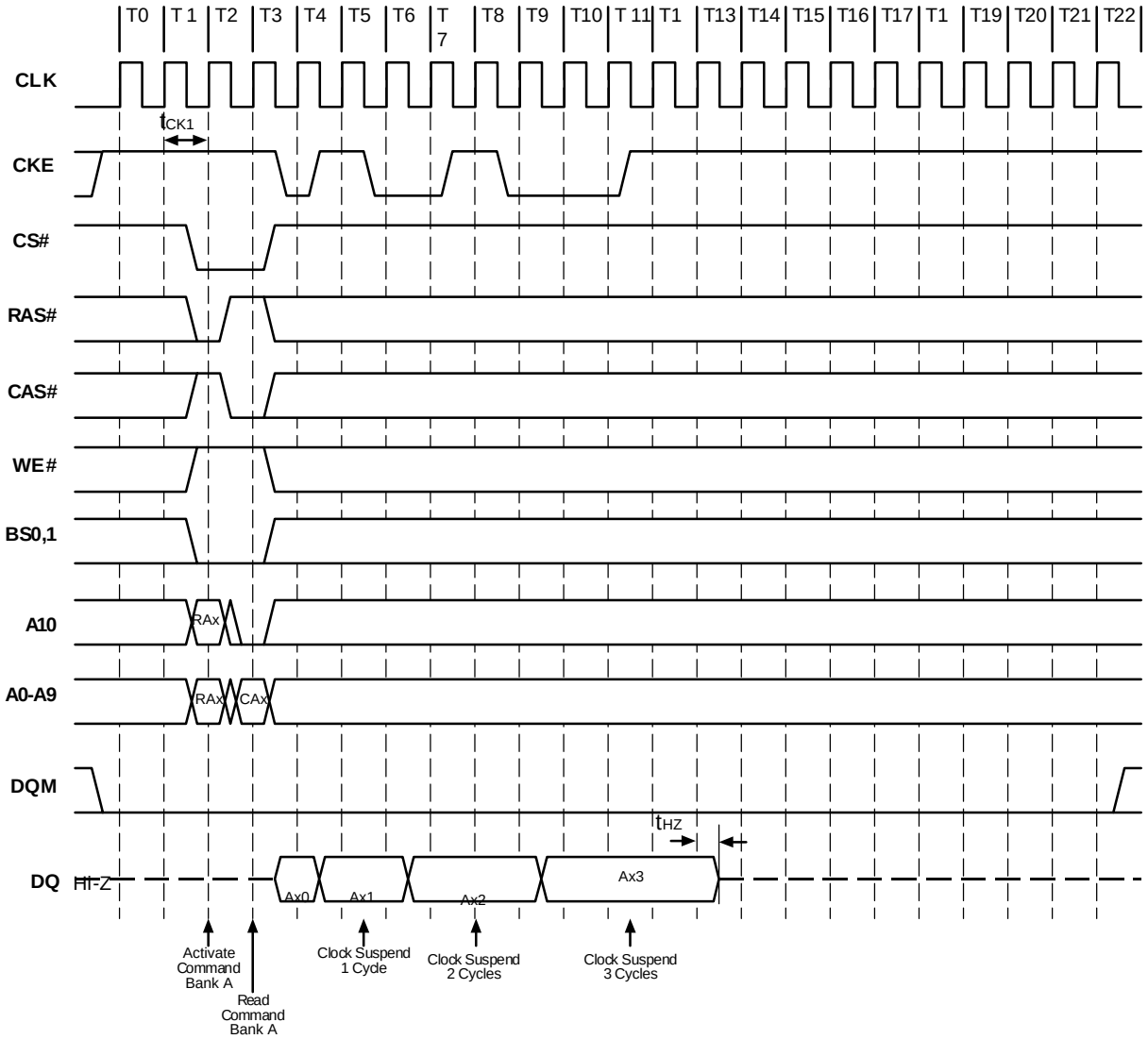
Note: To Enter SelfRefresh Mode

1. CS#, RAS# & CAS# with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in SelfRefresh mode as long as CKE stays "low".
4. Once the device enters SelfRefresh mode, minimum t_{RAS} is required before exit from SelfRefresh.

To Exit SelfRefresh Mode

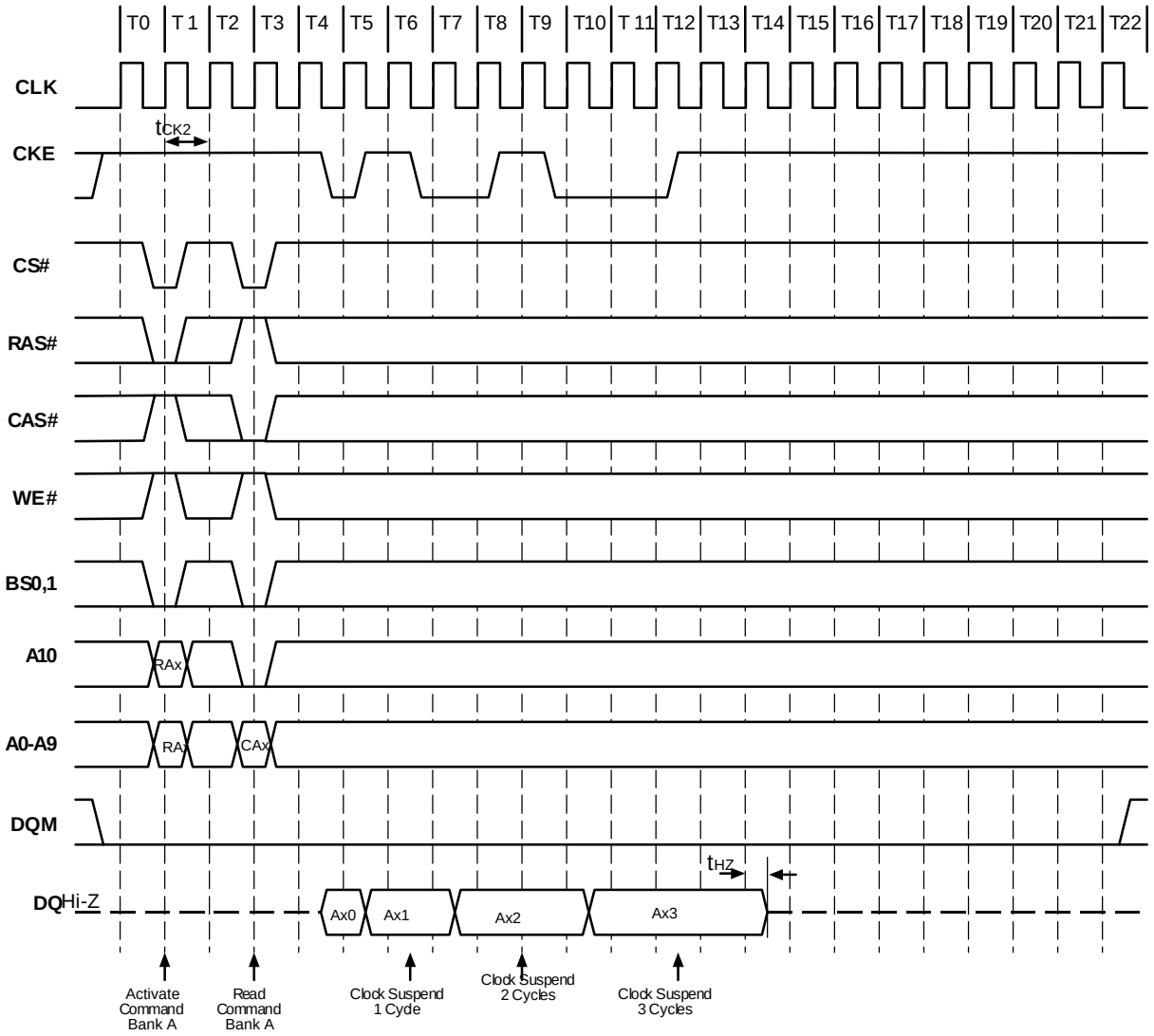
5. System clock restart and be stable before returning CKE high.
6. Enable CKE and CKE should be set high for minimum time of t_{SRX}.
7. CS# starts from high.
8. Minimum t_{RC} is required after CKE going high to complete SelfRefresh exit.
9. 4096 cycles of burst AutoRefresh is required before SelfRefresh entry and after SelfRefresh exit if the system uses burst refresh.

Figure 6.1. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=1)



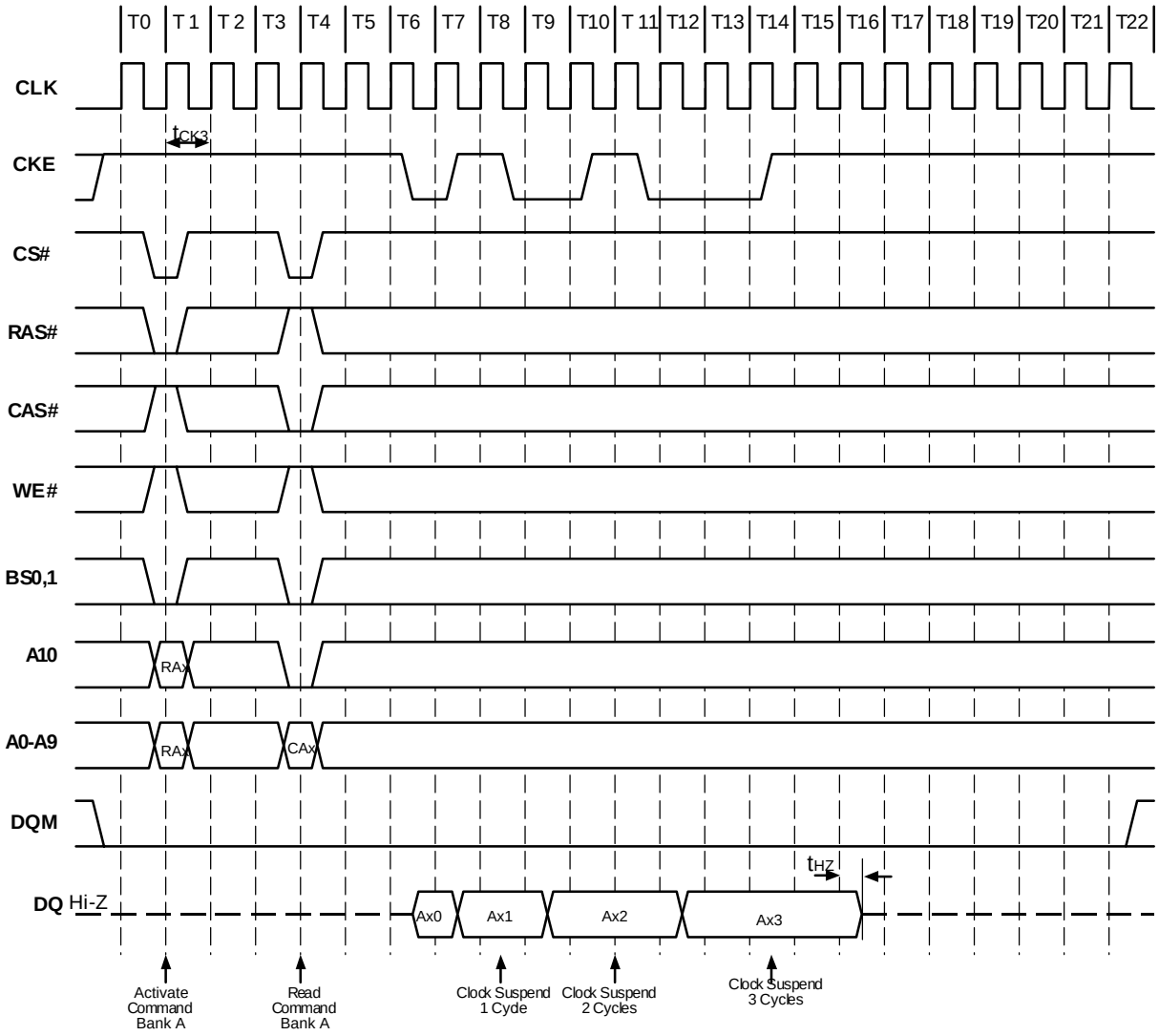
Note: CKE to CLK disable/enable = 1 clock

Figure 6.2. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=2)



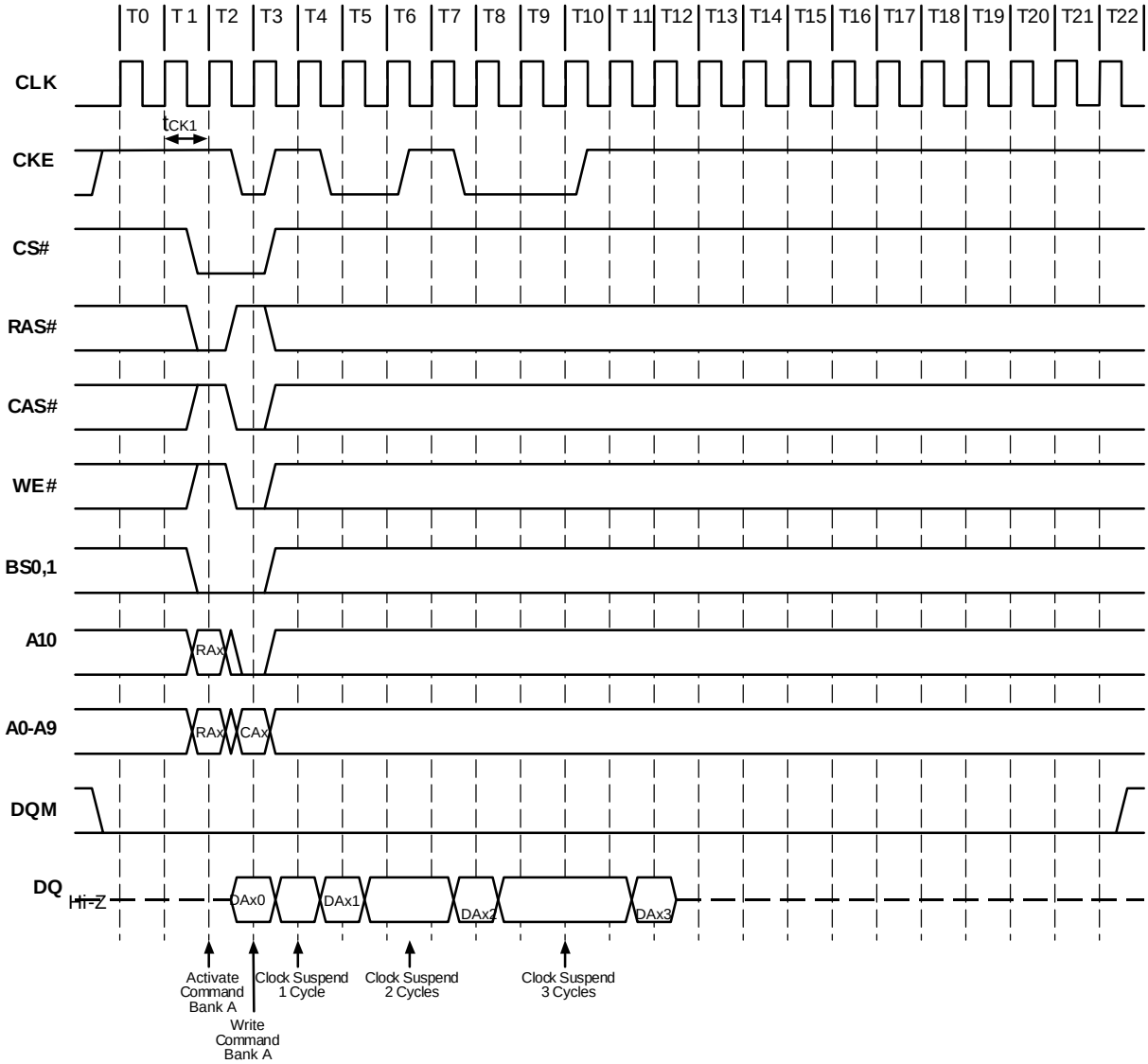
Note: CKE to CLK disable/enable = 1 clock

Figure 6.3. Clock Suspension During Burst Read (Using CKE)
(Burst Length=4, CAS# Latency=3)



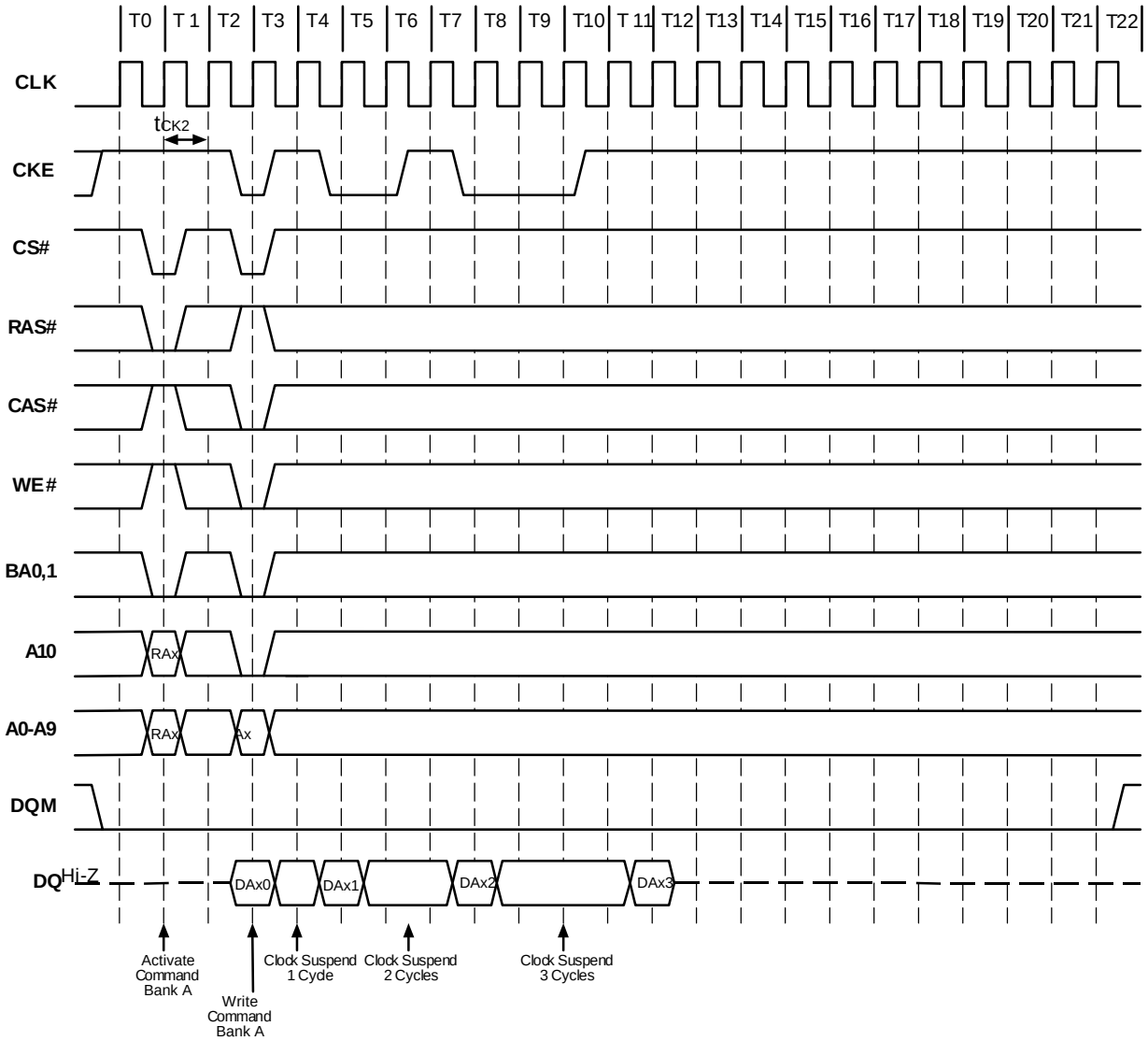
Note: CKE to CLK disable/enable = 1 clock

Figure 7.1. Clock Suspension During Burst Write (Using CKE)
(Burst Length = 4, CAS# Latency = 1)



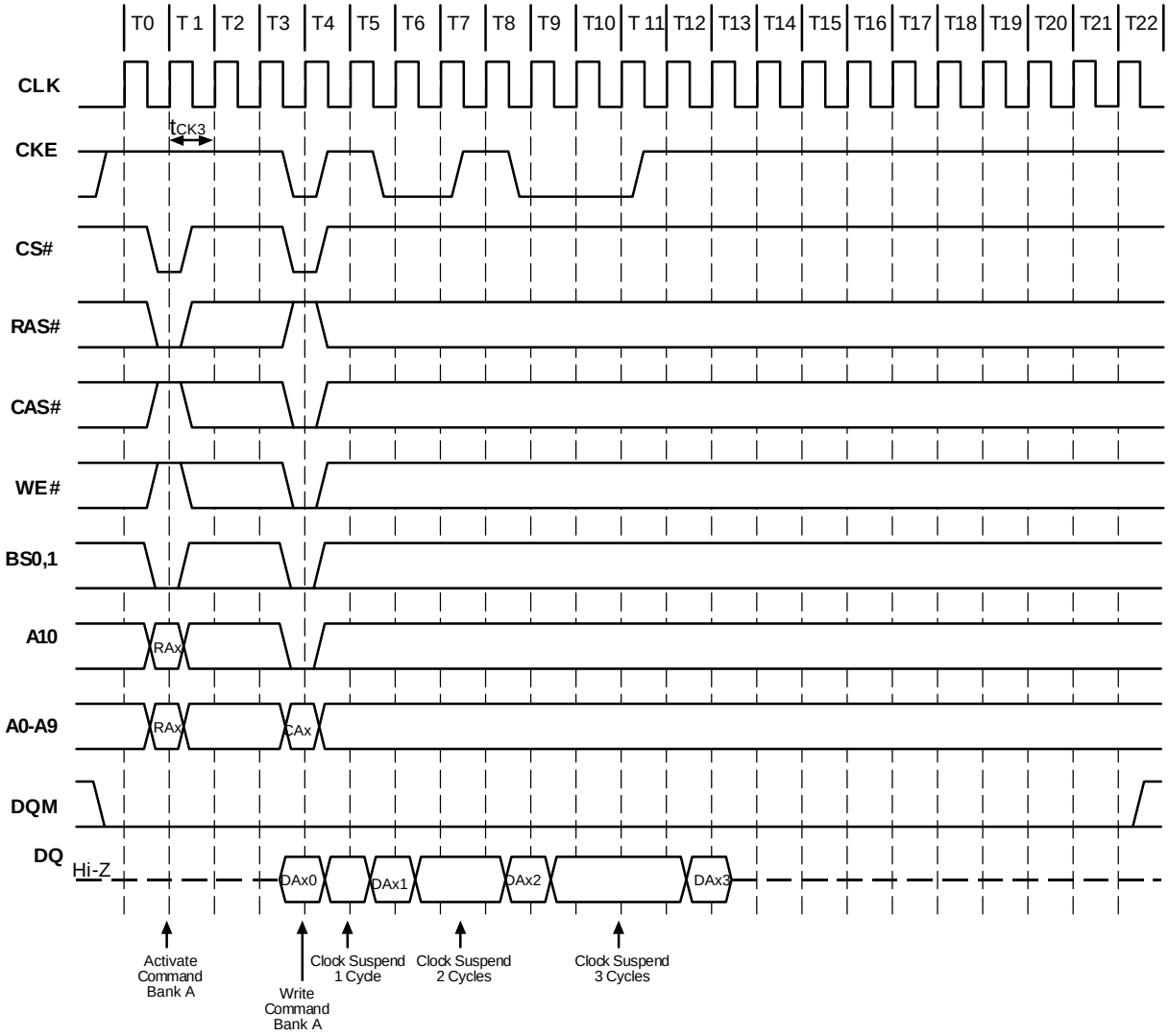
Note: CKE to CLK disable/enable = 1 clock

Figure 7.2. Clock Suspension During Burst Write (Using CKE)
(Burst Length=4, CAS# Latency=2)



Note: CKE to CLK disable/enable = 1 clock

Figure 7.3. Clock Suspension During Burst Write (Using CKE)
(Burst Length=4, CAS# Latency=3)



Note: CKE to CLK disable/enable = 1 clock

Figure 8. Power Down Mode and Clock Mask (Burst Length=4, CAS# Latency=2)

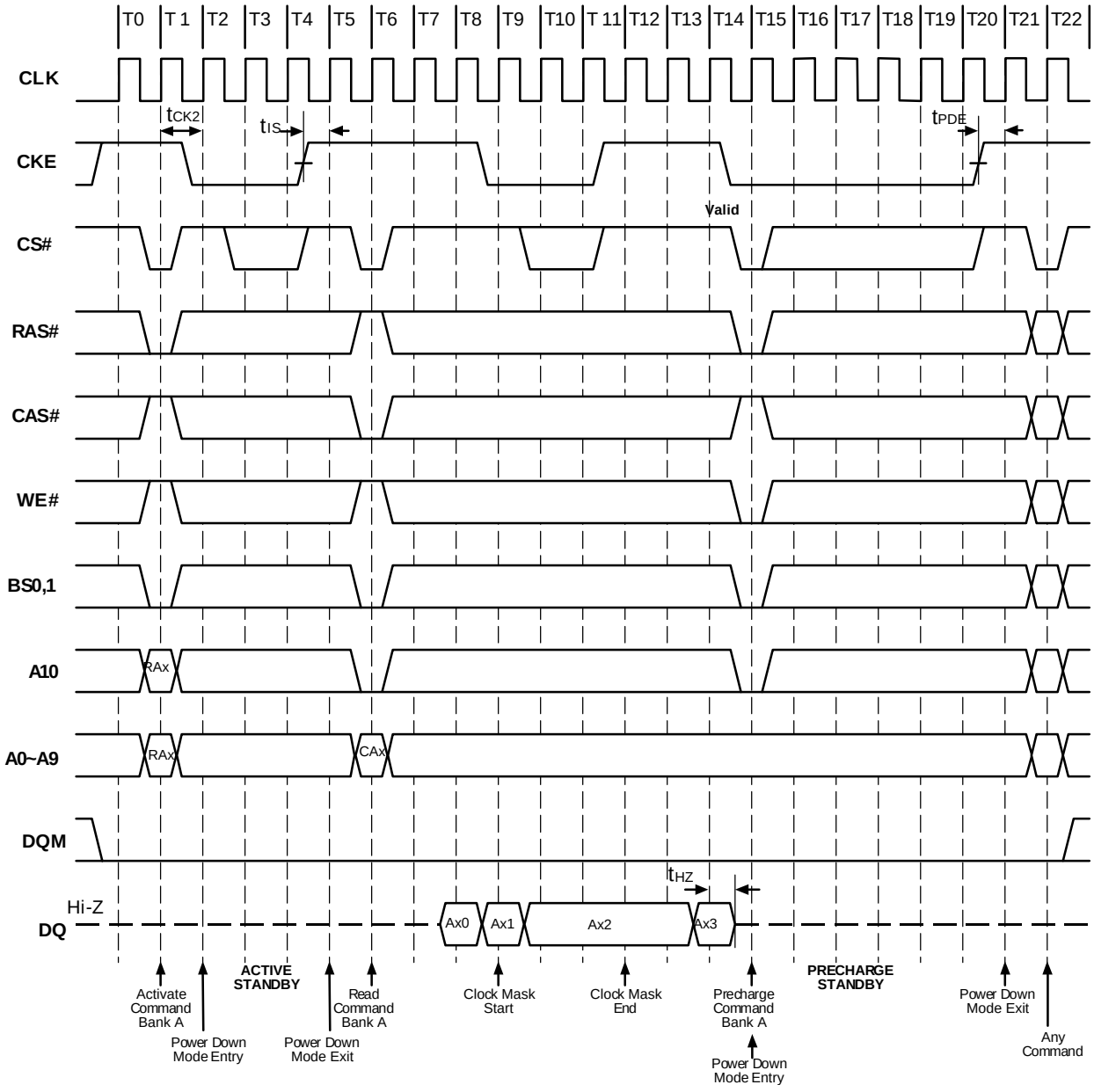


Figure 9.1. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=1)

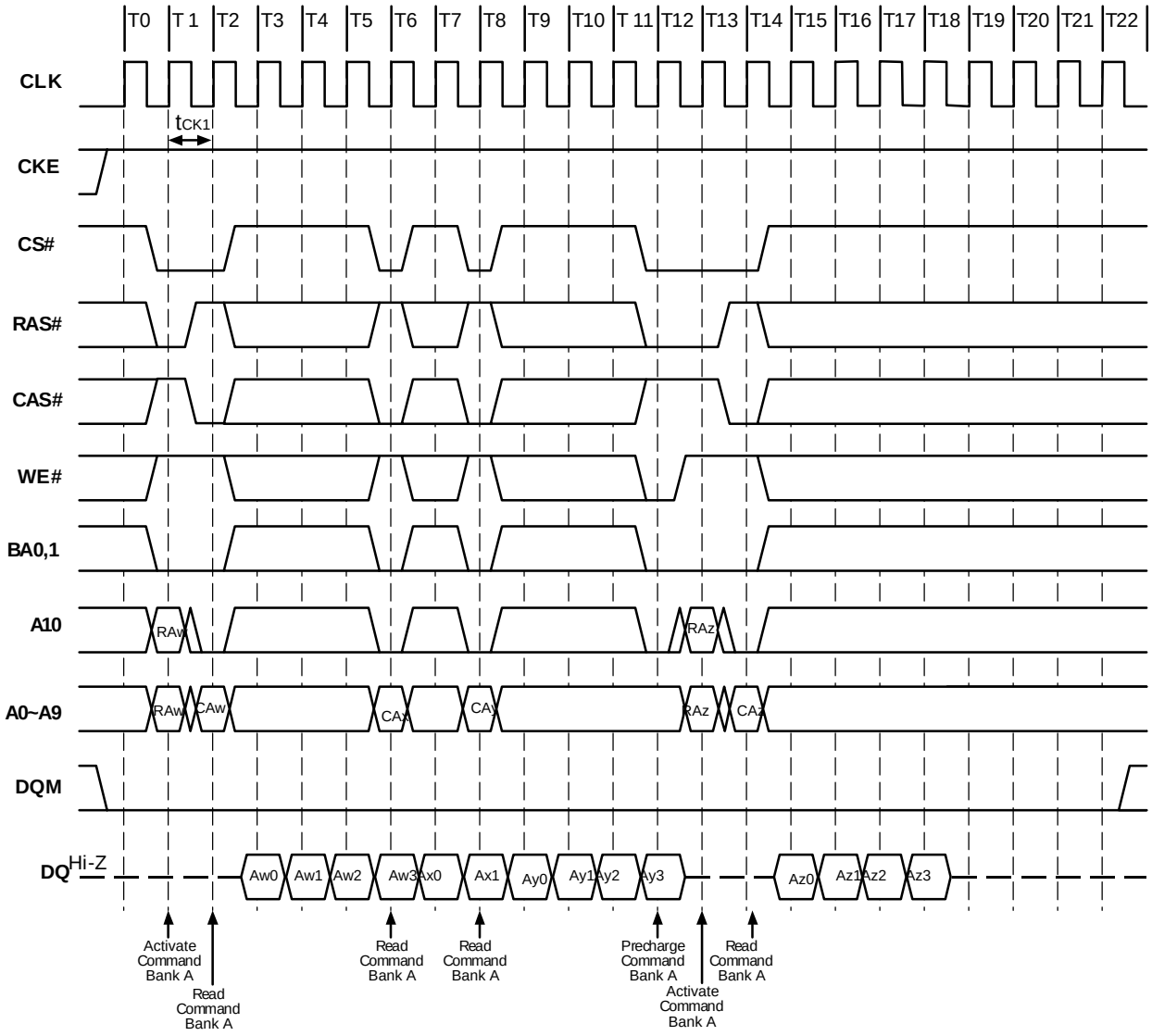


Figure 9.2. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=2)

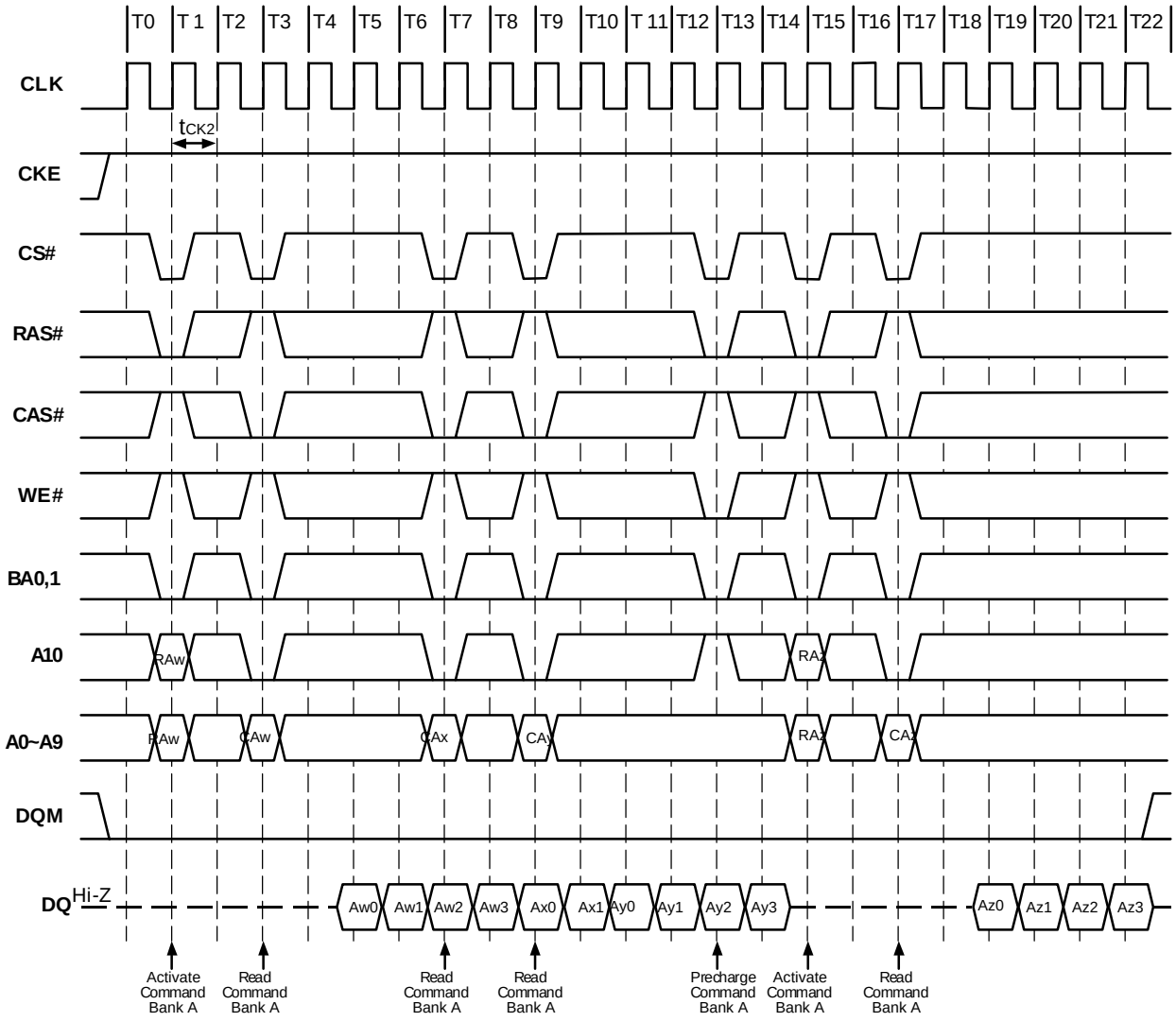


Figure 9.3. Random Column Read (Page within same Bank)
(Burst Length=4, CAS# Latency=3)

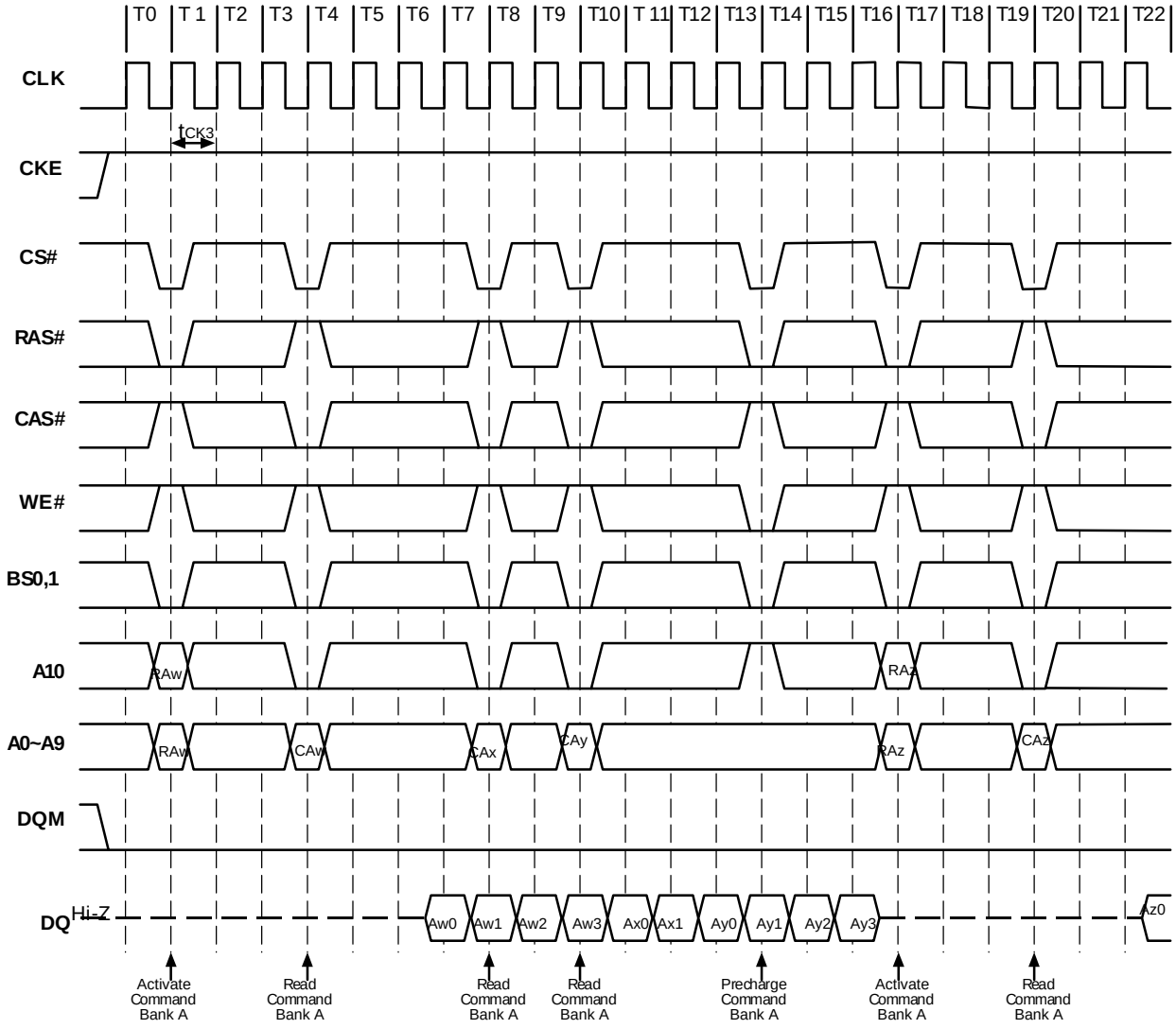


Figure 10.1. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=1)

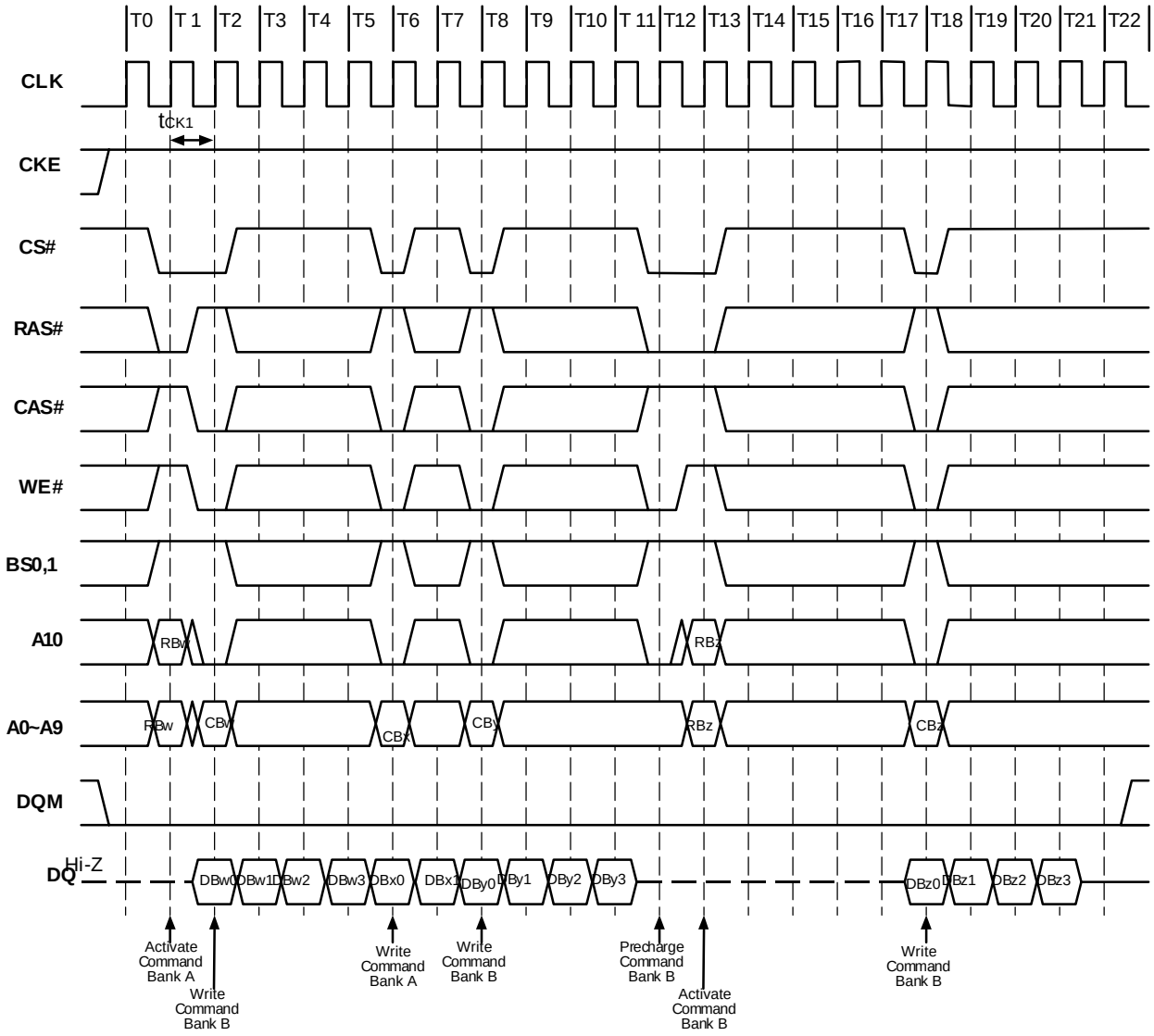


Figure 10.2. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=2)

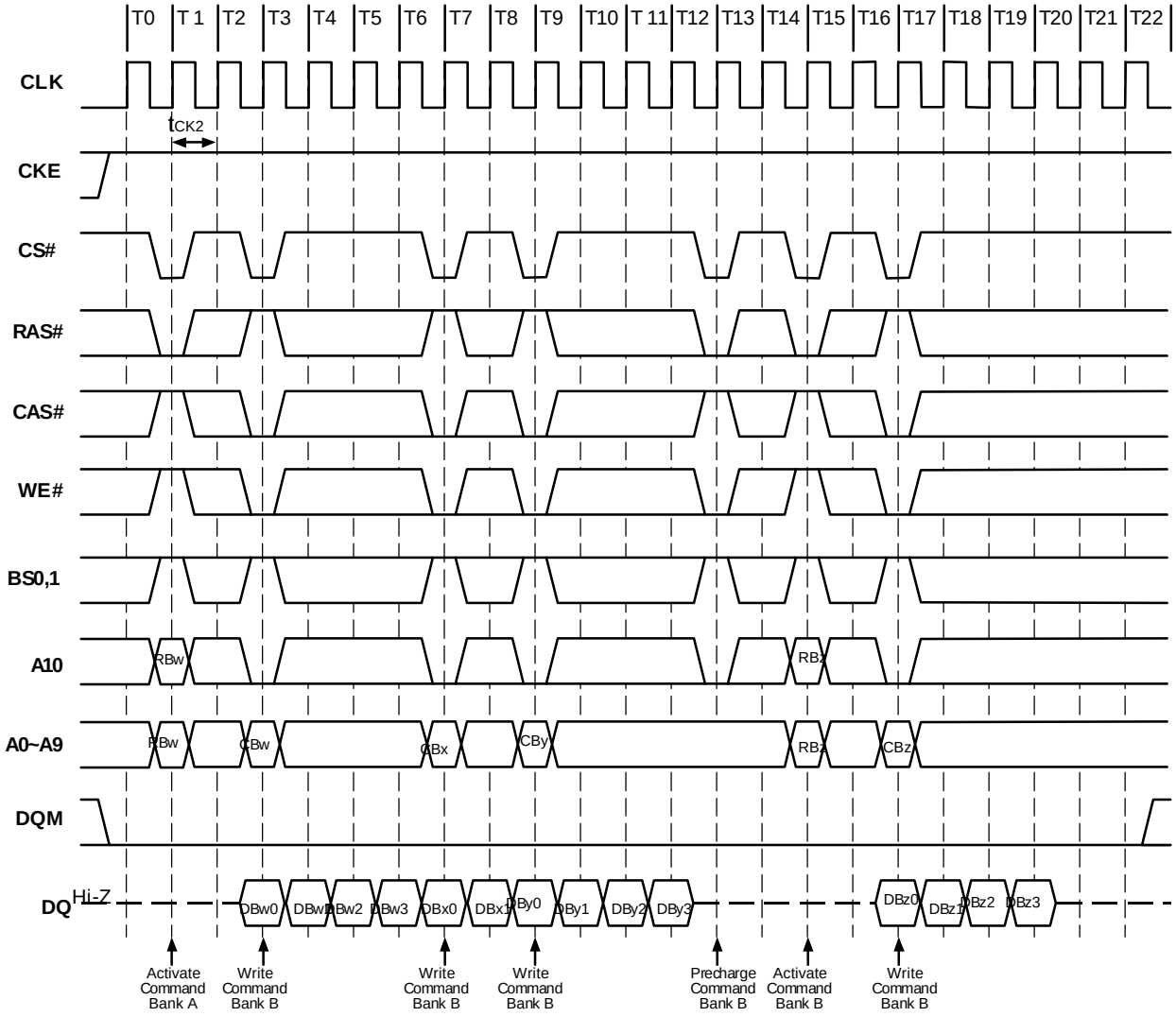


Figure 10.3. Random Column Write (Page within same Bank)
(Burst Length=4, CAS# Latency=3)

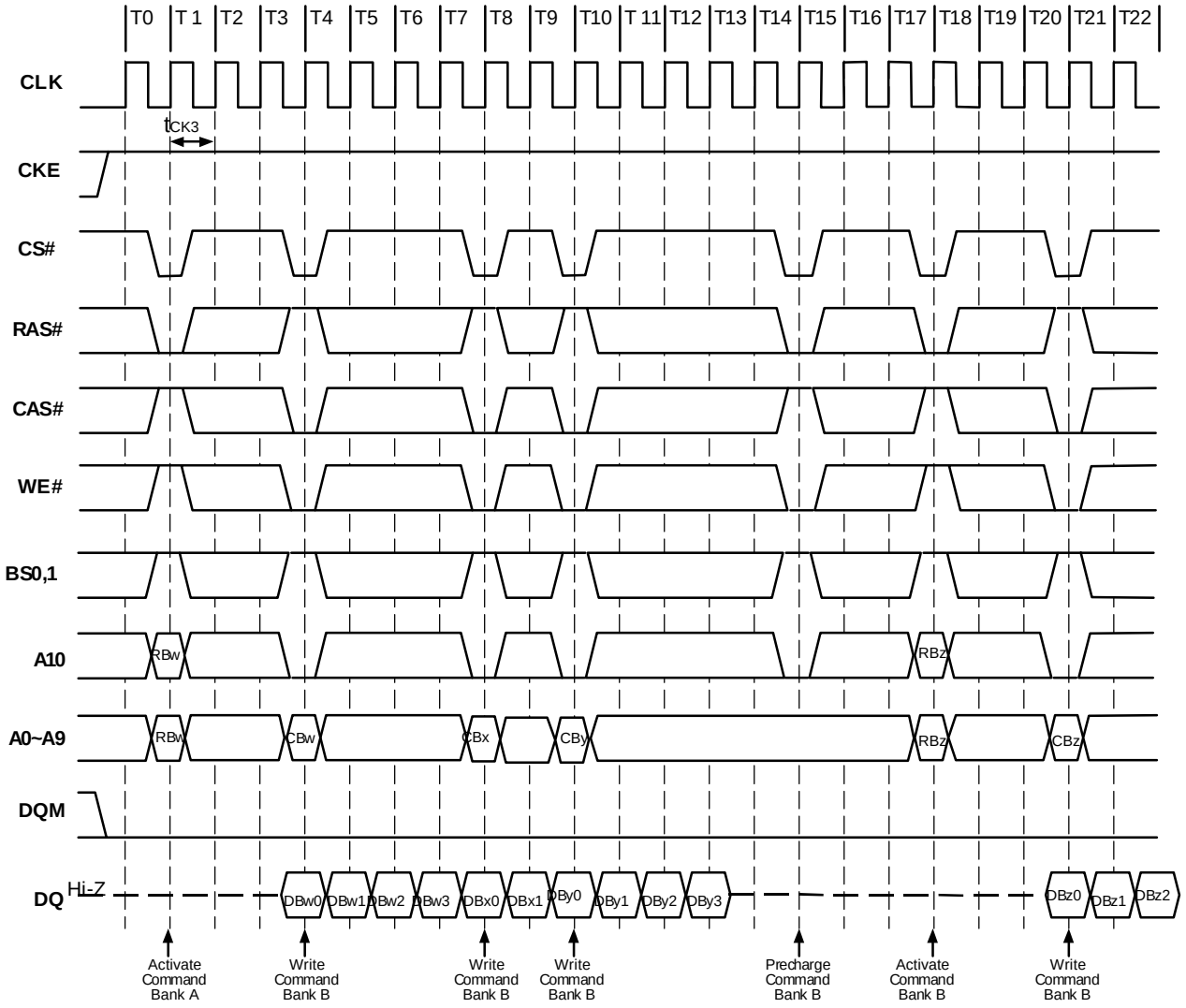


Figure 11.1. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=1)

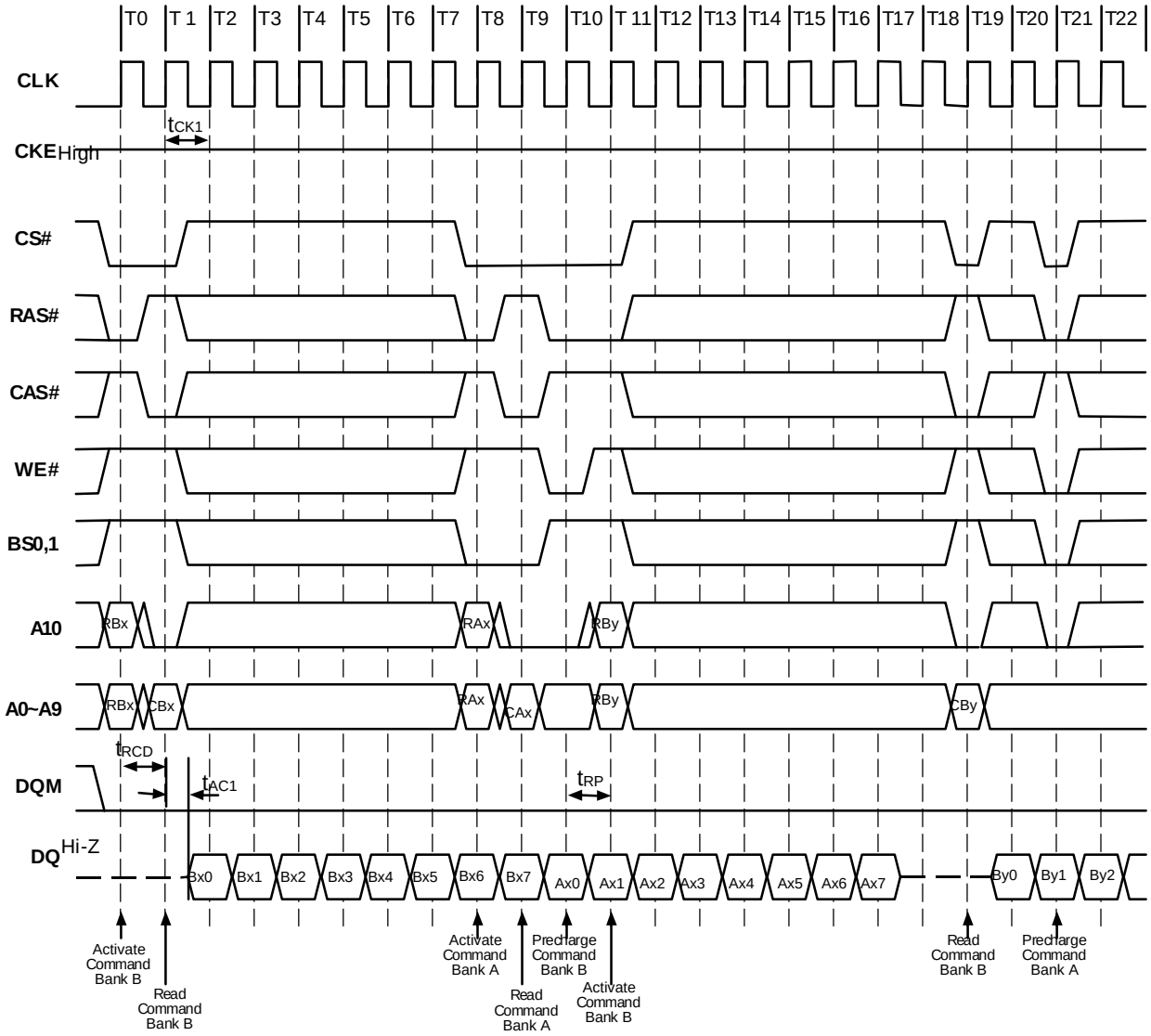


Figure 11.2. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=2)

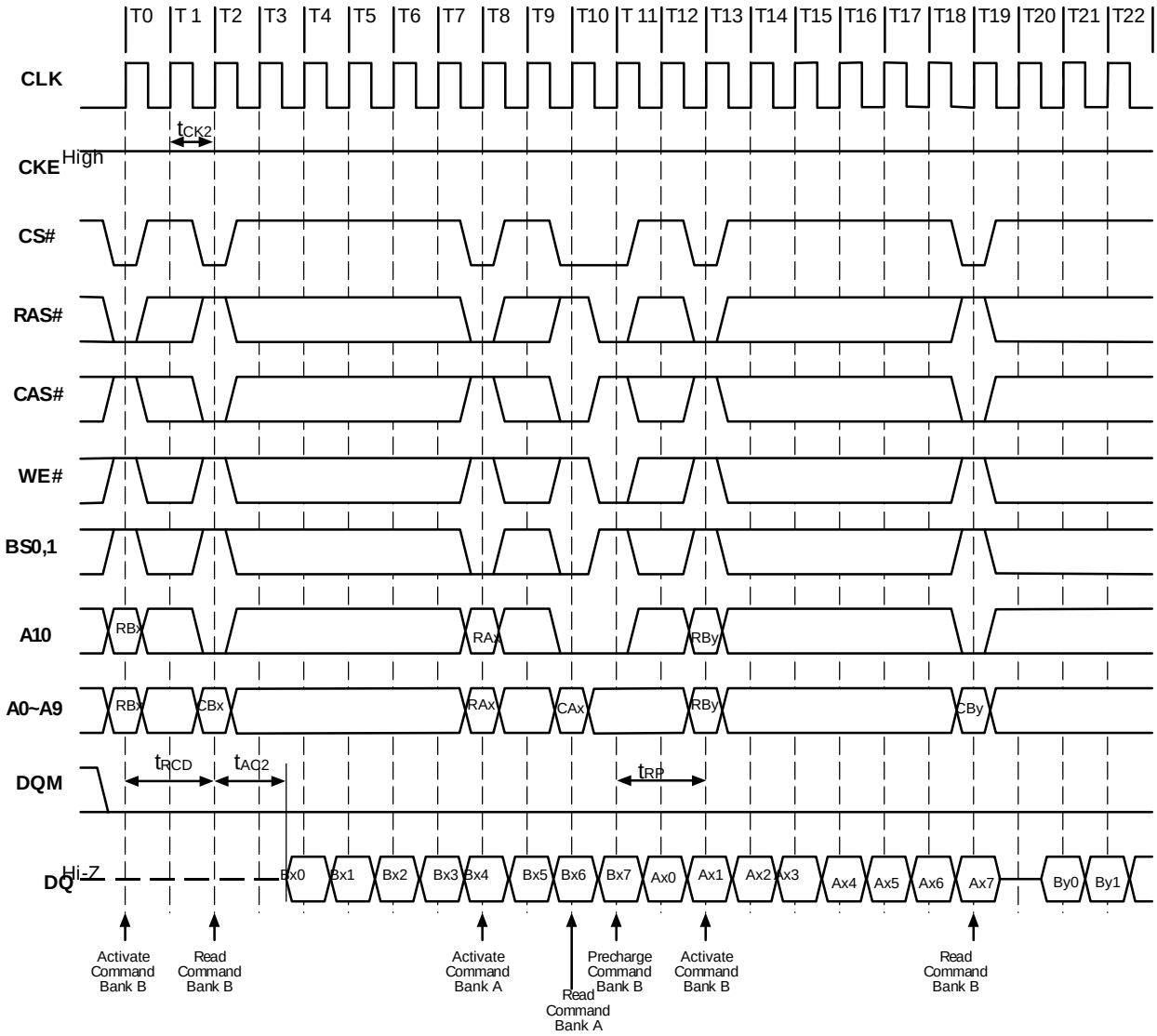


Figure 11.3. Random Row Read (Interleaving Banks)
(Burst Length=8, CAS# Latency=3)

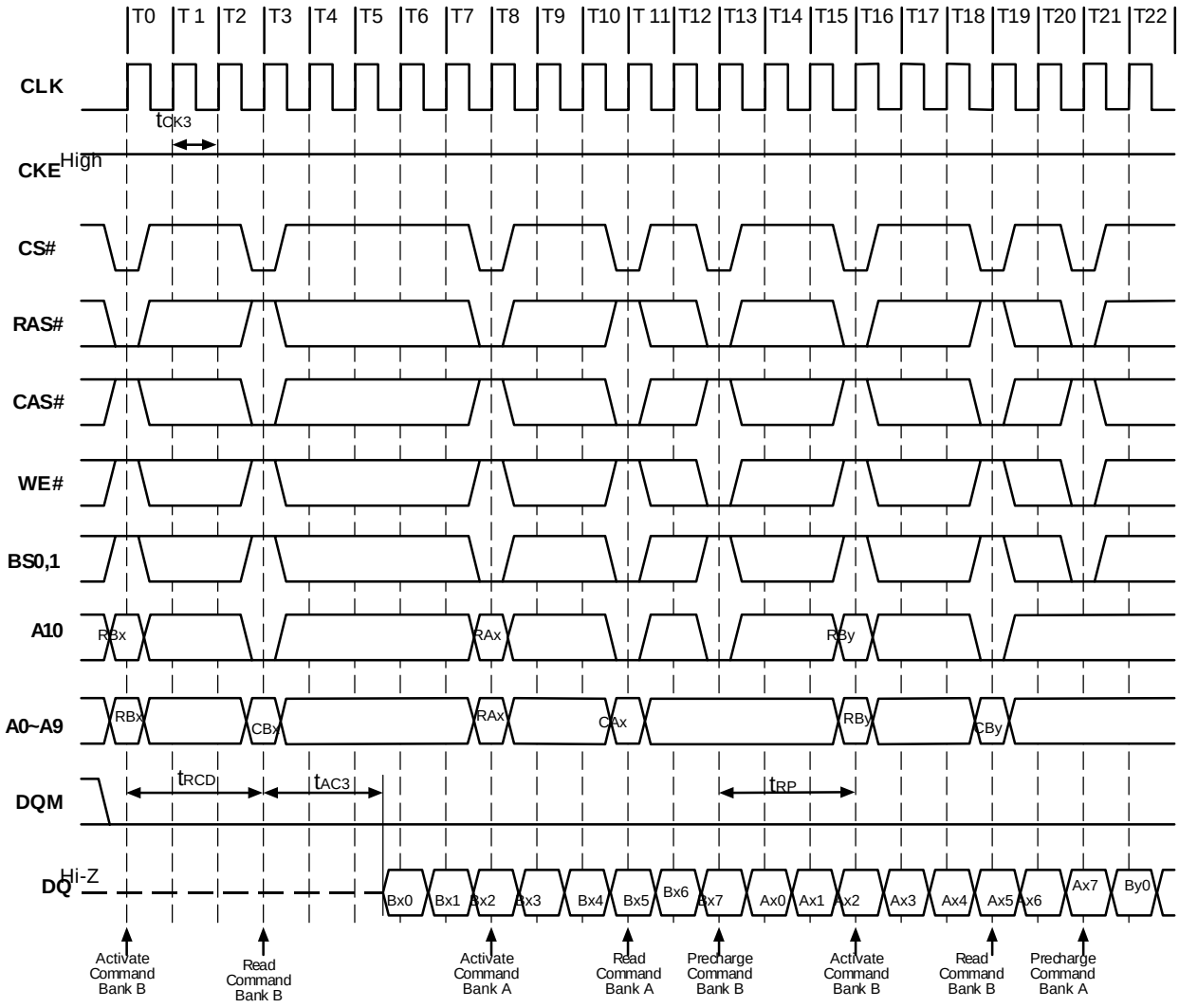


Figure 12.1. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=1)

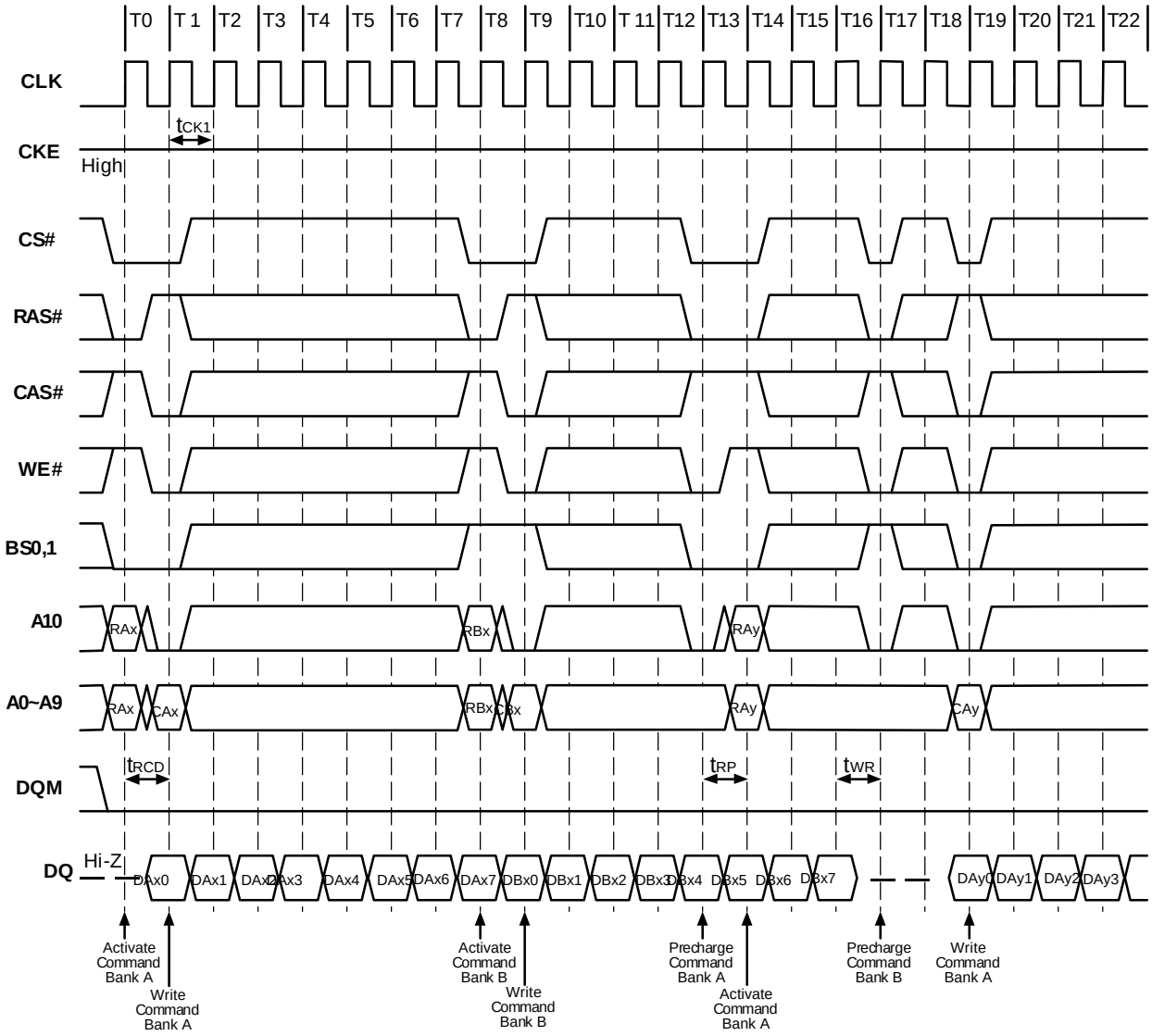
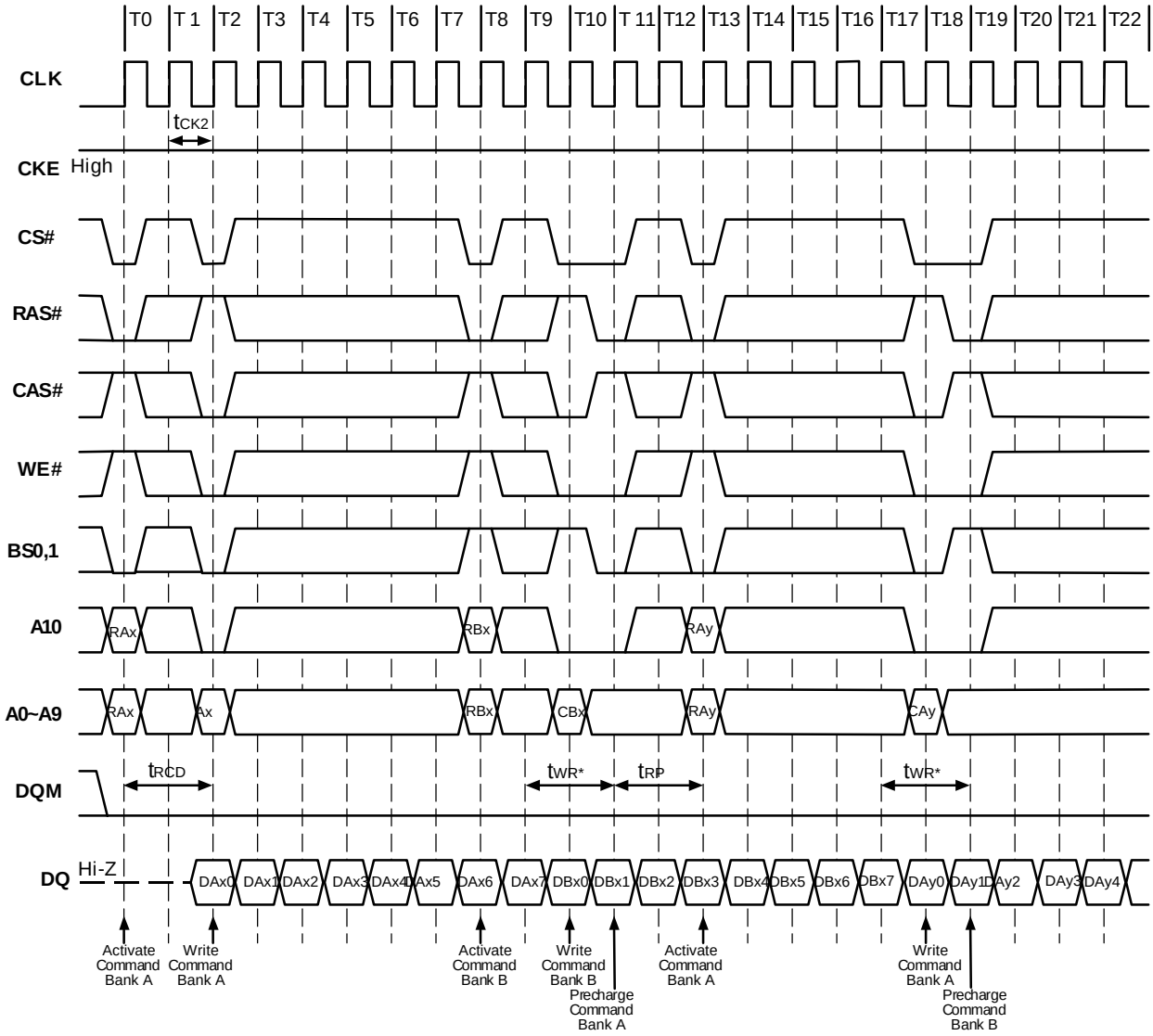
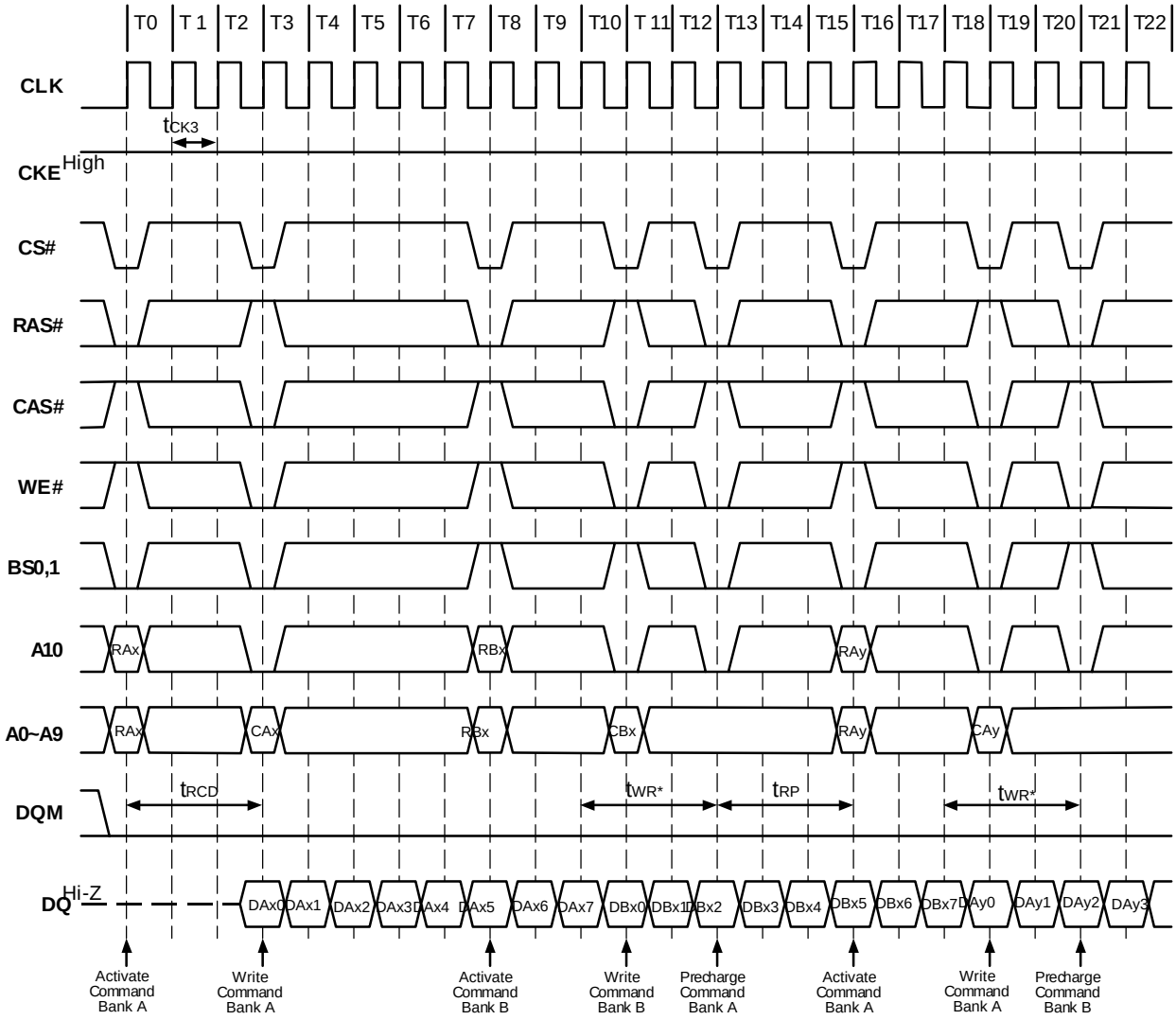


Figure 12.2. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=2)



***** tWR > tWR(min.)

Figure 12.3. Random Row Write (Interleaving Banks)
(Burst Length=8, CAS# Latency=3)



***** tWR > tWR(min.)

Figure 13.1. Read and Write Cycle (Burst Length=4, CAS# Latency=1)

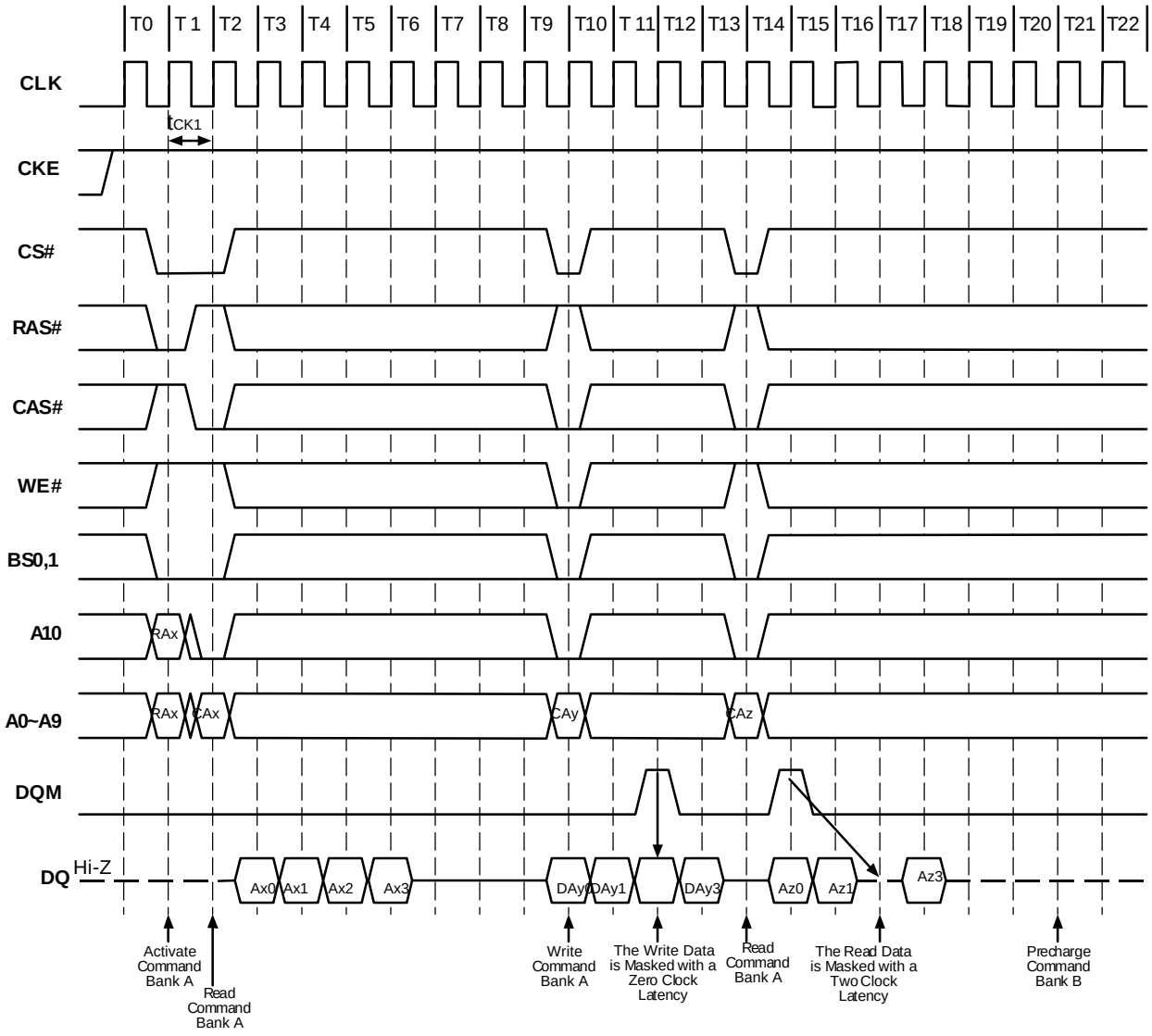


Figure 13.2. Read and Write Cycle (Burst Length=4, CAS# Latency=2)

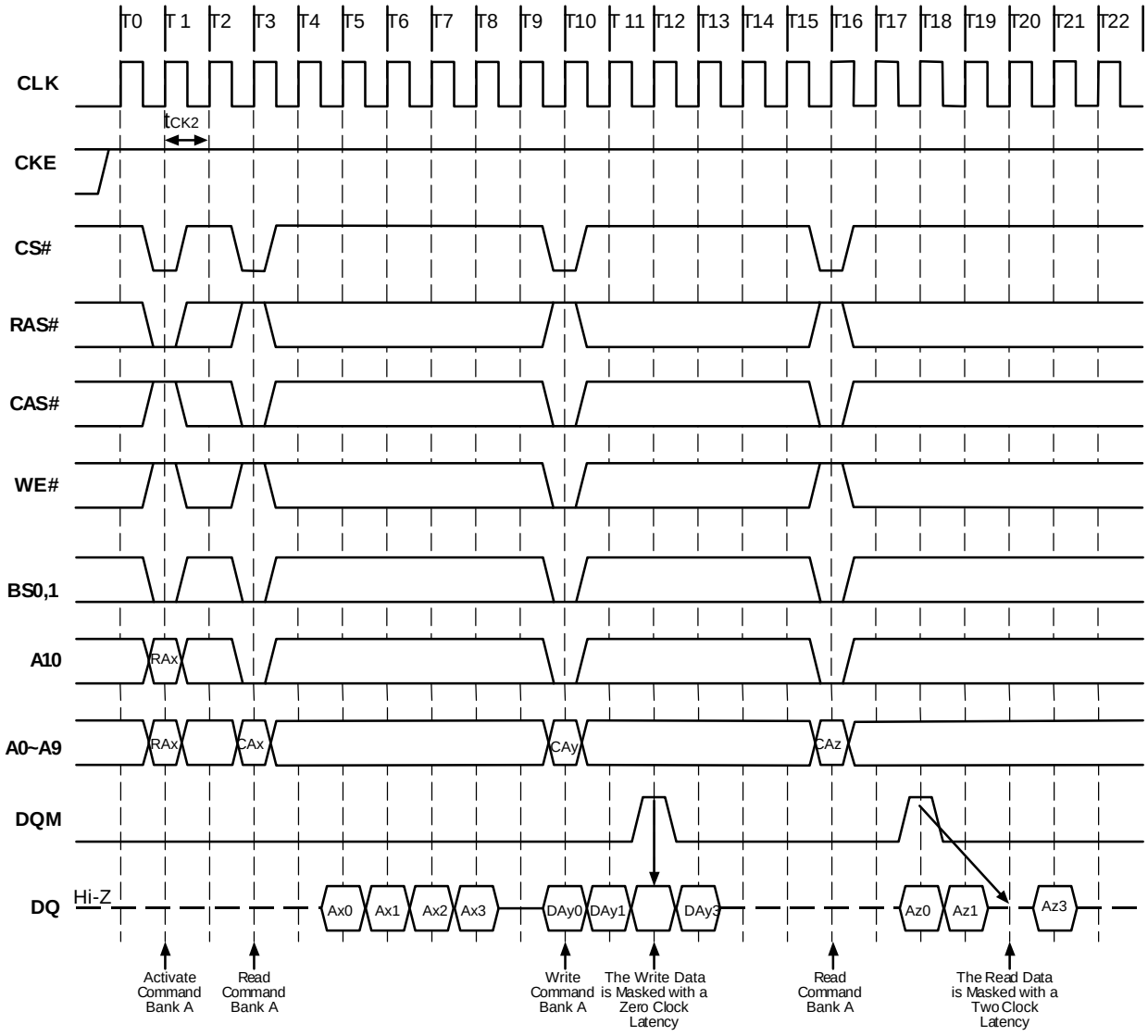


Figure 13.3. Read and Write Cycle (Burst Length=4, CAS# Latency=3)

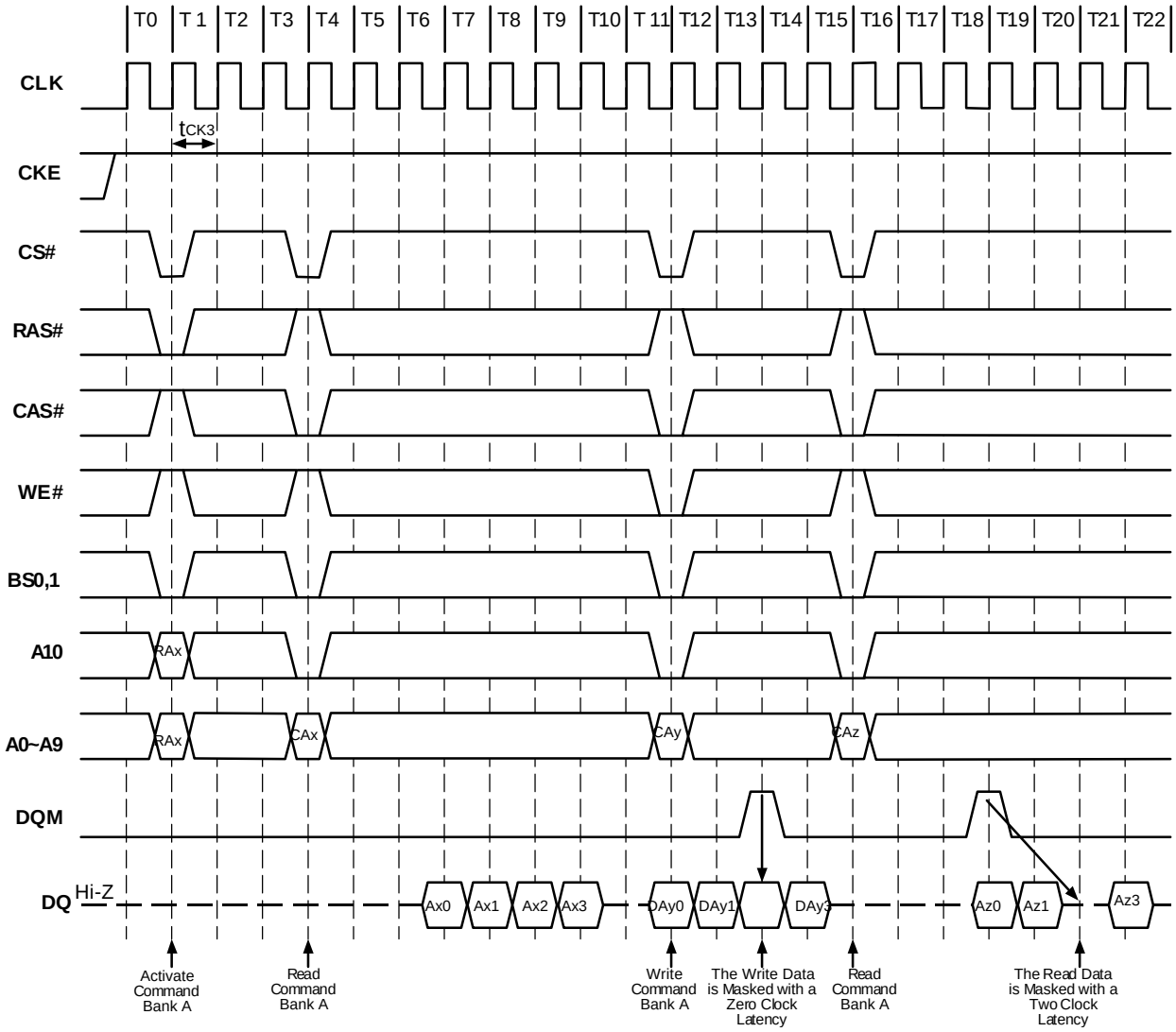


Figure 14.1. Interleaving Column Read Cycle (Burst Length=4, CAS# Latency=1)

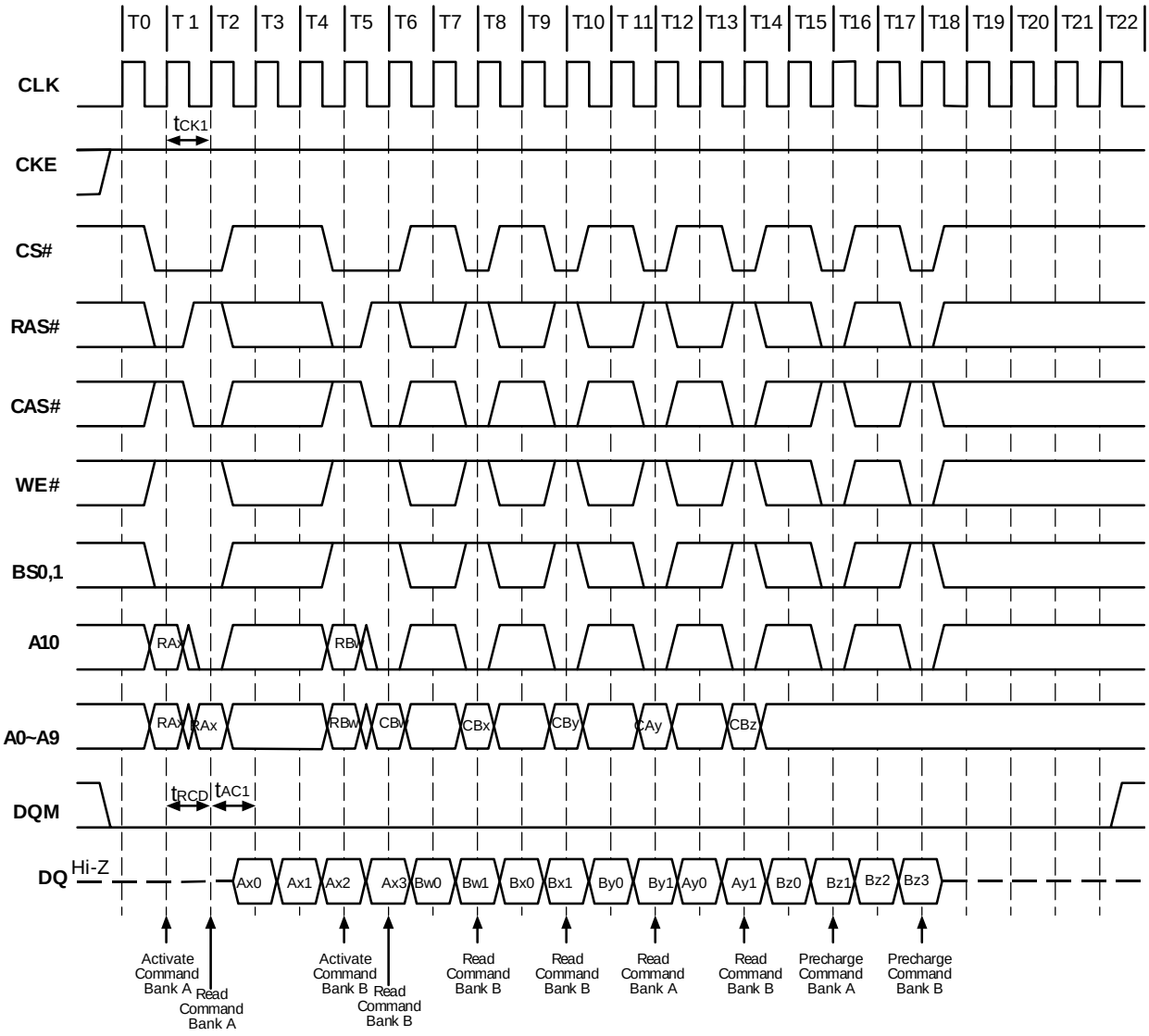


Figure 14.2. Interleaving Column Read Cycle (Burst Length=4, CAS# Latency=2)

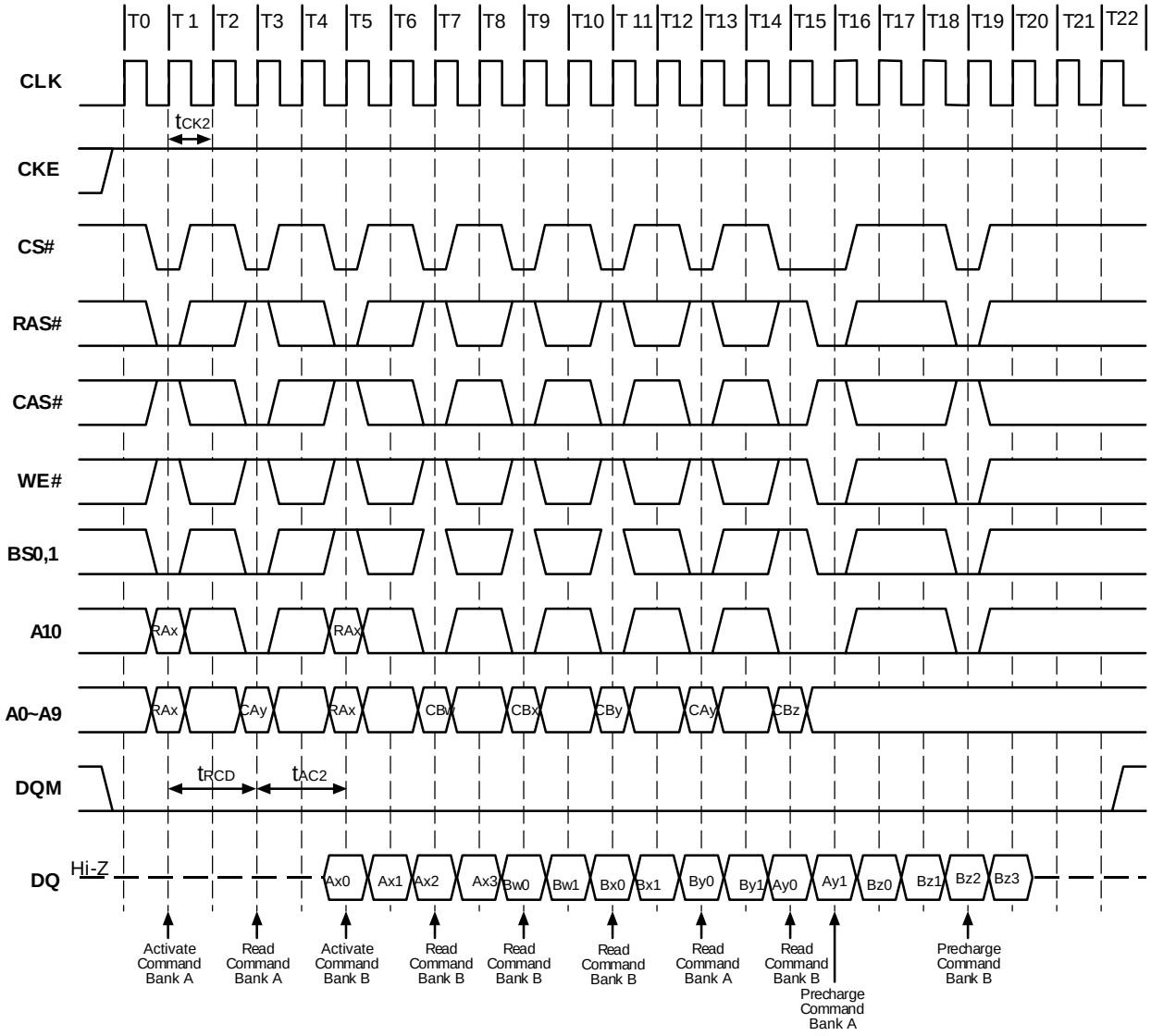


Figure 14.3. Interleaved Column Read Cycle (Burst Length=4, CAS# Latency=3)

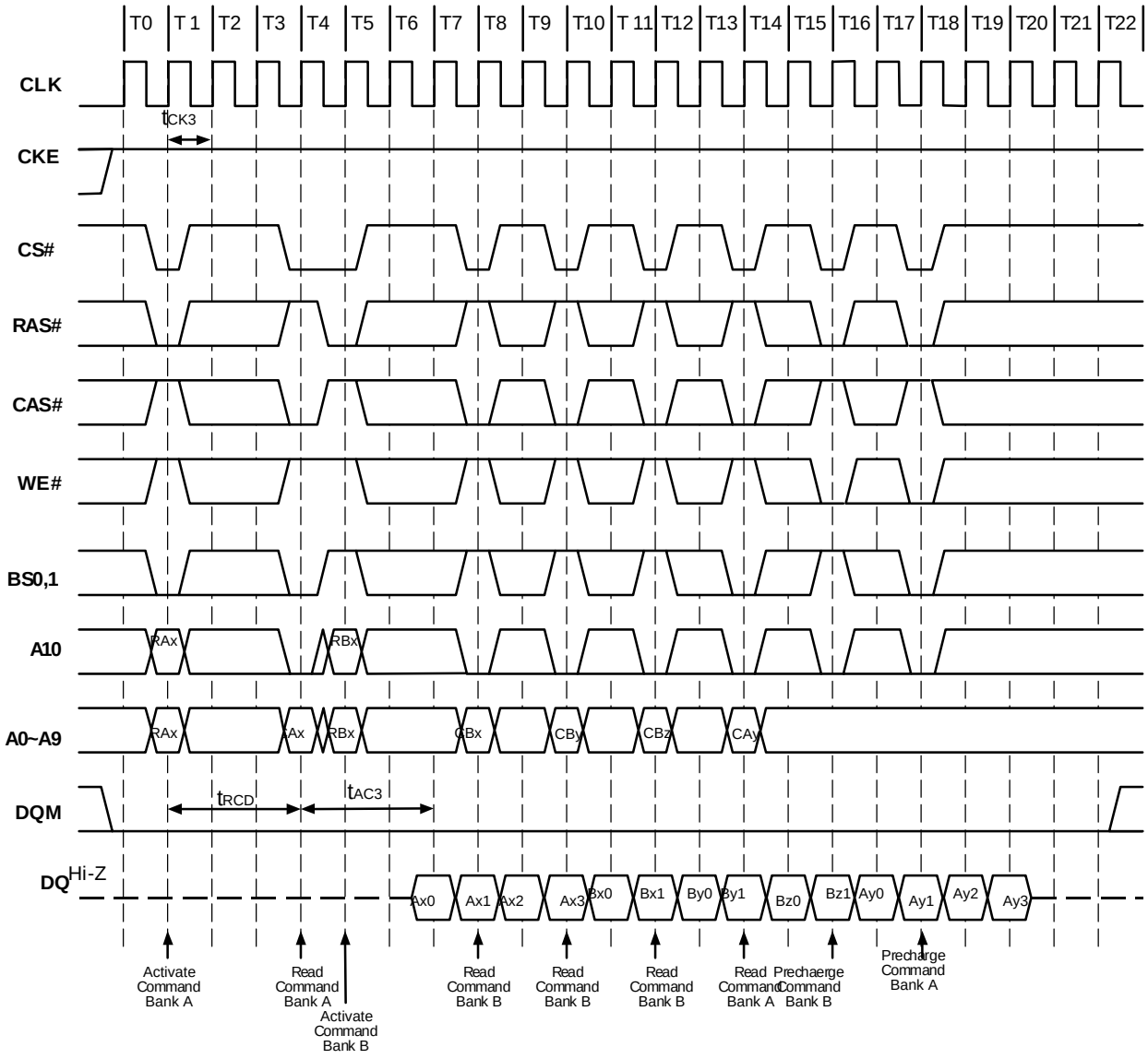


Figure 15.1. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=1)

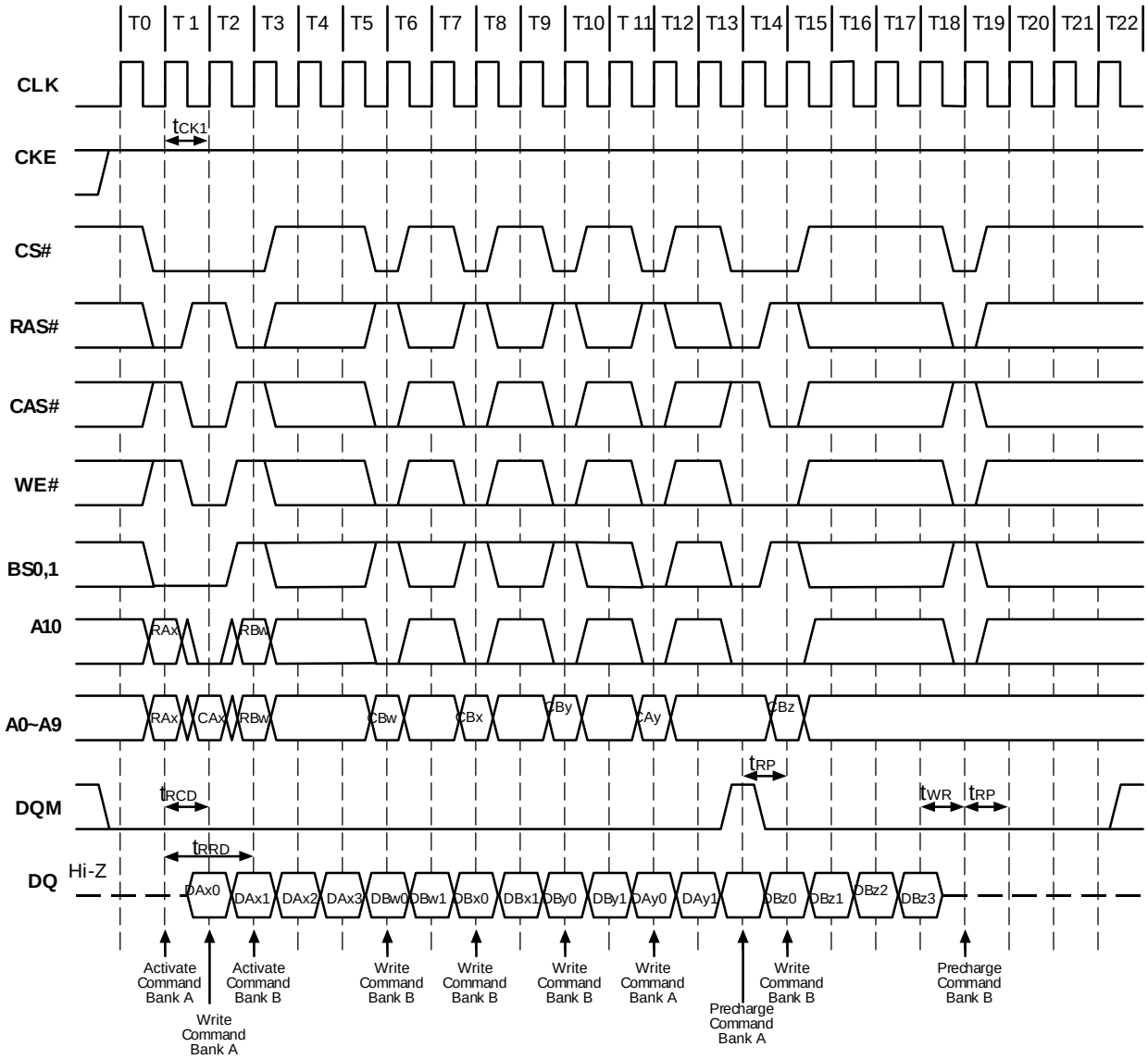


Figure 15.2. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=2)

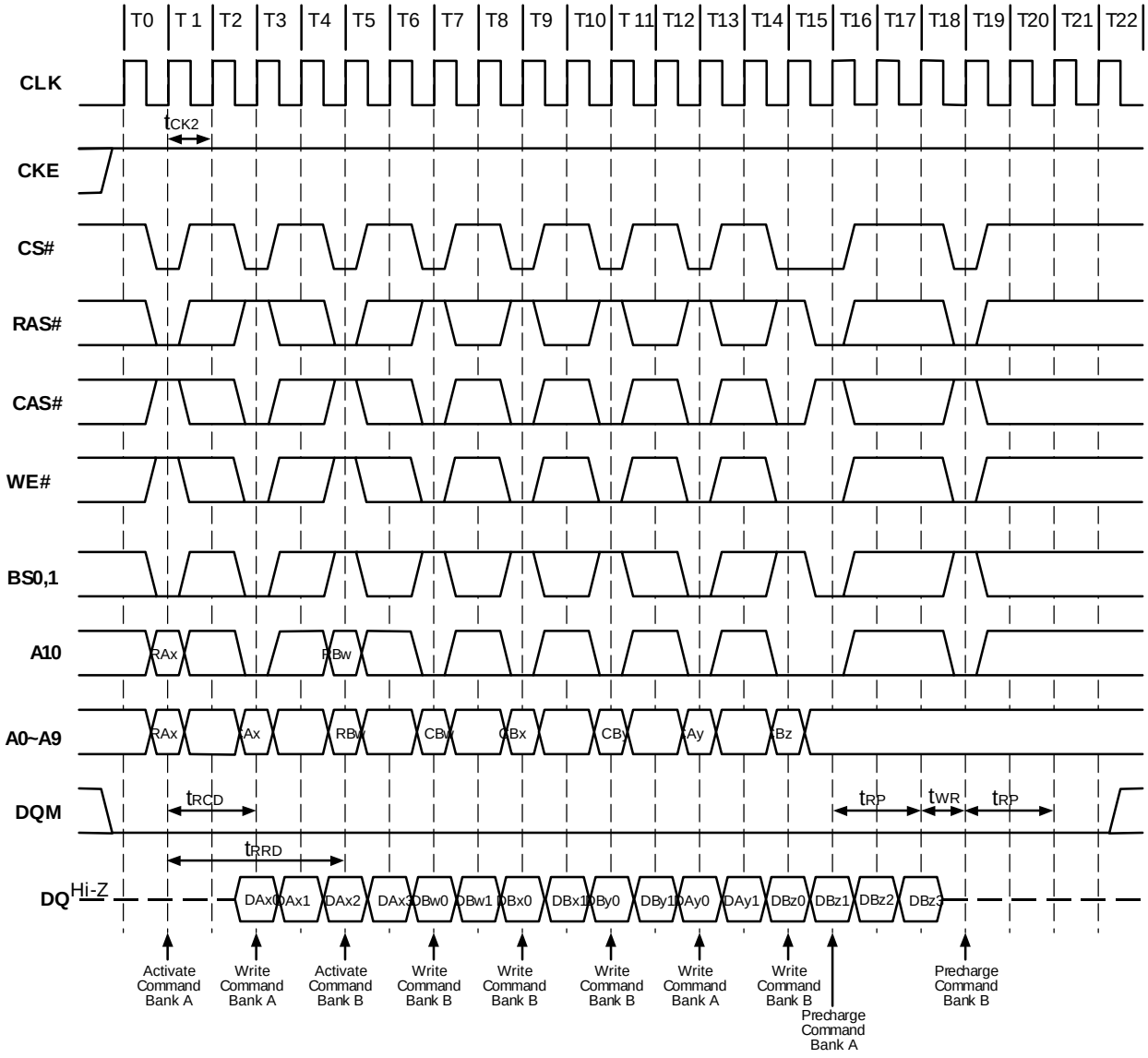


Figure 15.3. Interleaved Column Write Cycle (Burst Length=4, CAS# Latency=3)

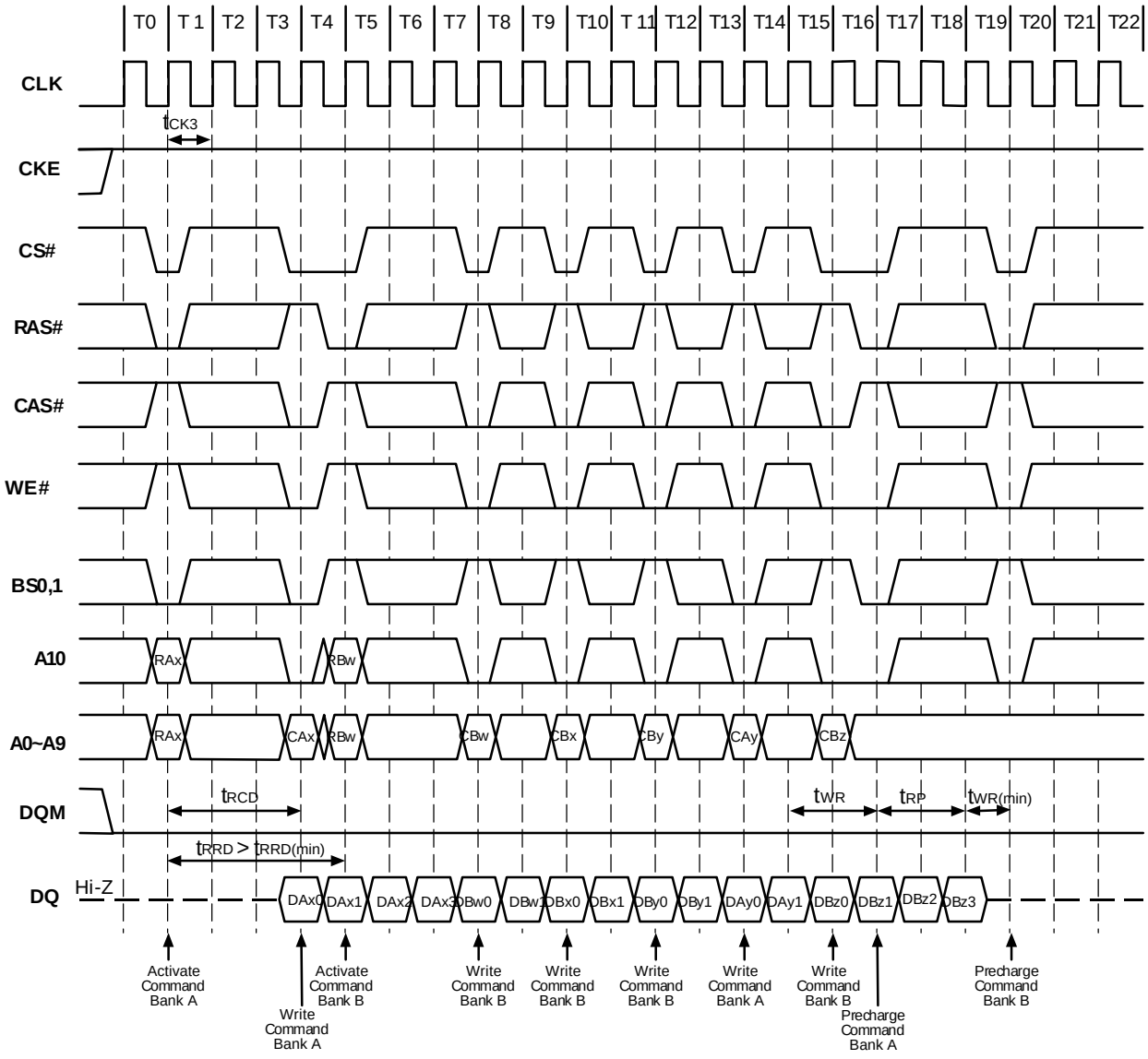


Figure 16.1. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=1)

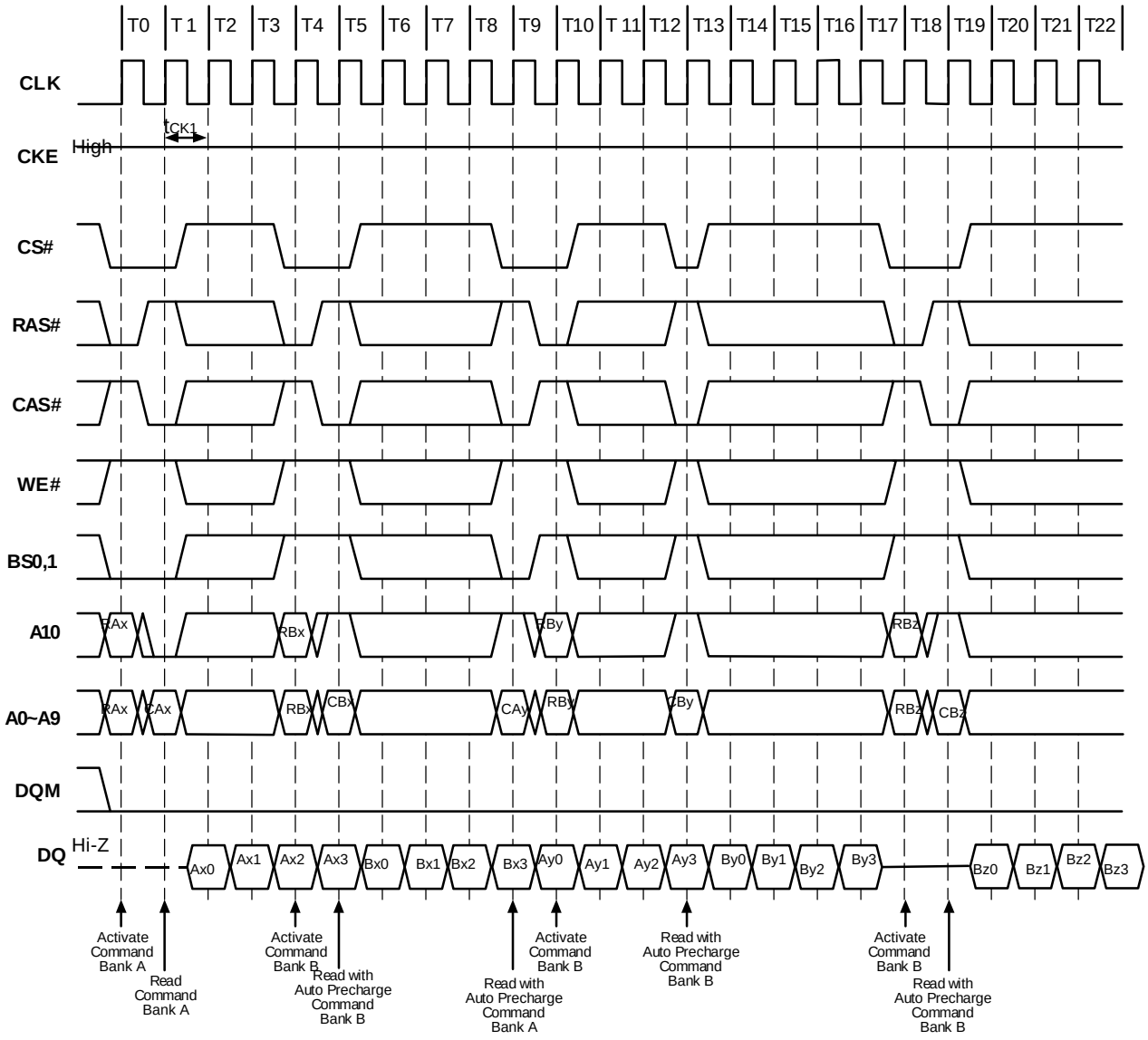


Figure 16.2. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=2)

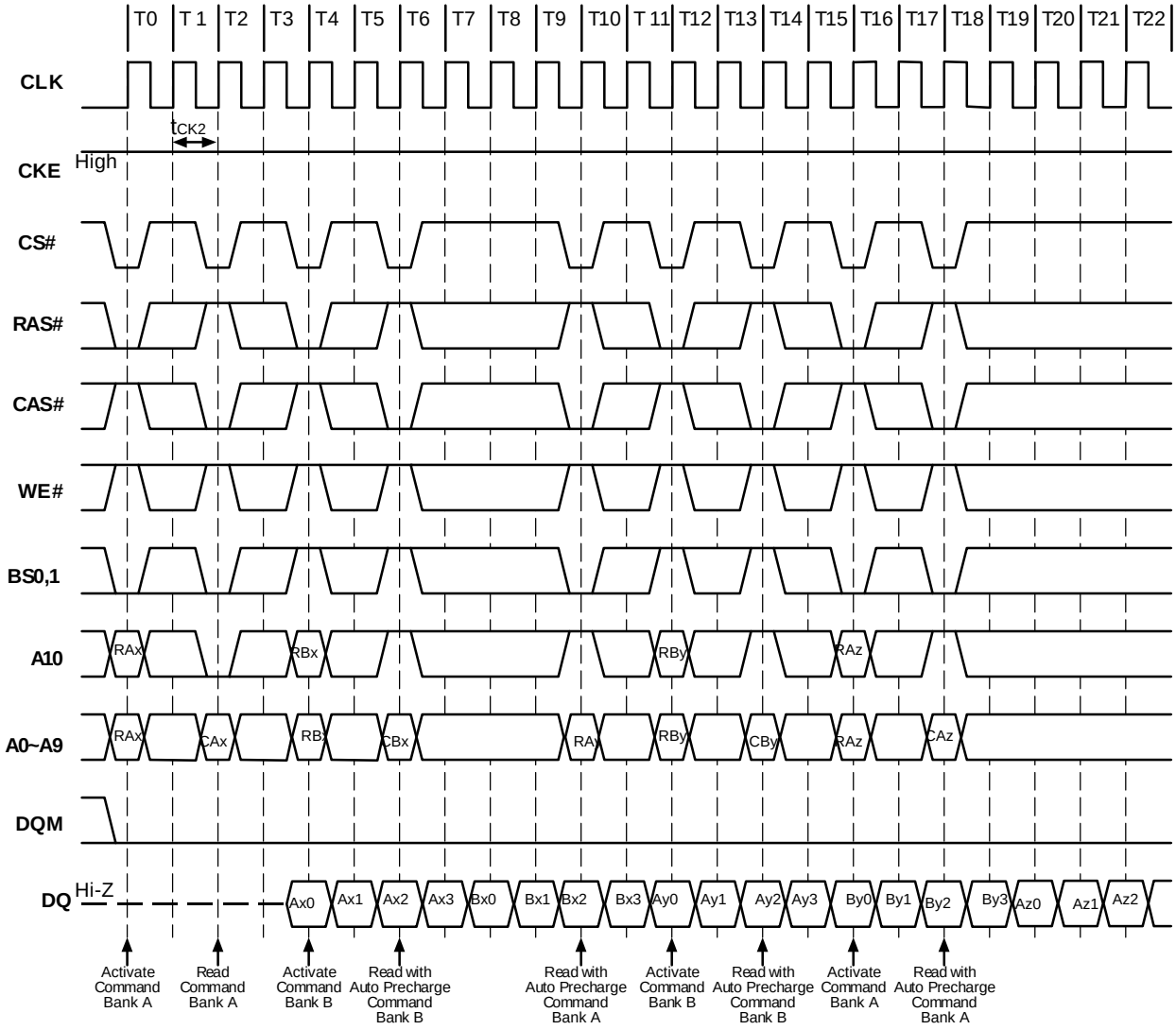


Figure 16.3. Auto Precharge after Read Burst (Burst Length=4, CAS# Latency=3)

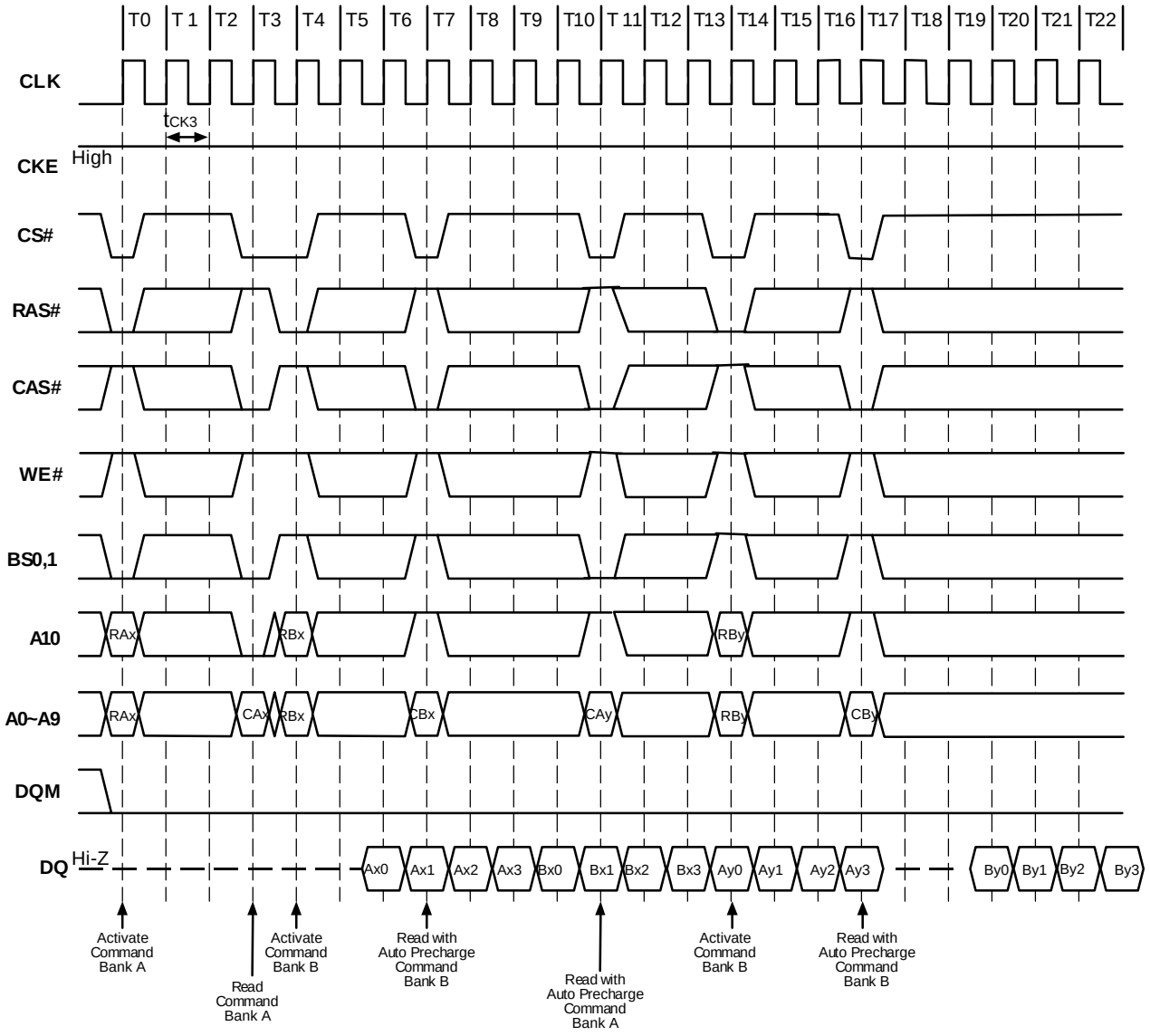


Figure 17.1. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=1)

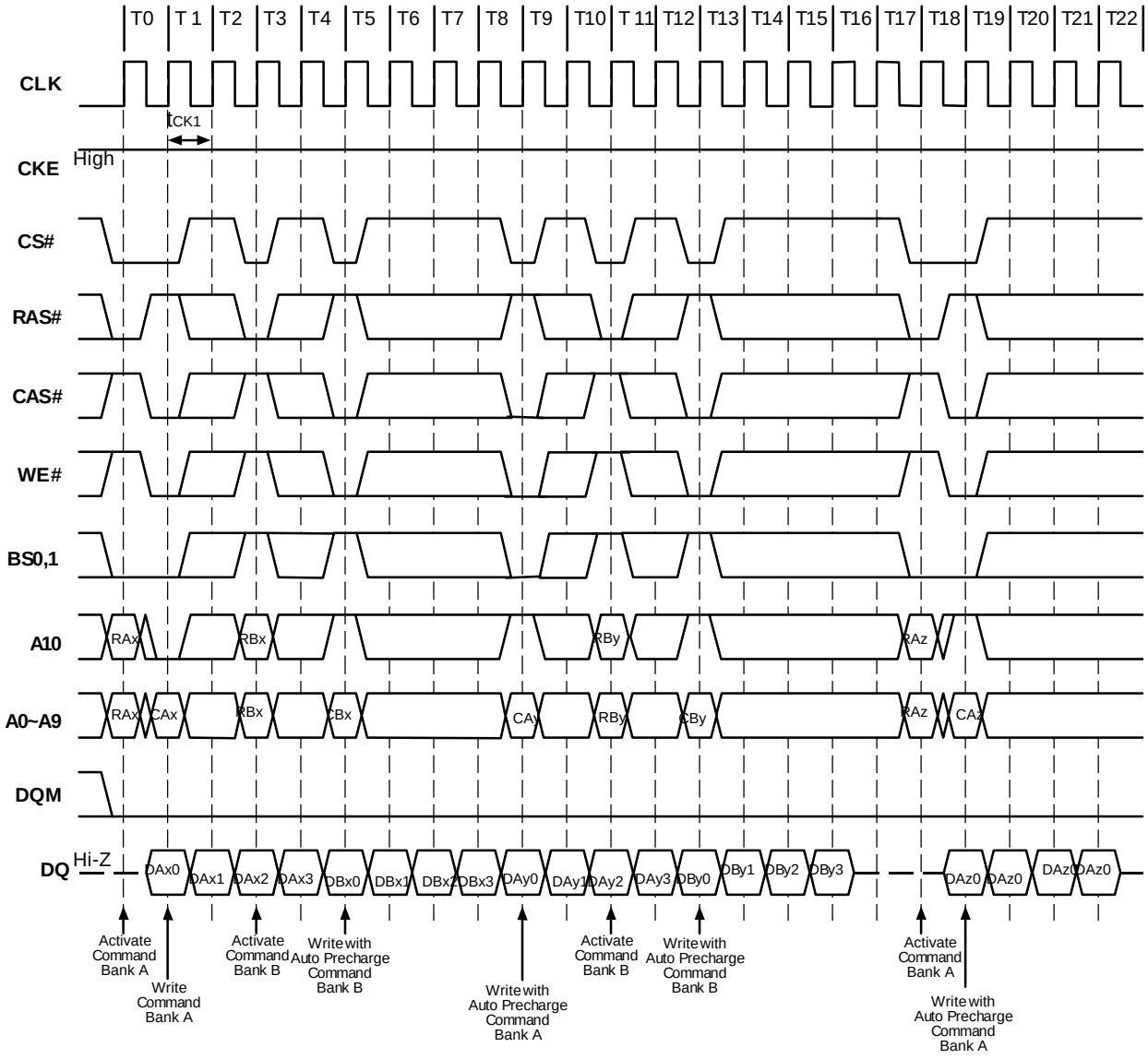


Figure 17.2. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=2)

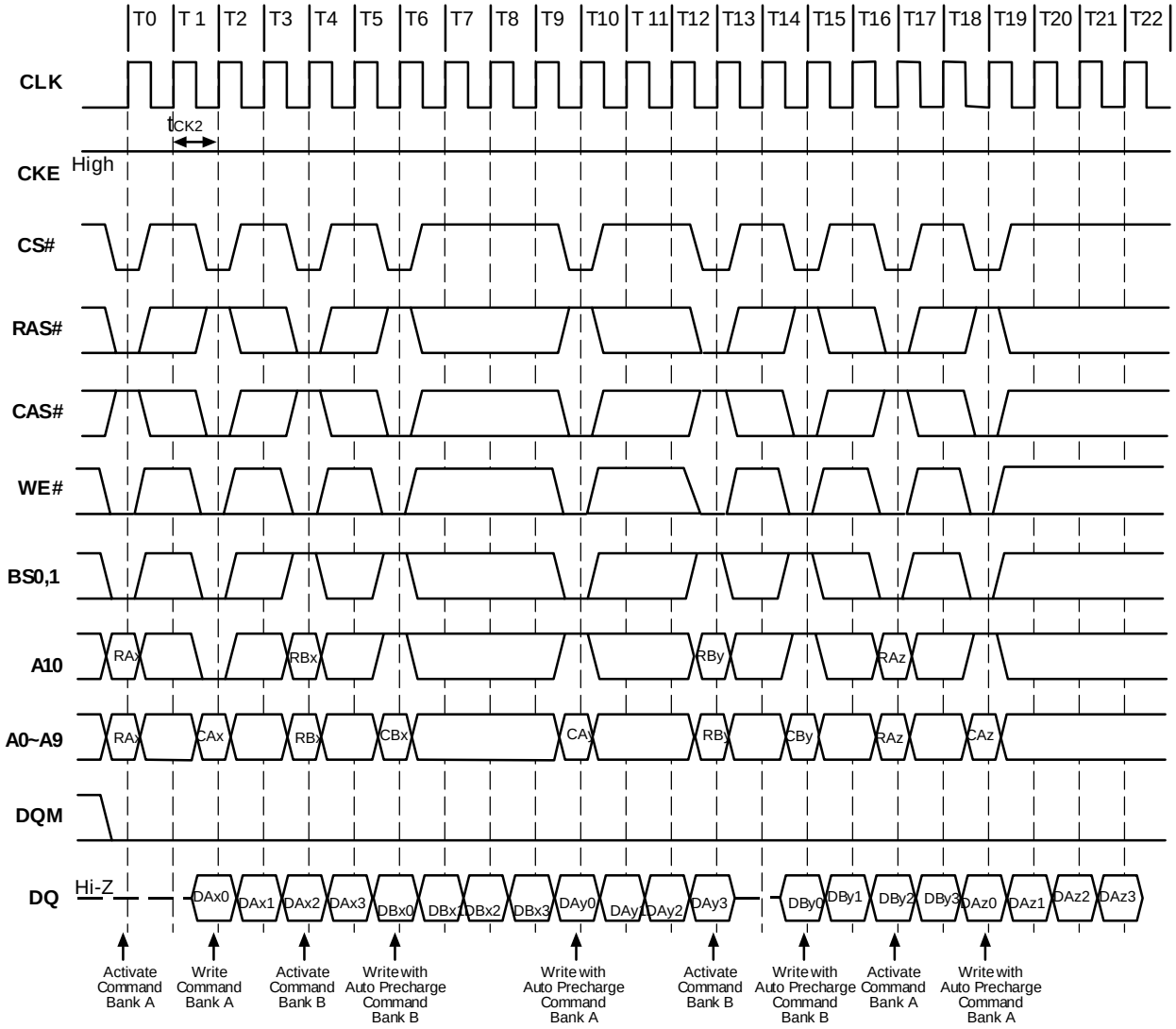


Figure 17.3. Auto Precharge after Write Burst (Burst Length=4, CAS# Latency=3)

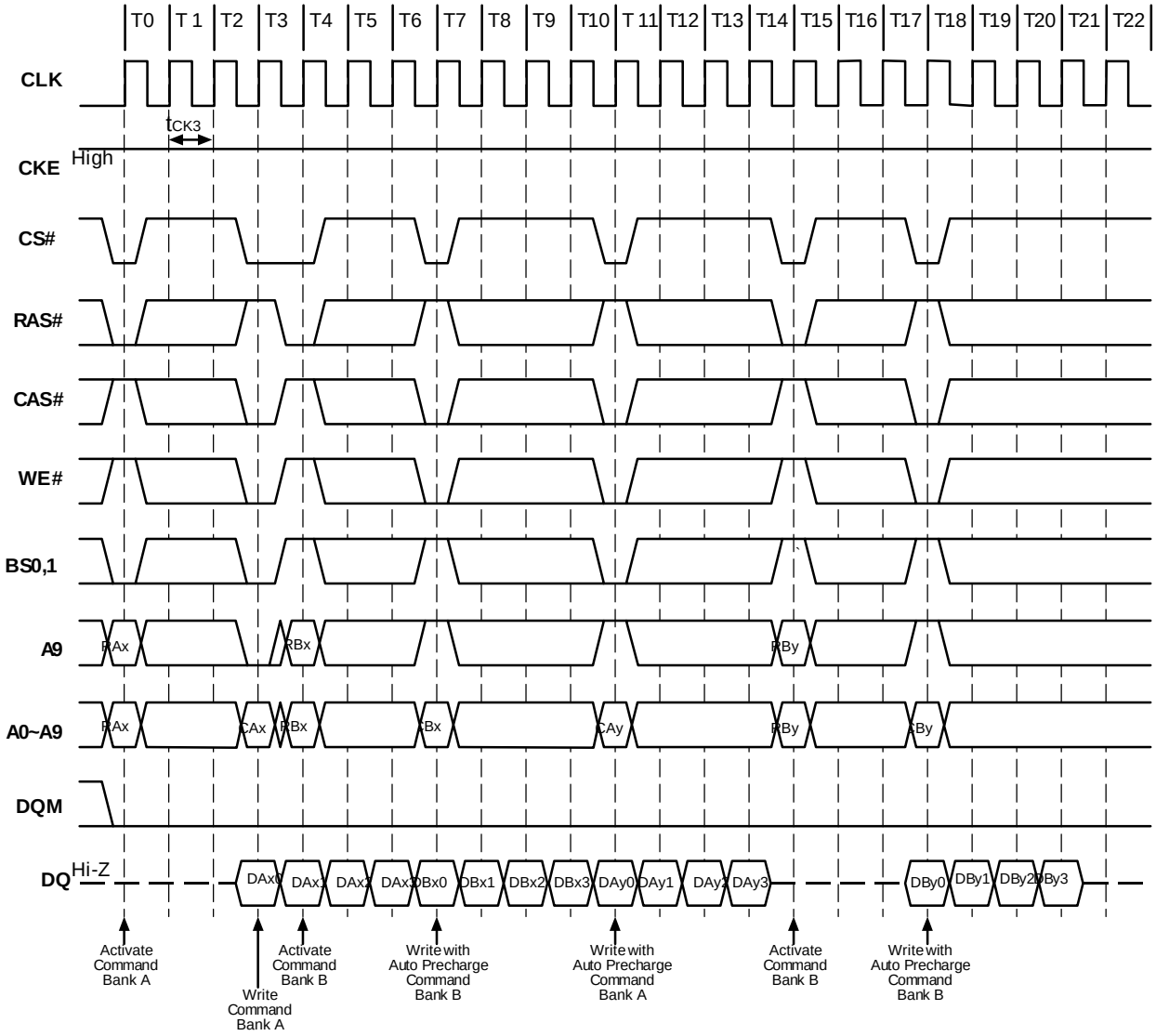


Figure 18.1. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=1)

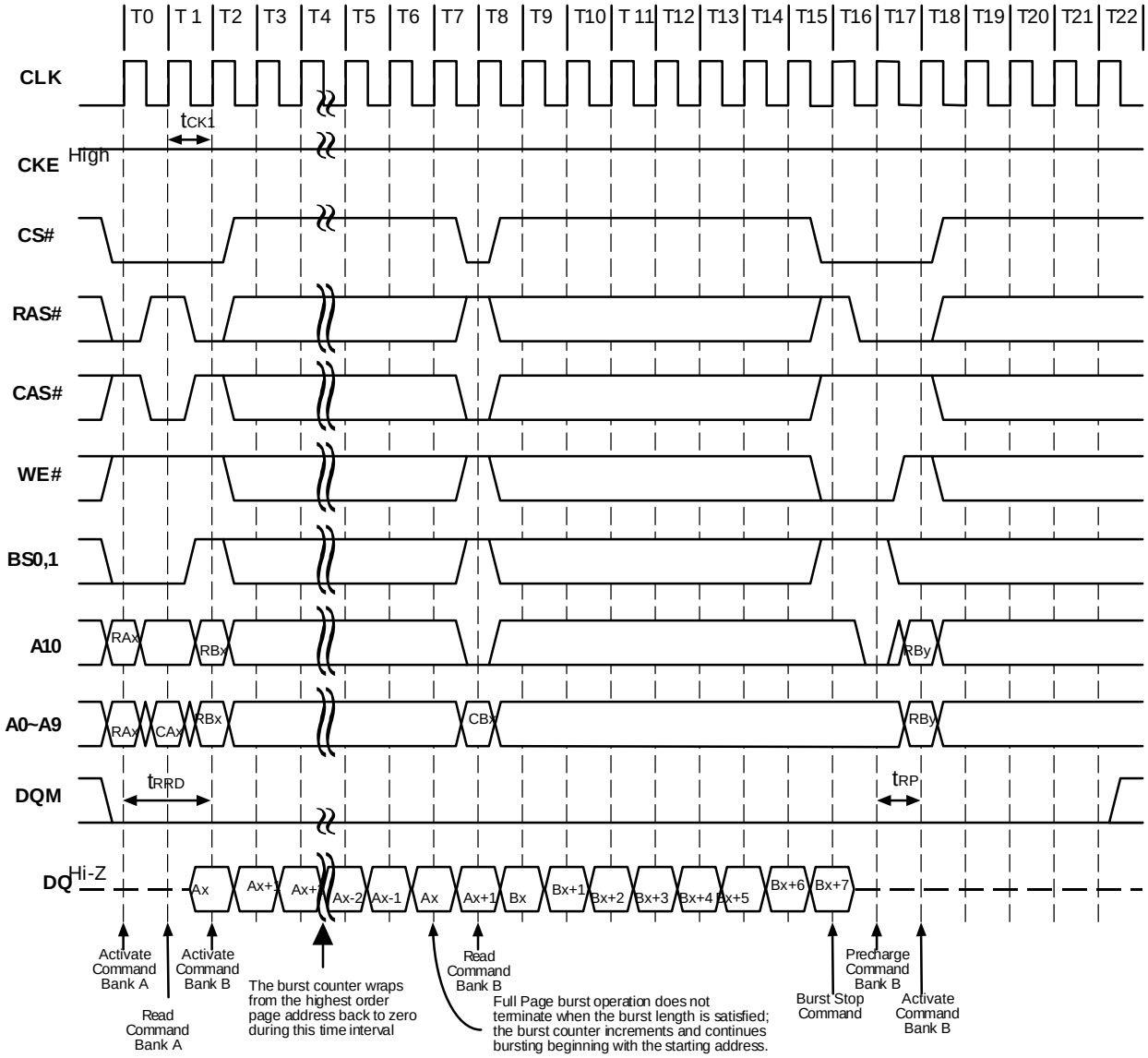


Figure 18.2. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=2)

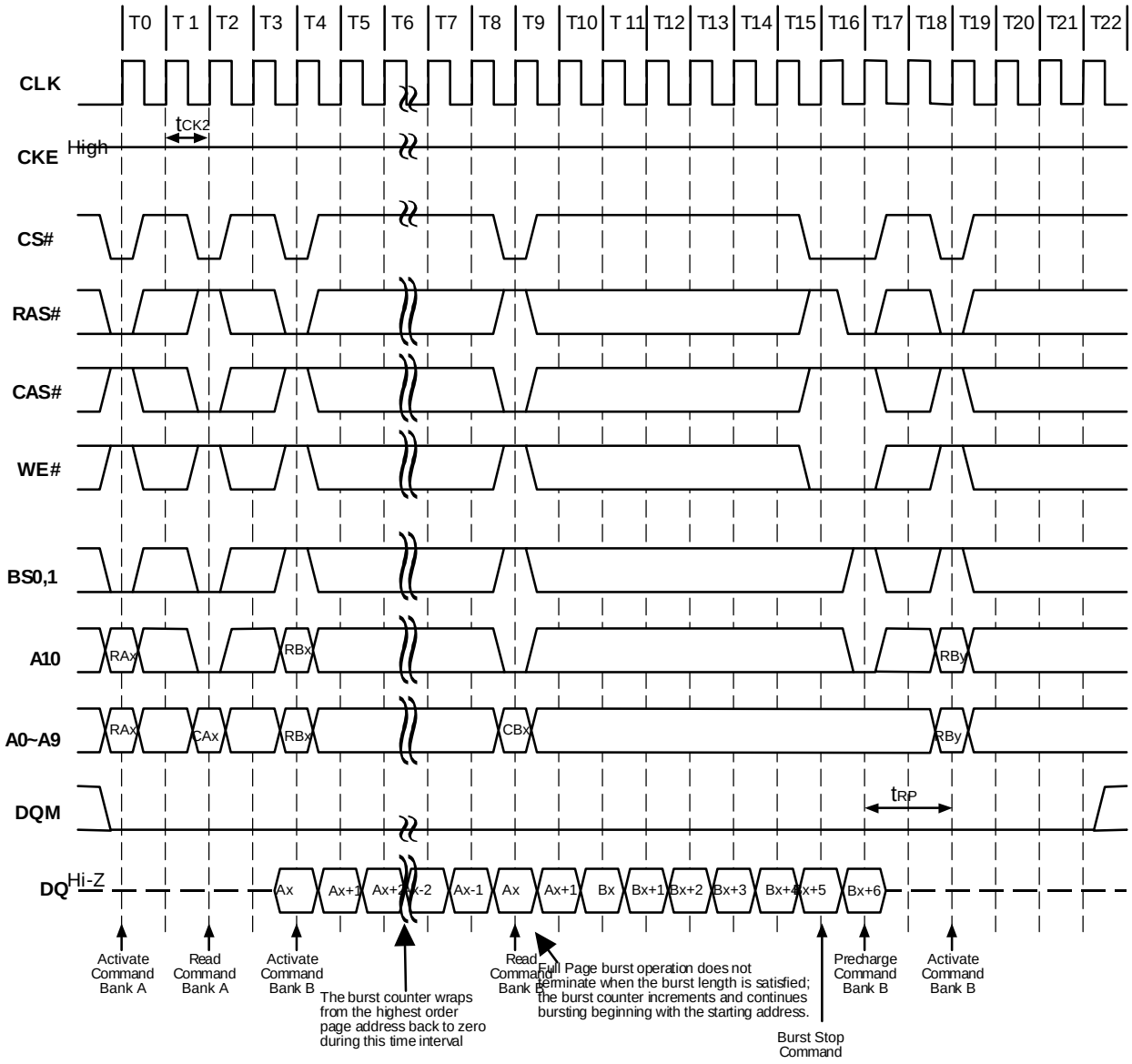


Figure 18.3. Full Page Read Cycle (Burst Length=Full Page, CAS# Latency=3)

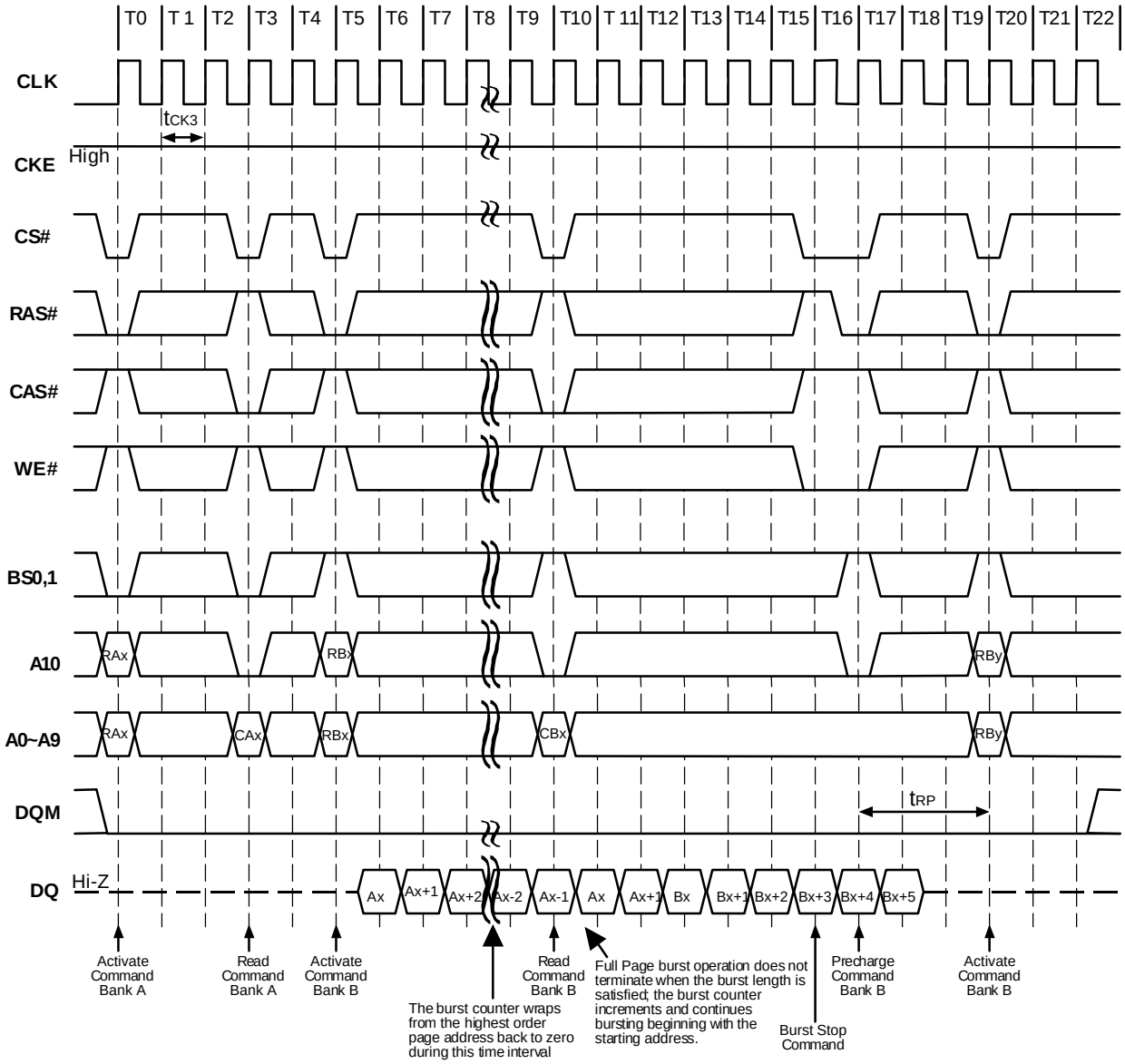


Figure 19.1. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=1)

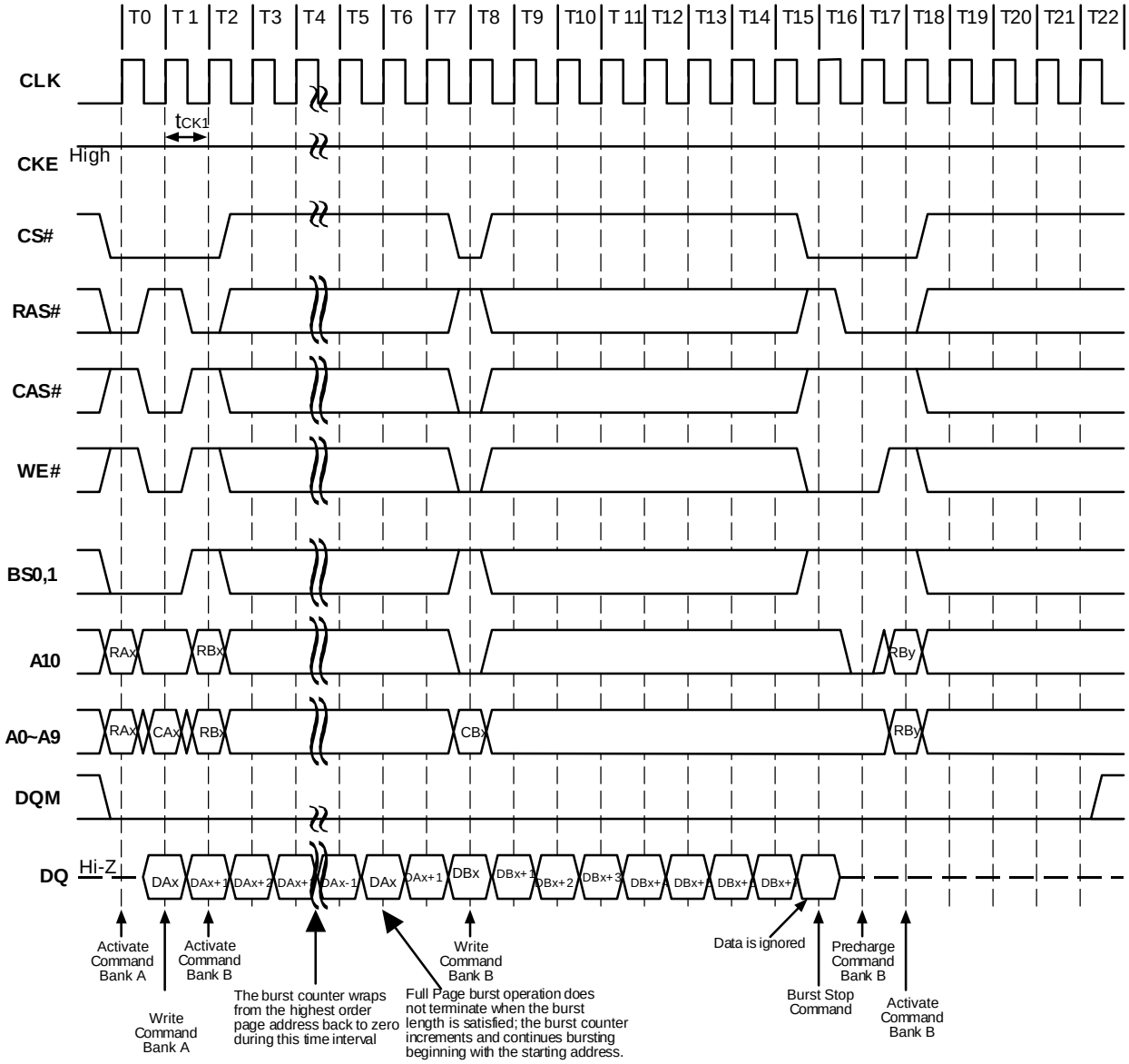


Figure 19.2. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=2)

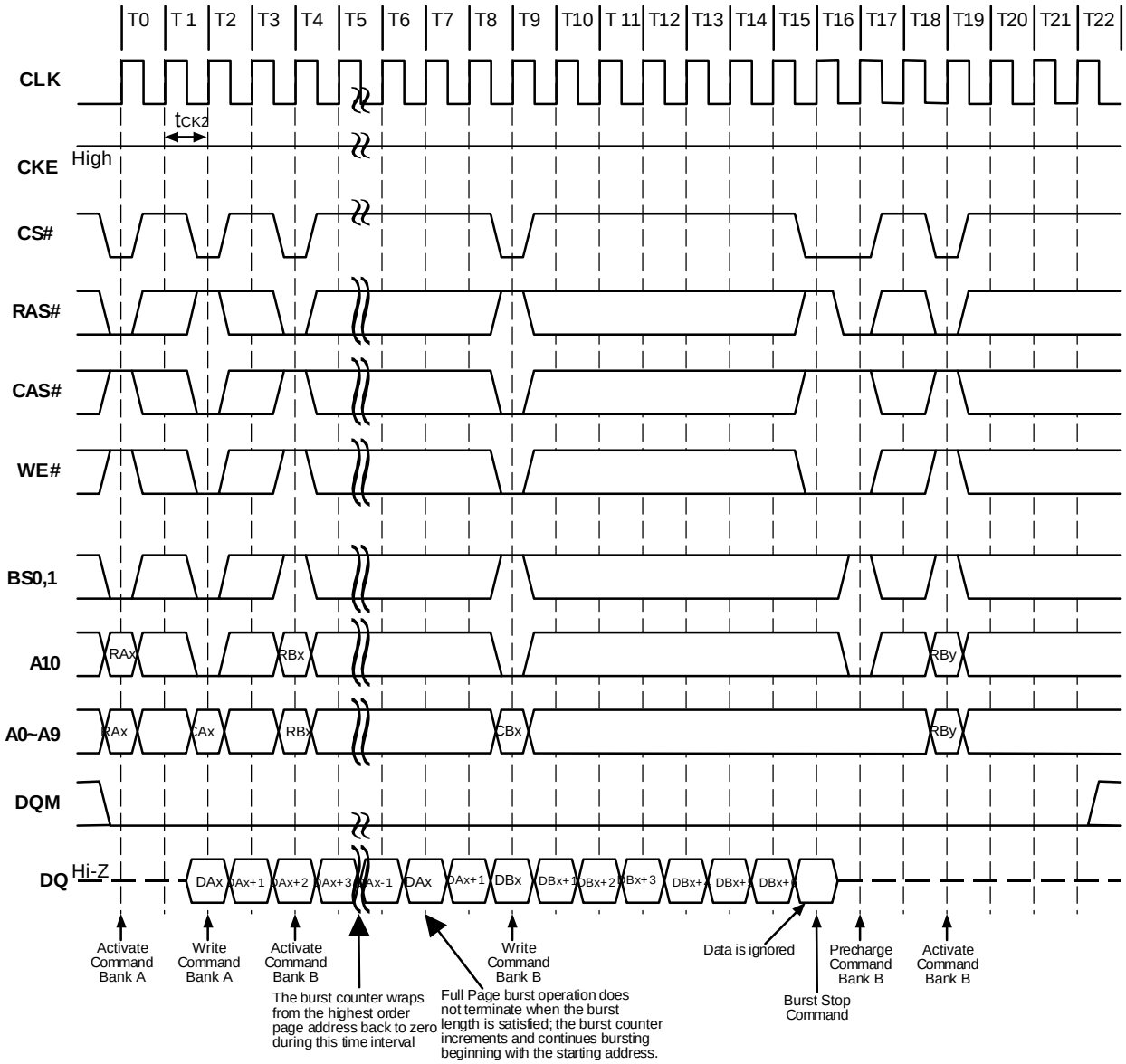


Figure 19.3. Full Page Write Cycle (Burst Length=Full Page, CAS# Latency=3)

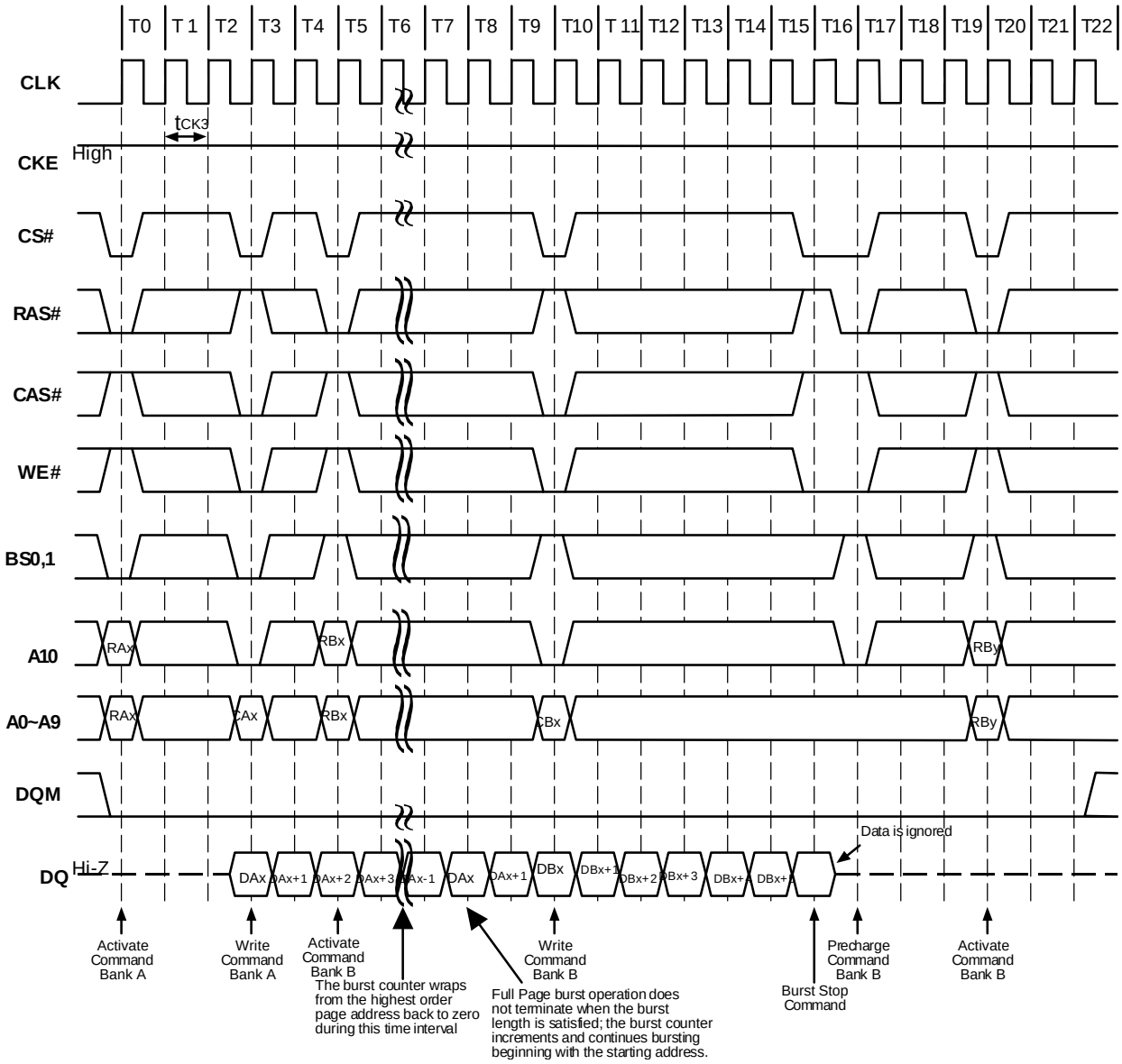


Figure 20. Byte Write Operation (Burst Length=4, CAS# Latency=2)

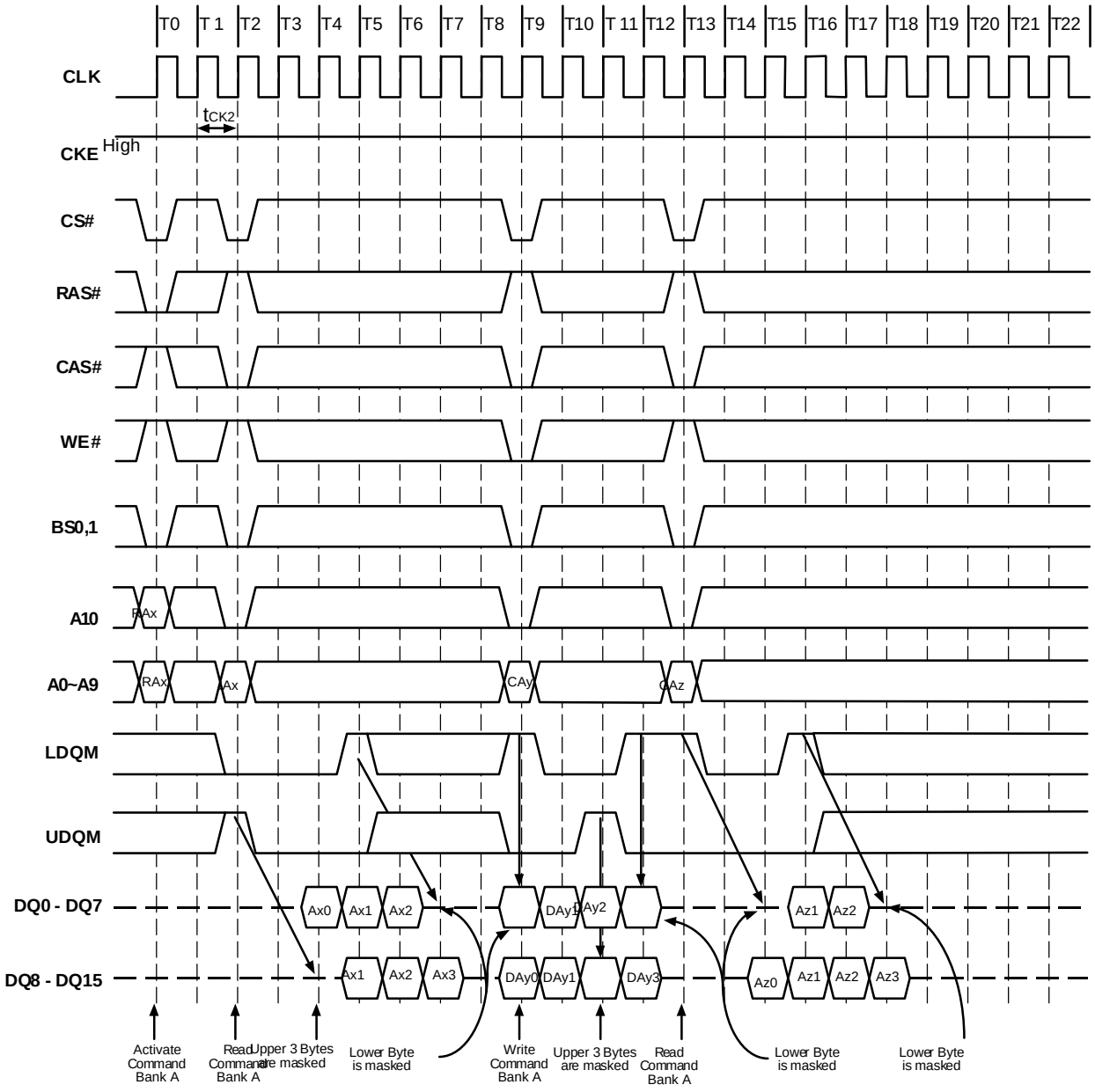


Figure 21. Random Row Read (Interleaving Banks)

(Burst Length=2, CAS# Latency=1)

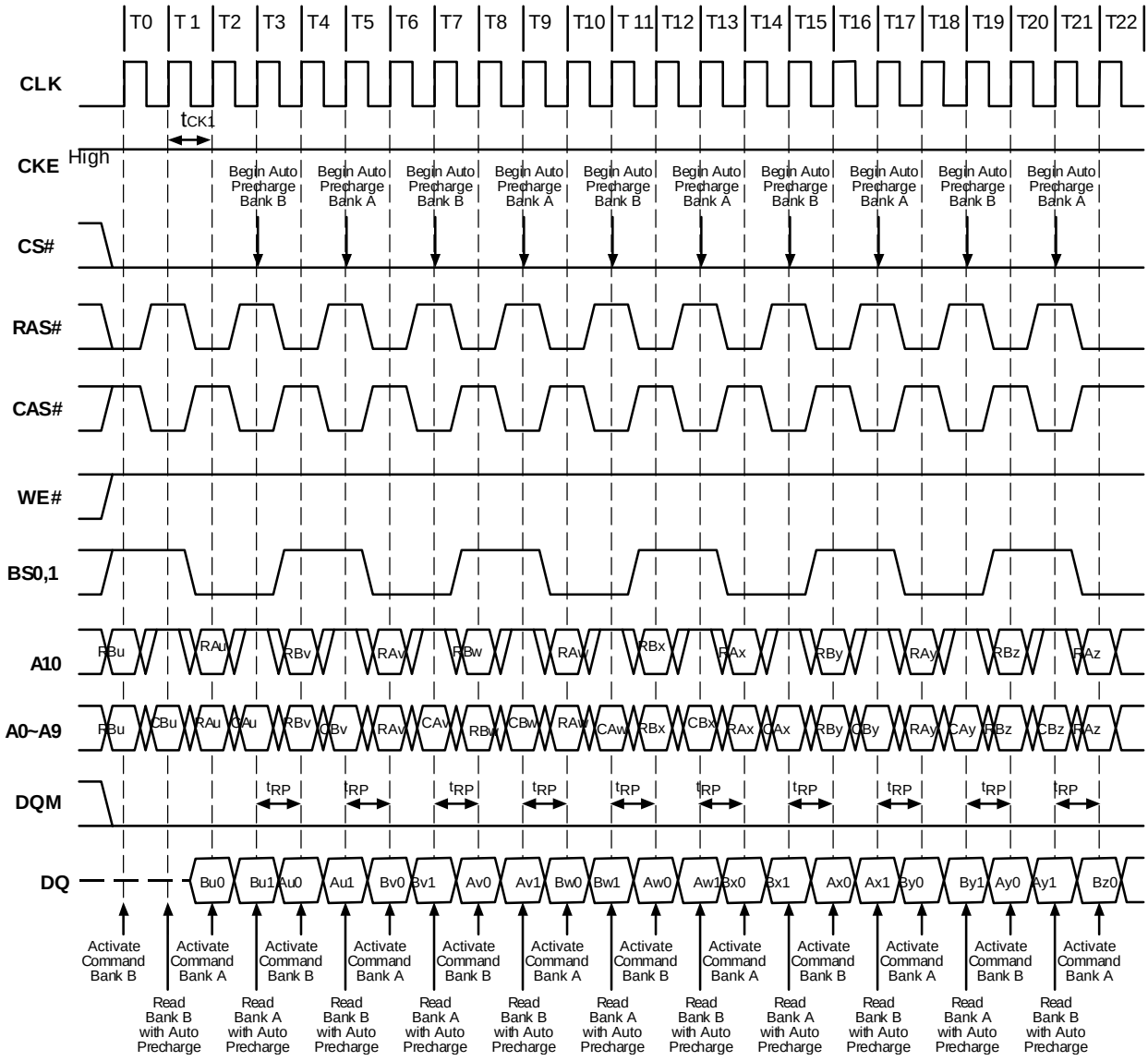


Figure 22. Full Page Random Column Read (Burst Length=Full Page, CAS# Latency=2)

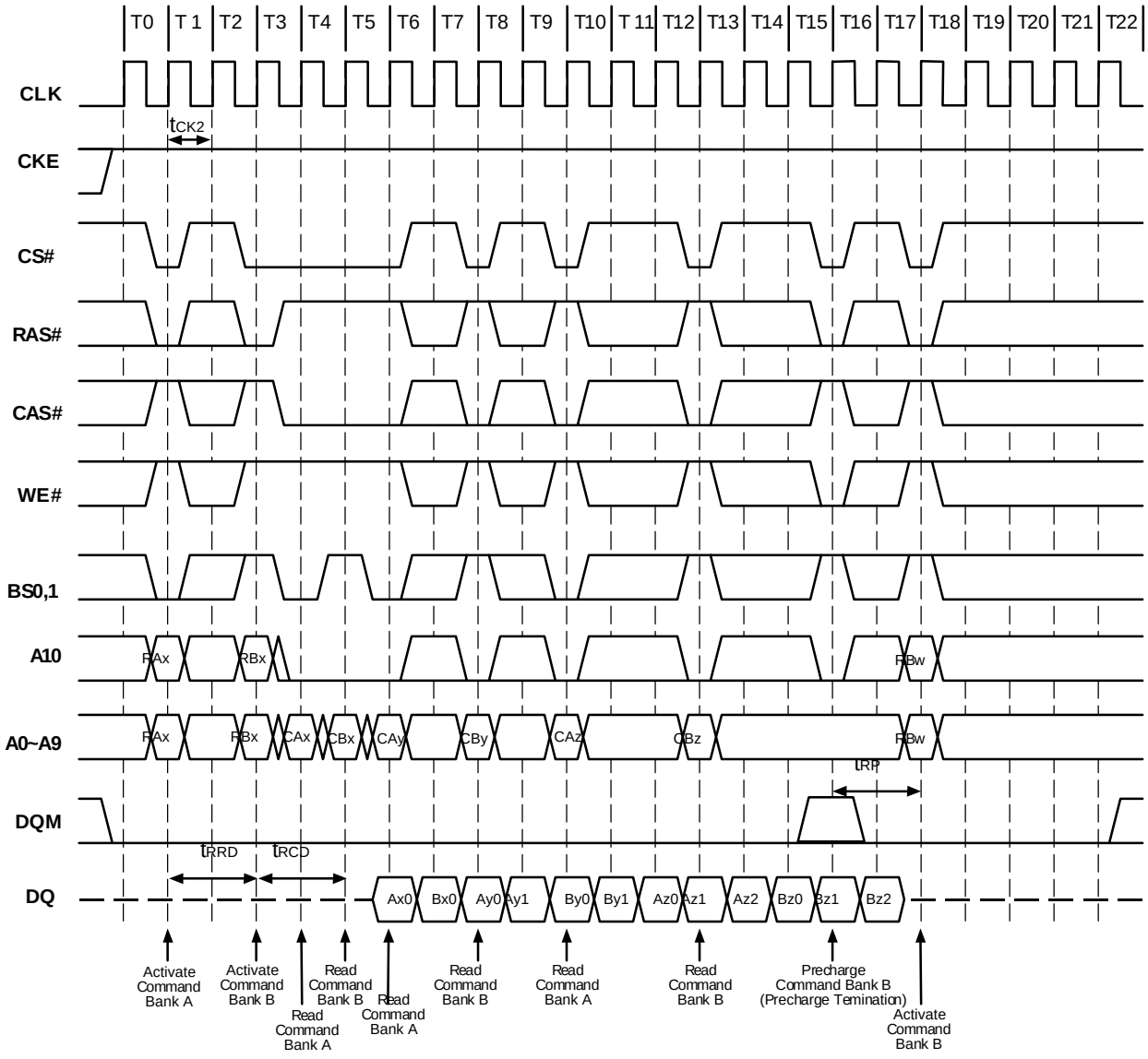


Figure 23. Full Page Random Column Write (Burst Length=Full Page, CAS# Latency=2)

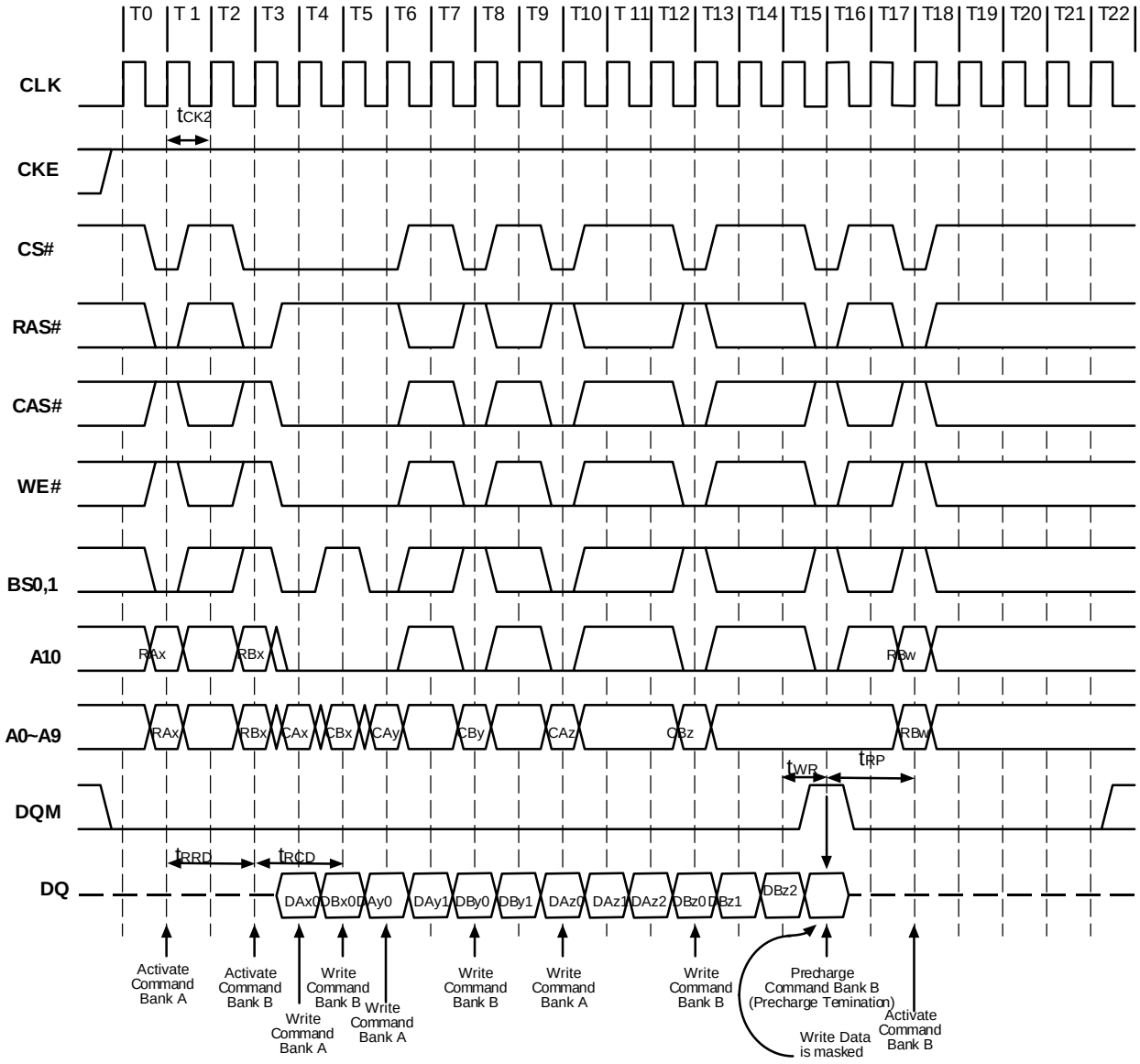


Figure 24.1. Precharge Termination of a Burst (Burst Length=Full Page, CAS# Latency=1)

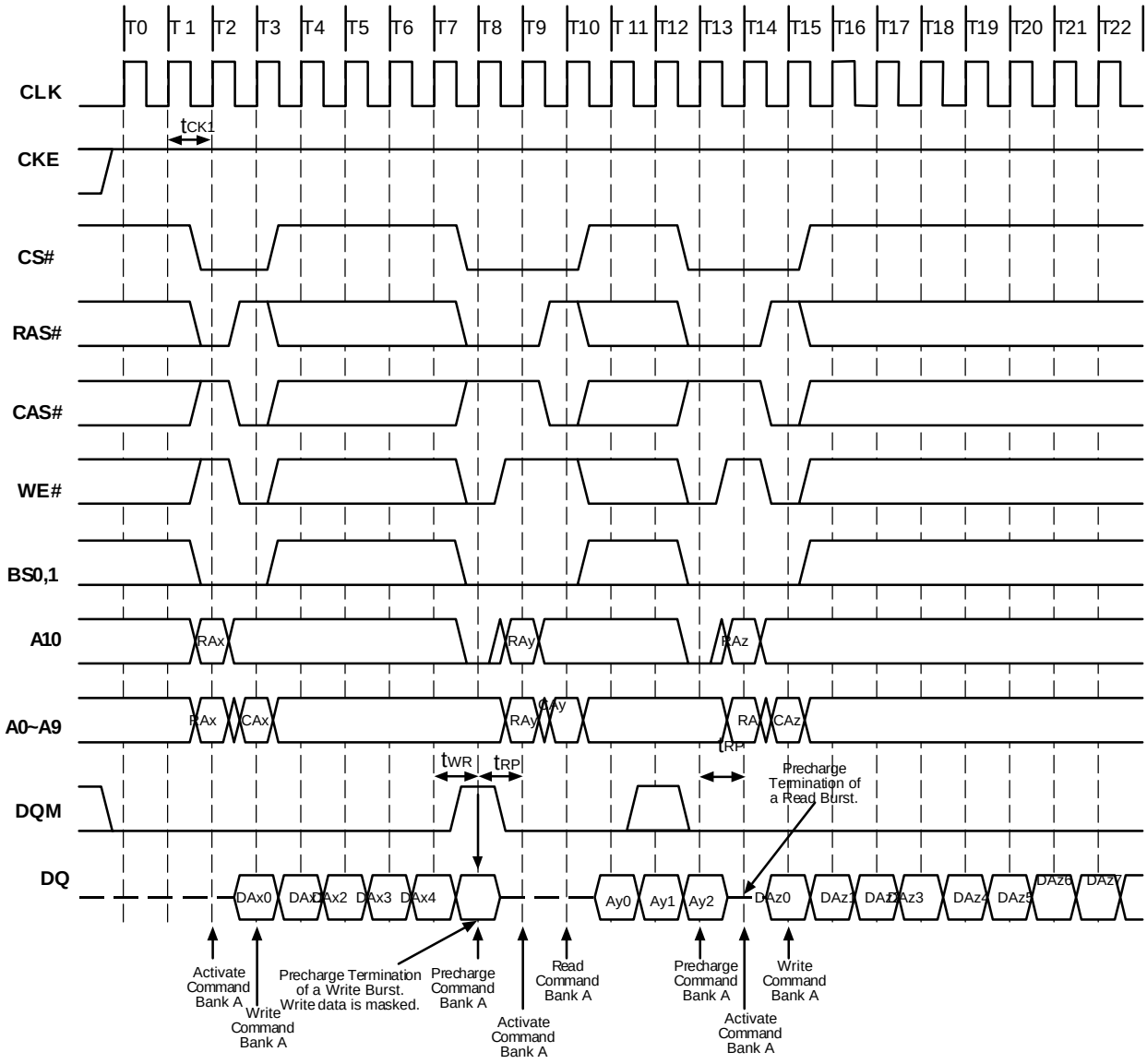


Figure 24.2. Precharge Termination of a Burst
(Burst Length=8 or Full Page, CAS# Latency=2)

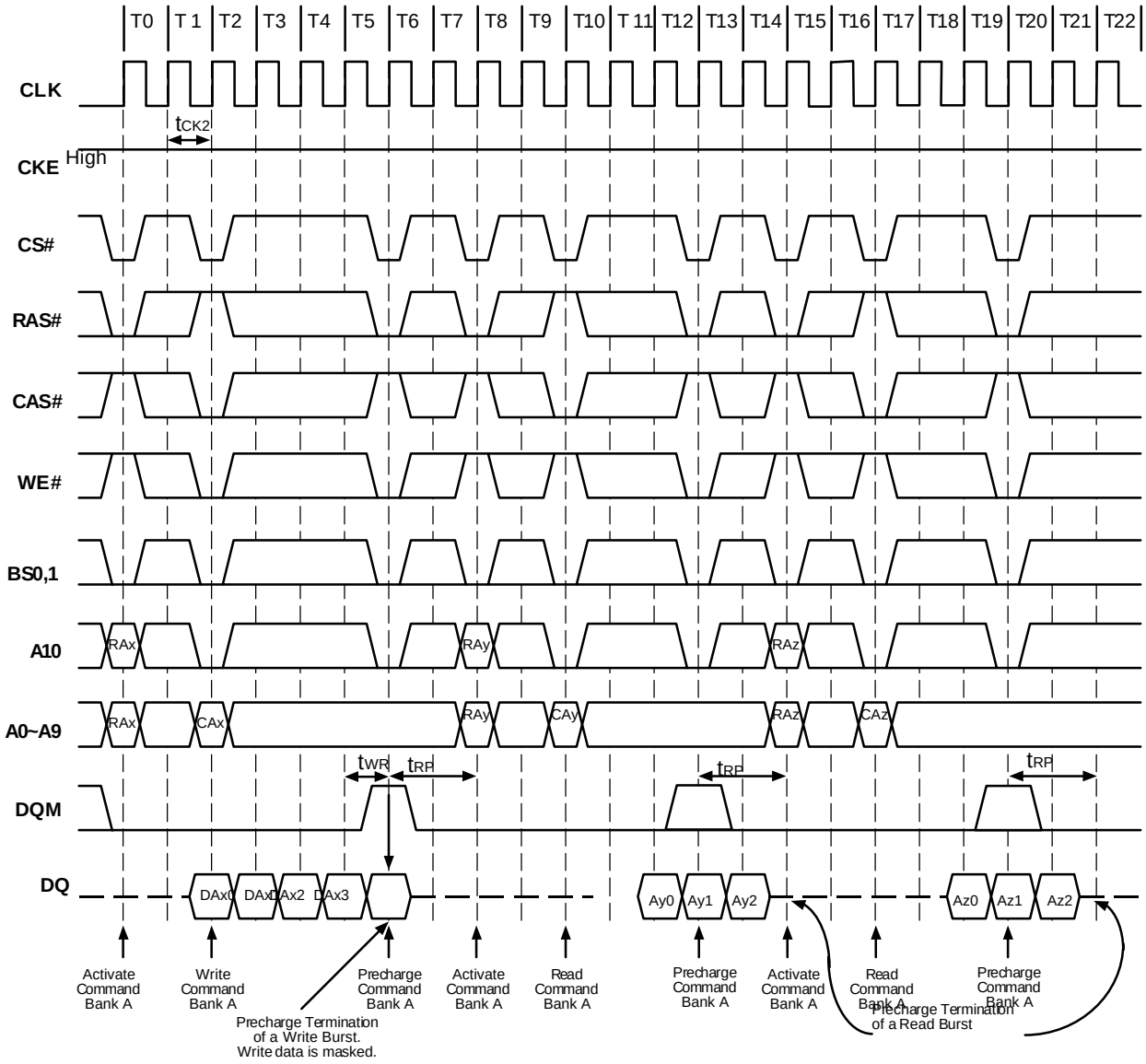
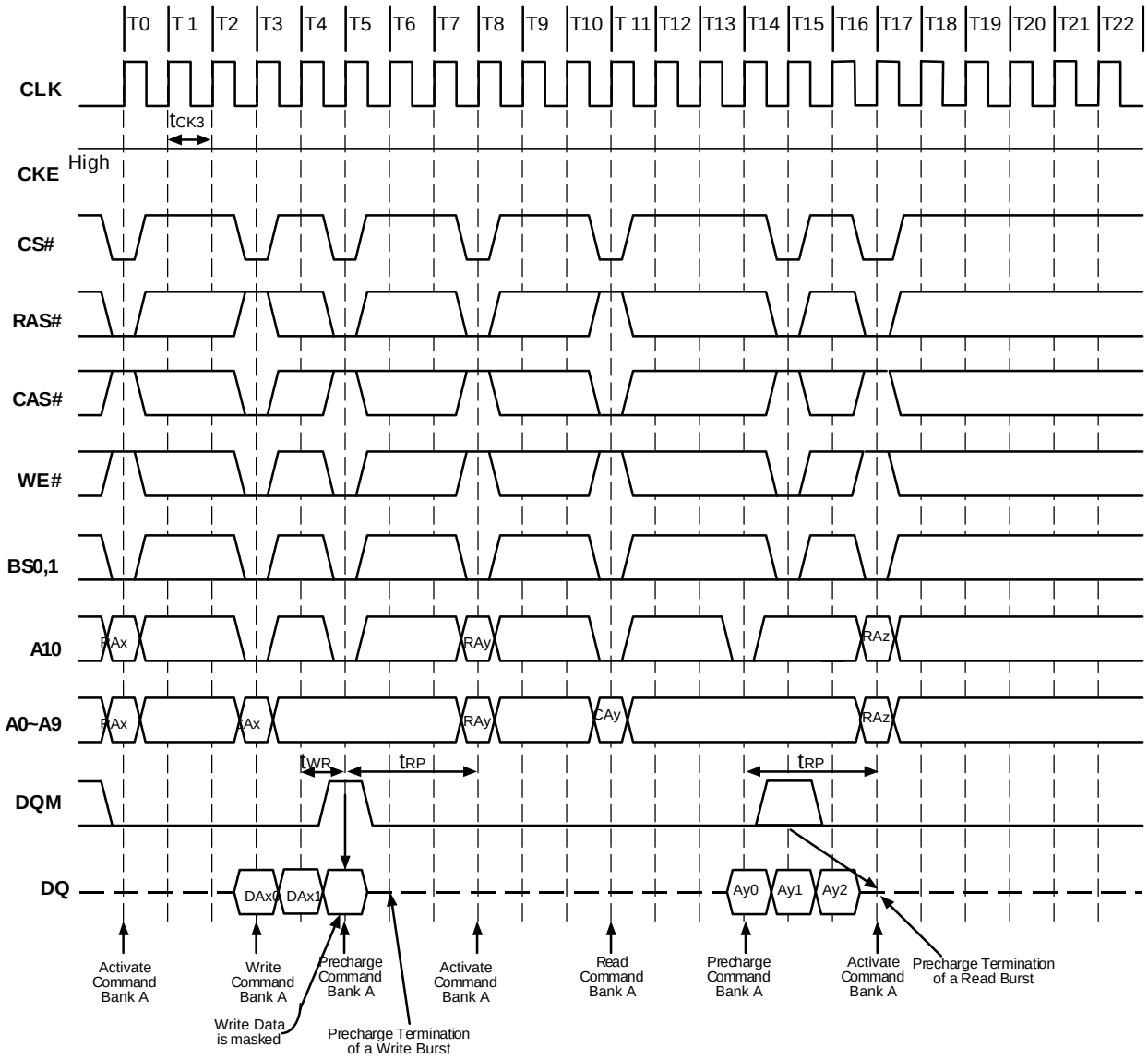
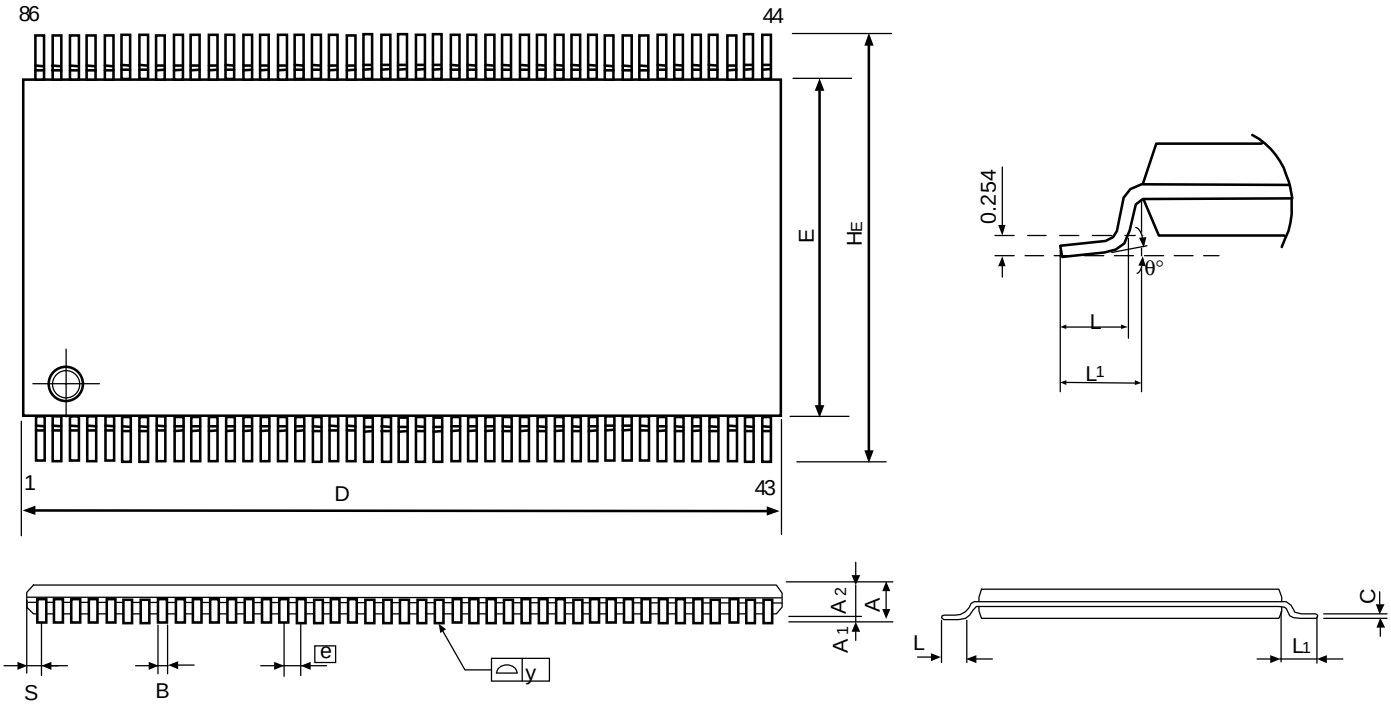


Figure 24.3. Precharge Termination of a Burst
(Burst Length=4, 8 or Full Page, CAS# Latency=3)



86 Pin TSOP II Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Normal	Max	Min	Normal	Max
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.037	0.039	0.041	0.95	1	1.05
B	0.007	0.008	0.009	0.17	0.2	0.23
C	-	0.005	-	-	0.127	-
D	0.87	0.875	0.88	22.09	22.22	22.35
E	0.395	0.400	0.405	10.03	10.16	10.29
e	-	0.0197	-	-	0.50	-
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.0315	-	-	0.80	-
S	-	0.024	-	-	0.61	-
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes :

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension : mm