TPS62620, TPS62621, TPS62622
TPS62623, TPS62624, TPS62625
SLVS848D – JULY 2009 – REVISED OCTOBER 2015

TPS6262x 600-mA, 6-MHz High-Efficiency Step-Down Converter In Chip Scale Packaging

1 Features

- Wide Input Voltage Range from 2.3 V to 5.5 V
- 6 MHz Regulated Frequency Operation
- 90% Efficiency at 6 MHz Operation
- 31 µA Quiescent Current
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Automatic PFM/PWM Mode Switching
- Low Ripple Light-Load PFM Mode
- Internal Soft Start, 120-µs Start-Up Time
- Integrated Active Power-Down Sequencing (TPS62624 only)
- Current Overload and Thermal Shutdown Protection
- Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Complete Sub 1-mm Component Profile Solution
- Total Solution Size < 12 mm^2
- Available in a 6-Pin NanoFree™ (WCSP) Regular and Ultra-Thin Packaging

2 Applications

- Mobile Phones, Smartphones
- WLAN, GPS and Bluetooth™ Applications
- DTV Tuner Applications
- DC/DC Micro Modules

3 Description

The TPS6262x device family provides high-frequency synchronous step-down DC/DC converters optimized for battery-powered portable applications. Intended for low-power applications, the TPS6262x devices support up to 600 mA load current, and allow the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3 V to 5.5 V, the devices support applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 1.2 V to 2.3 V.

The TPS6262x devices operate at a regulated 6-MHz switching frequency and enter the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The pulse frequency modulation (PFM) mode extends the battery life by reducing the quiescent current to 31 µA (typical) during light load and standby operation. For noise-sensitive applications, the device can be forced into fixed frequency pulse width modulation (PWM) mode by pulling the MODE pin high.

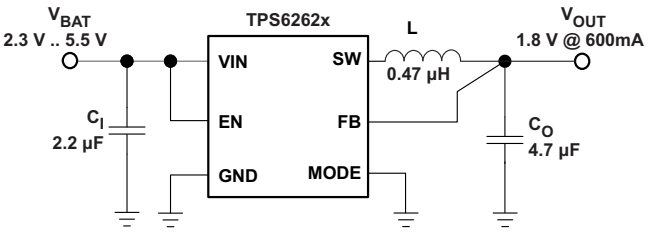
The TPS6262x devices operate over a free air temperature range of –40°C to 85°C. They are available in a 6-pin chip-scale package (WCSP).

Device Information(1)

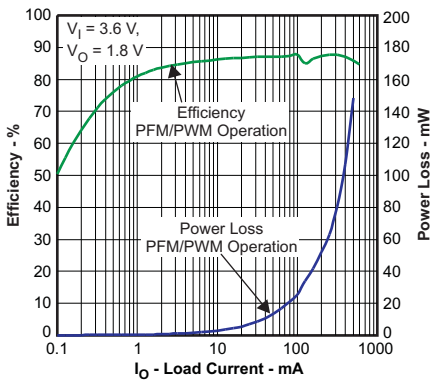
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6262x	DSBGA (6)	1.30 mm × 0.96 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Efficiency vs. Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2011) to Revision D — **Page**

- Added *ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section* ... 1
- Changed Chip Scale package marking code from YMSS and LLLL, to YMDS and CC ... 21

Changes from Revision B (December 2009) to Revision C — **Page**

- Changed $I_{(SD)}$ specification MAX rating from 1 TO 2.5 in ELEC CHARA table, under SUPPLY CURRENT. ... 5

Changes from Revision A (July 2009) to Revision B — **Page**

- Added YFD package option ... 21

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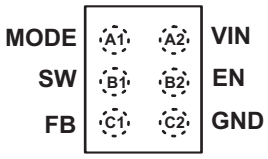
5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	OUTPUT DISCHARGE FUNCTION	PACKAGE MARKING CHIP CODE
TPS62620	1.82 V	No	GF
			GE
TPS62621	1.8 V	No	GH
TPS62622	1.5 V	No	GV
TPS62623	1.225 V	No	GZ
			K3
TPS62624	1.2 V	Yes	GX
TPS62625	1.2 V	No	KC

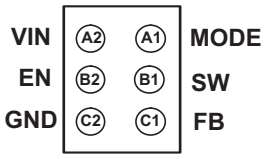
6 Pin Configuration and Functions

YFF or YFD Package
6-Pin DSBGA

TPS6262x
(TOP VIEW)



TPS6262x
(BOTTOM VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE	A1	IN	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = Low: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents.
			MODE = High: Low-noise mode enabled, regulated frequency PWM operation forced.
VIN	A2	IN	Power supply input.
SW	B1	IN/OUT	This is the switch pin of the converter and is connected to the drain of the internal power MOSFETs.
EN	B2	IN	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_{IN} enables the device. This pin must not be left floating and must be terminated.
FB	C1	IN	Output feedback sense input. Connect FB to the converter's output.
GND	C2	–	Ground pin.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Voltage at VIN, SW (2)	–0.3	7	V
	Voltage at FB (2)	-0.3	3.6	
	Voltage at EN, MODE (2)	-0.3	V_{IN} + 0.3	
	Power dissipation	Internally limited		
T_A	Operating temperature range (3)	-40	85	°C
T_J (max)	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{IN}	2.3		5.5	V
Operating free air temperature, T_A	–40		85	°C
Operating junction temperature, T_J			150	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS626x YFF/YFD (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.3 V to 5.5 V, V_{OUT} = 1.82 V, EN = 1.82 V, AUTO mode and T_A = –40°C to 85°C. Typical values are at V_{IN} = 3.6 V, V_{OUT} = 1.82 V, EN = 1.82 V, AUTO mode and T_A = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{IN}	Input voltage range			2.3		5.5	V
I_Q	Operating quiescent current		I_{OUT} = 0 mA, device not switching		31	55	µA
			I_{OUT} = 0 mA, PWM mode		7.6		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	2.5	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage			1.0			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1	µA
POWER SWITCH							
$R_{DS(on)}$	P-channel MOSFET on resistance	TPS62620 TPS62621 TPS62622	V_{IN} = $V_{(GS)}$ = 3.6 V, PWM mode		270		mΩ
			V_{IN} = $V_{(GS)}$ = 2.5 V, PWM mode		350		mΩ
		TPS62623 TPS62624	V_{IN} = $V_{(GS)}$ = 3.6 V, PWM mode		480		mΩ
			V_{IN} = $V_{(GS)}$ = 2.5 V, PWM mode		640		mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5 V, –40°C ≤ T_J ≤ 85°C			1	µA
$R_{DS(on)}$	N-channel MOSFET on resistance	TPS6262x	V_{IN} = $V_{(GS)}$ = 3.6 V, PWM mode		140		mΩ
			V_{IN} = $V_{(GS)}$ = 2.5 V, PWM mode		200		mΩ
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5 V, –40°C ≤ T_J ≤ 85°C			1	µA
R_{DIS}	Discharge resistor for power-down sequence				15	50	Ω
	P-MOS current limit		2.3 V ≤ V_{IN} ≤ 4.8 V, open loop	975	1100	1200	mA
	Input current under short-circuit conditions		V_{OUT} shorted to ground		19		mA
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS6262x	I_{OUT} = 0 mA, PWM mode	5.4	6	6.6	MHz
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS6262x	2.3 V ≤ V_{IN} ≤ 4.8 V, 0 mA ≤ I_{OUT} ≤ 600 mA PFM/PWM operation	0.98 × V_{NOM}	V_{NOM}	1.03 × V_{NOM}	V
			2.3 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 600 mA PFM/PWM operation	0.98 × V_{NOM}	V_{NOM}	1.04 × V_{NOM}	V
			2.3 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 600 mA PWM operation	0.98 × V_{NOM}	V_{NOM}	1.02 × V_{NOM}	V
	Line regulation		V_{IN} = V_{OUT} + 0.5 V (min 2.3 V) to 5.5V, I_{OUT} = 200 mA		0.13		%/V
	Load regulation		I_{OUT} = 0 mA to 600 mA		–0.0003		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power save mode ripple voltage	TPS62620 TPS62621	I_{OUT} = 1 mA		20		mV_{PP}
		TPS62623 TPS62624	I_{OUT} = 1 mA		24		mV_{PP}
	Start-up time	TPS62620	I_{OUT} = 0 mA, time from active EN to V_{OUT}		120		µs

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7.6 Typical Characteristics

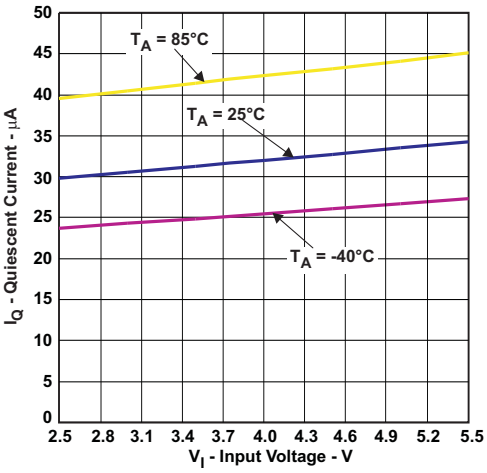
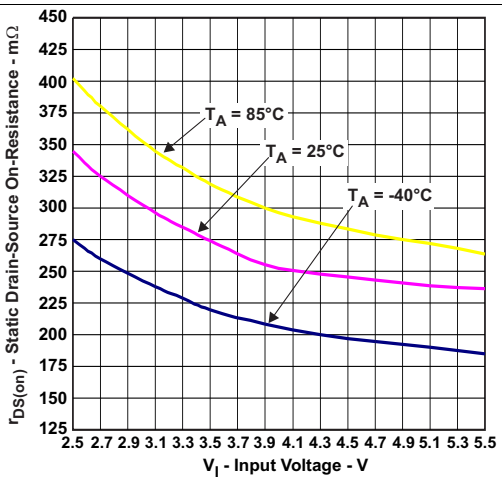
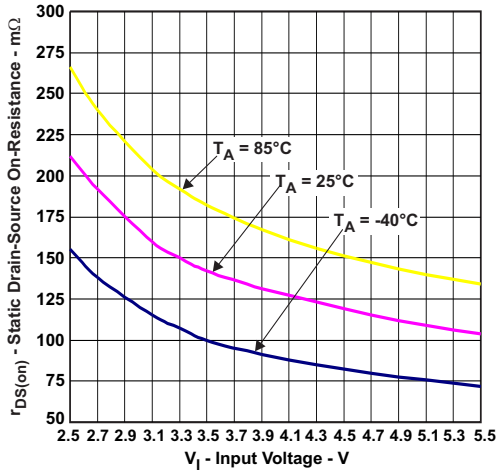


Figure 1. Quiescent Current vs Input Voltage



TPS62620 PWM Mode Operation

Figure 2. P-Channel $R_{DS(on)}$ vs Input Voltage



TPS62620 PWM Mode Operation

Figure 3. N-Channel $R_{DS(on)}$ vs Input Voltage

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8 Detailed Description

8.1 Overview

The TPS6262x synchronous step-down DC/DC converters typically operate at a regulated 6-MHz frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the TPS6262x converters operate in power-save mode with pulse frequency modulation (PFM).

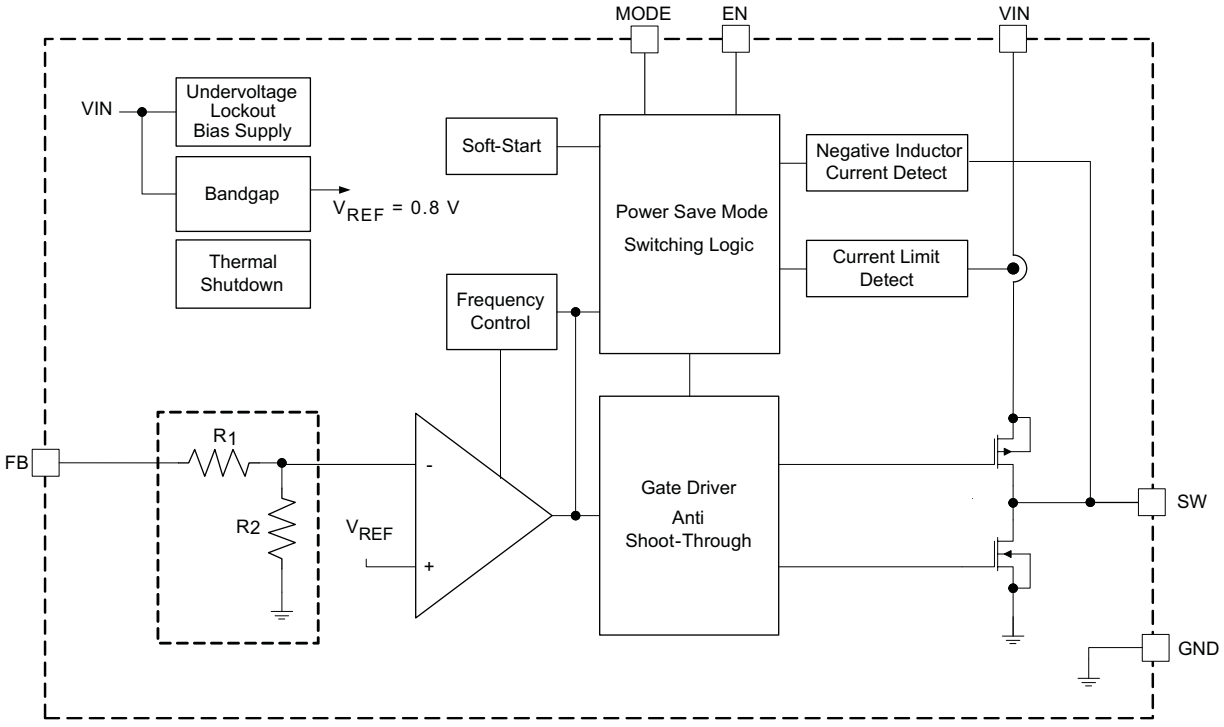
The converters use a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_{OUT} is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6262x converters are inherently stable over a range of L and C_{OUT}.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 31 µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Mode Selection

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

8.3.2 Enable

The device starts operation when EN is set high and starts up with the soft start. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1 µA. In this mode, the P- and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

8.3.3 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6262x devices have a UVLO threshold set to 2.05 V (typical). Fully functional operation is permitted down to 2.1 V input voltage.

8.3.4 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6262x devices have an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the on-time from a minimum pulse-width of 35 ns as a function of the output voltage. This mode of operation continues for ca. 100 µs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSFET remains on until the inductor current has reset. After a further 100 µs, the device ramps up to the full current limit operation if the output voltage has risen above 0.5 V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

8.4.2 Switching Frequency

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10 MHz to 12 MHz, which is controlled to circa 6 MHz by a frequency locked loop.

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Device Functional Modes (continued)

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6 MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6 MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

8.4.3 Power-Save Mode

If the load current decreases, the converter will enter power save mode operation automatically. During power-save mode the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFM on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

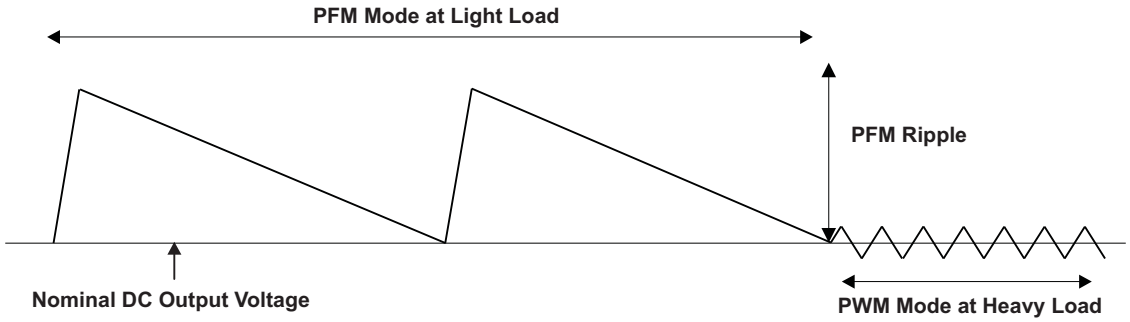


Figure 4. Operation in PFM Mode and Transfer to PWM Mode

8.4.4 Output Capacitor Discharge (TPS62624 Only)

The TPS62624 device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 15 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value. All the other voltage options do not have the output capacitor discharge function enabled.

8.4.5 Short-Circuit Protection

The TPS6262x devices integrate a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4 V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5 V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6262x device family provides high-frequency synchronous step-down DC/DC converters optimized for battery-powered portable applications. Intended for low-power applications, the TPS6262x devices support up to 600 mA load current, and allow the use of low cost chip inductor and capacitors.

9.2 Typical Application

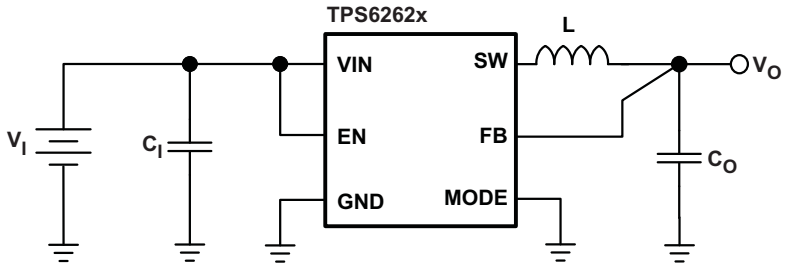


Figure 5. TPS6262x Typical Application Schematic

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions.

Table 1 shows the list of components for the *Application Curves*.

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
L	1 µH	MURATA LQM21PN1R0NGR
C_{IN}	2.2µF, 6.3V, 0402, X5R	MURATA GRM155R60J225ME15
C_{OUT}	4.7µF, 6.3V, 0402, X5R	MURATA GRM155R60J475M

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The TPS6262x device family of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3 µH to 1.3 µH and with output capacitors in the range of 4.7 µF to 10 µF. The internal compensation is optimized to operate with an output filter of L = 0.47 µH and C_{OUT} = 4.7 µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see section *Checking Loop Stability*.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

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$$\Delta I_L = \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{L \times f_{SW}}$$

where:

- f_{SW} = Switching frequency (6 MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current (1)

$$\Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

where:

- ΔI_L = Peak-to-peak inductor ripple current
- $I_{L(MAX)}$ = Maximum inductor current (2)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6262x converters.

Table 2. List Of Inductors(1)

MANUFACTURER	SERIES	DIMENSIONS
MURATA	LQM21PN1R0NGR	2.0 x 1.2 x 1.0 max. height
	LQM21PNR54MG0	2.0 x 1.2 x 1.0 max. height
	LQM21PNR47MC0	2.0 x 1.2 x 0.55 max. height
	LQM21PN1R0MC0	2.0 x 1.2 x 0.55 max. height
	LQM21PN1R5MC0	2.0 x 1.2 x 0.55 max. height
HITACHI METALS	HSLI-201210AG-R47	2.0 x 1.2 x 1.0 max. height
	HSLI-201210SW-R85	2.0 x 1.2 x 1.0 max. height
	JSLI-201610AG-R70	2.0 x 1.6 x 1.0 max. height
TOKO	MDT2012-CX1R0A	2.0 x 1.2 x 1.0 max. height
FDK	MIPS2012D1R0-X2	2.0 x 1.2 x 1.0 max. height
TAIYO YUDEN	NM2012NR82	2.0 x 1.2 x 1.0 max. height
	NM20121NR0	2.0 x 1.2 x 1.0 max. height

(1) See the *Third-Party Products* disclaimer.

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9.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS6262x converters allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 1.6 µF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 4.7 µF capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is 1% of the nominal output voltage V_{OUT}.

The output voltage ripple during PFM mode operation can be kept very small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger ones. Increasing the output capacitor value and the effective inductance will minimize the output ripple voltage.

9.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2-µF capacitor is sufficient.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_{IN}.

9.2.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

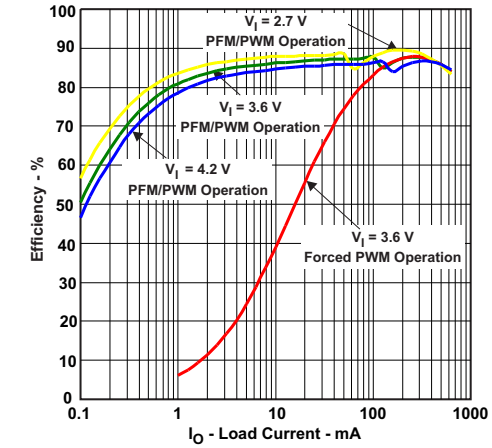
As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $R_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

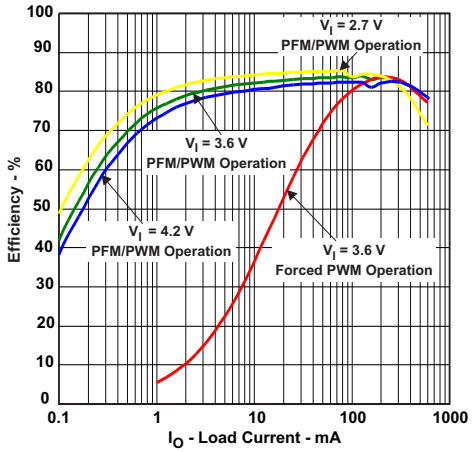
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9.2.3 Application Curves



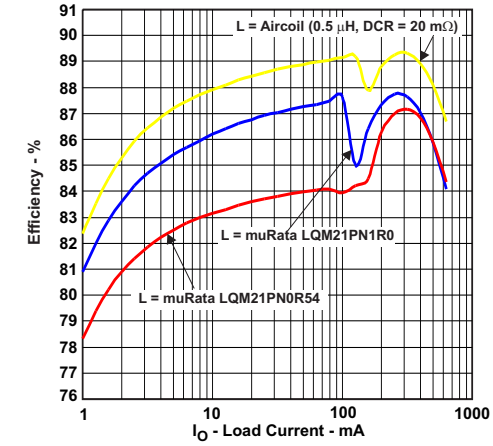
V_{OUT} = 1.82 V

Figure 6. Efficiency vs Load Current, V_{OUT} = 1.82 V



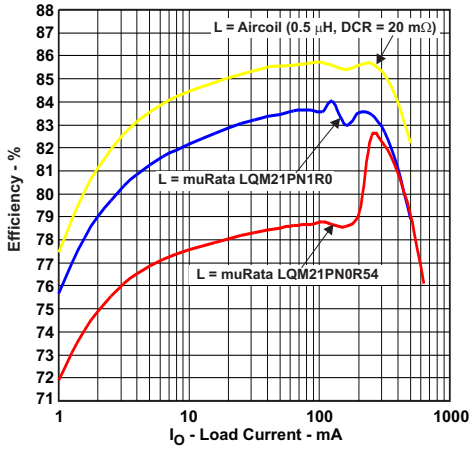
V_{OUT} = 1.2 V

Figure 7. Efficiency vs Load Current, V_{OUT} = 1.2 V



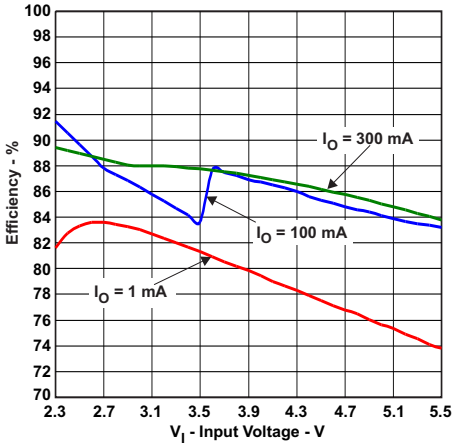
V_{OUT} = 1.82 V V_{IN} = 3.6 V PFM/PWM Operation

Figure 8. Efficiency vs Load Current, V_{OUT} = 1.82 V, PWM/PFM Operation



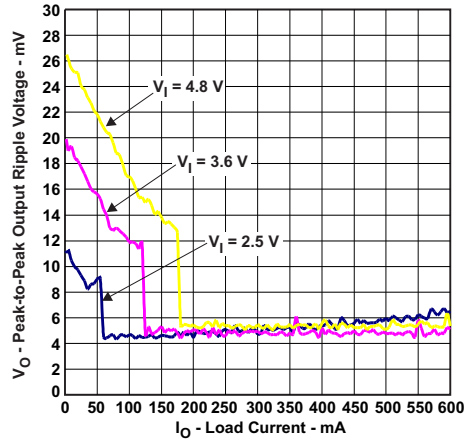
V_{OUT} = 1.2 V V_{IN} = 3.6 V PFM/PWM Operation

Figure 9. Efficiency vs Load Current, V_{OUT} = 1.2 V, PWM/PFM Operation



V_{OUT} = 1.82 V PFM/PWM Operation

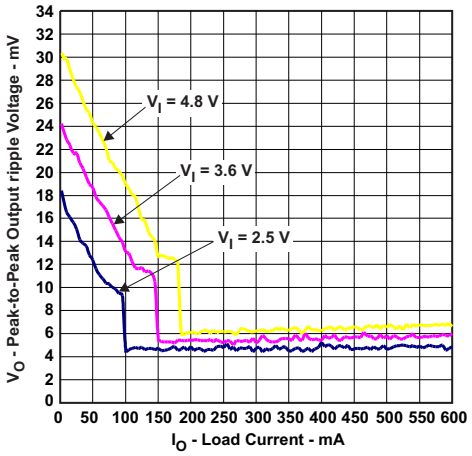
Figure 10. Efficiency vs Input Voltage, V_{OUT} = 1.82 V, PWM/PFM Operation



V_{OUT} = 1.82 V

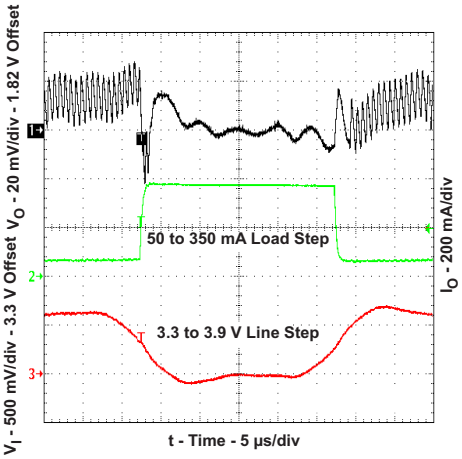
Figure 11. Peak-To-Peak Output Ripple Voltage vs Load Current, V_{OUT} = 1.82 V

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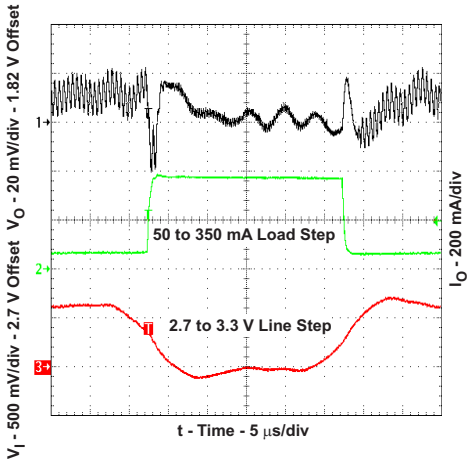
V_{OUT} = 1.2 V

Figure 12. Peak-To-Peak Output Ripple Voltage vs Load Current, V_{OUT} = 1.2 V



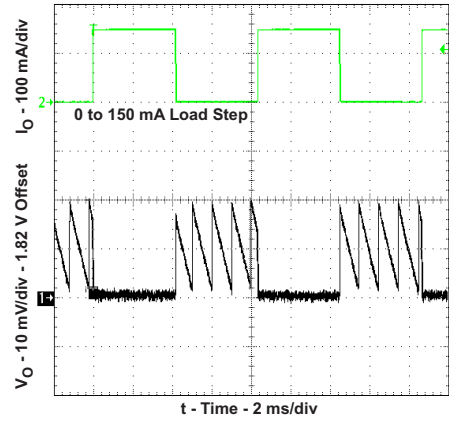
V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

Figure 13. Combined Line/Load Transient Response, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



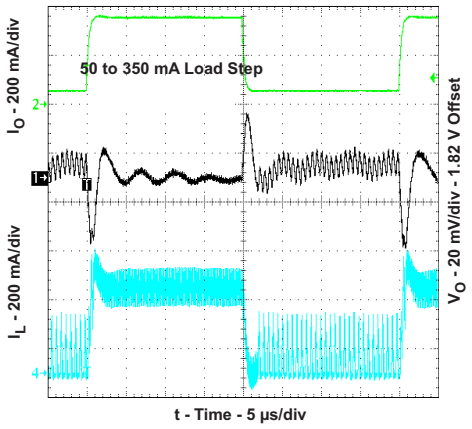
V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

Figure 14. Combined Line/Load Transient Response, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



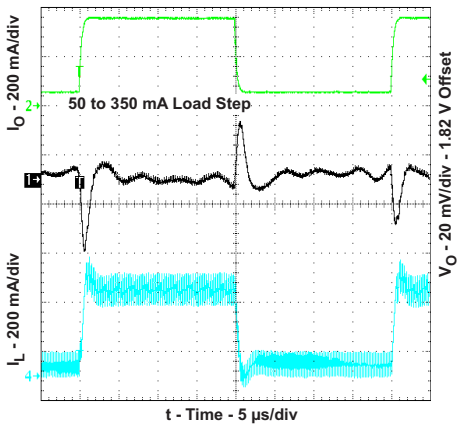
V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

Figure 15. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

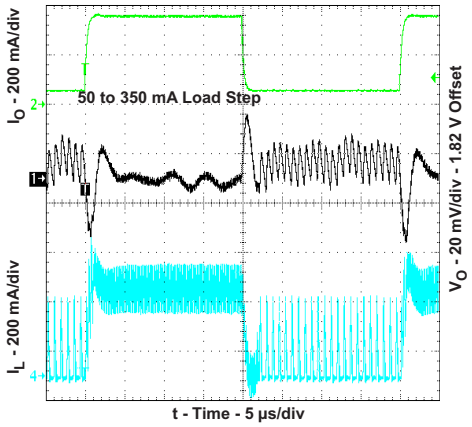
Figure 16. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



V_{OUT} = 1.82 V V_{IN} = 2.7 V MODE = Low

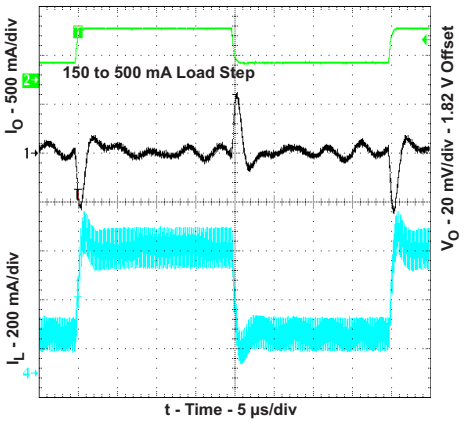
Figure 17. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 2.7 V

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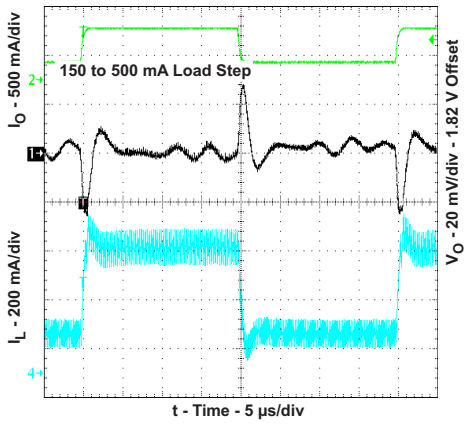
V_{OUT} = 1.82 V V_{IN} = 4.8 V MODE = Low

Figure 18. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 4.8 V



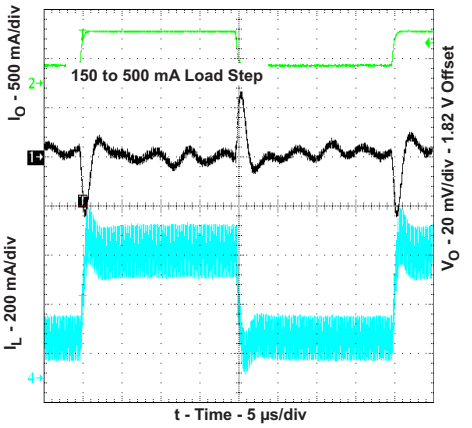
V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

Figure 19. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



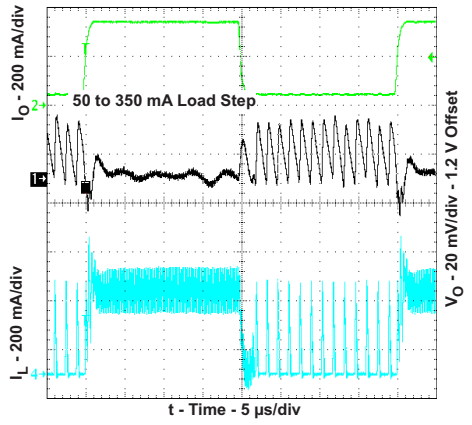
V_{OUT} = 1.82 V V_{IN} = 2.7 V MODE = Low

Figure 20. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 2.7 V



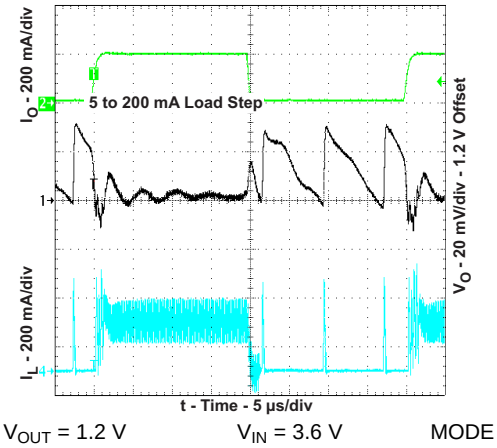
V_{OUT} = 1.82 V V_{IN} = 4.8 V MODE = Low

Figure 21. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.82 V, V_{IN} = 4.8 V



V_{OUT} = 1.2 V V_{IN} = 3.6 V MODE = Low

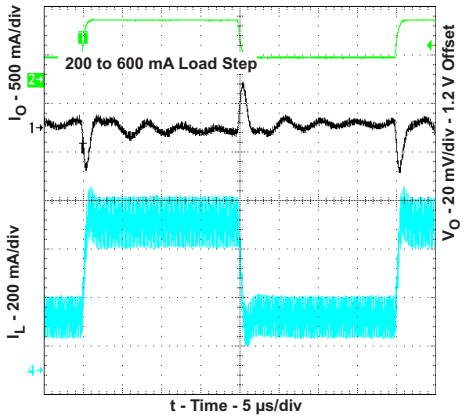
Figure 22. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.2 V, V_{IN} = 3.6 V



V_{OUT} = 1.2 V V_{IN} = 3.6 V MODE = Low

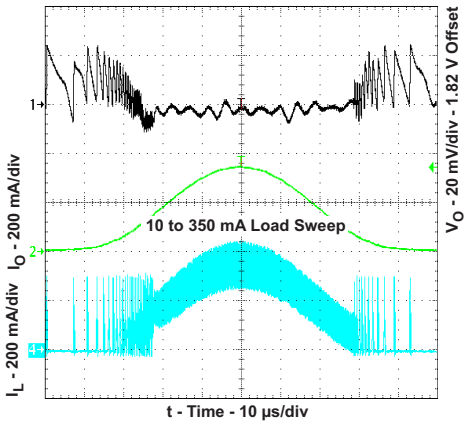
Figure 23. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.2 V, V_{IN} = 3.6 V

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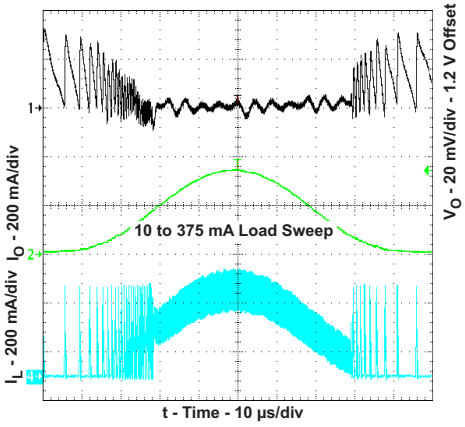
V_{OUT} = 1.2 V V_{IN} = 3.6 V MODE = Low

Figure 24. Load Transient Response in PFM/PWM Operation, V_{OUT} = 1.2 V, V_{IN} = 3.6 V



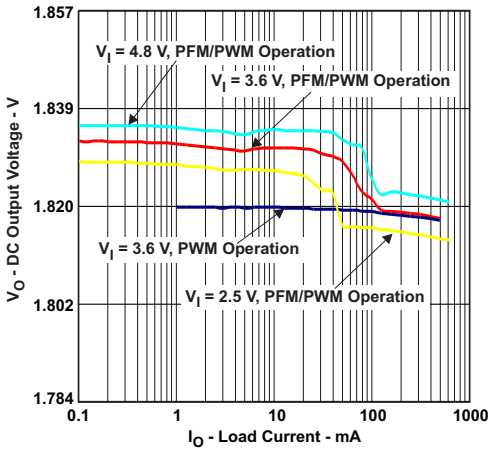
V_{OUT} = 1.82 V V_{IN} = 3.6 V MODE = Low

Figure 25. AC Load Transient Response, V_{OUT} = 1.82 V, V_{IN} = 3.6 V



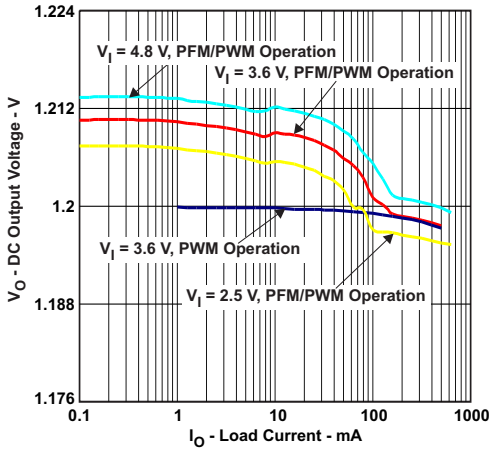
V_{OUT} = 1.2 V V_{IN} = 3.6 V MODE = Low

Figure 26. AC Load Transient Response, V_{OUT} = 1.2 V, V_{IN} = 3.6 V



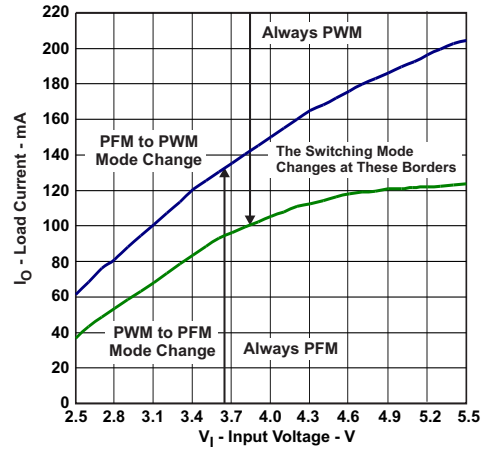
V_{OUT} = 1.82 V PFM/PWM Operation

Figure 27. DC Output Voltage vs Load Current, V_{OUT} = 1.82 V



V_{OUT} = 1.2 V PFM/PWM Operation

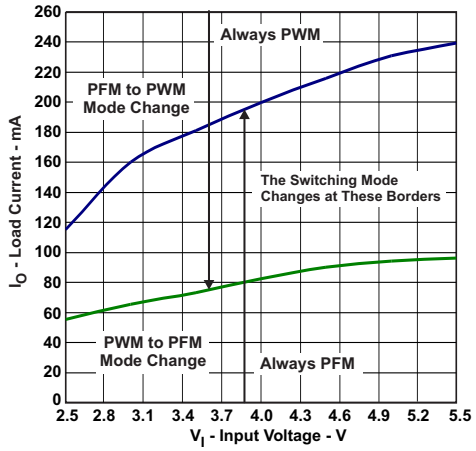
Figure 28. DC Output Voltage vs Load Current, V_{OUT} = 1.2 V



V_{OUT} = 1.82 V Mode Change

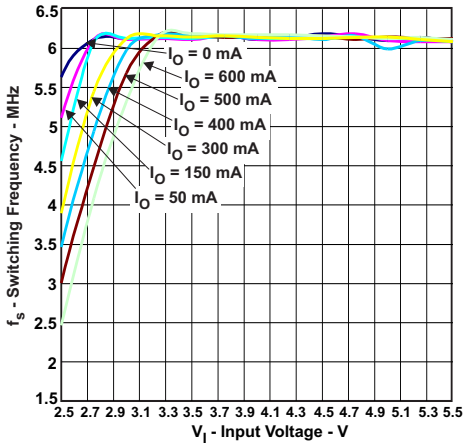
Figure 29. PFM/PWM Boundaries, V_{OUT} = 1.82 V

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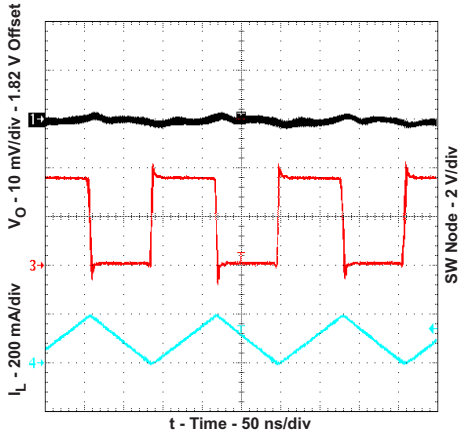
V_{OUT} = 1.2 V Mode Change

Figure 30. PFM/PWM Boundaries, V_{OUT} = 1.2 V



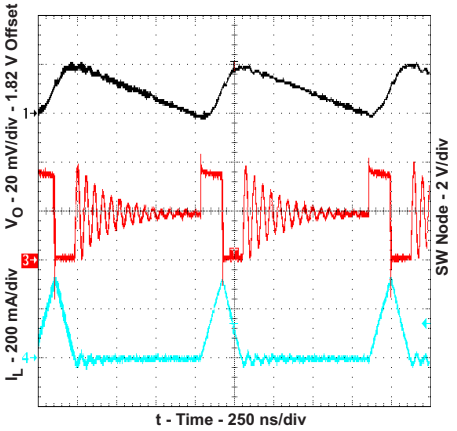
V_{OUT} = 1.82 V

Figure 31. PWM Switching Frequency vs Input Voltage



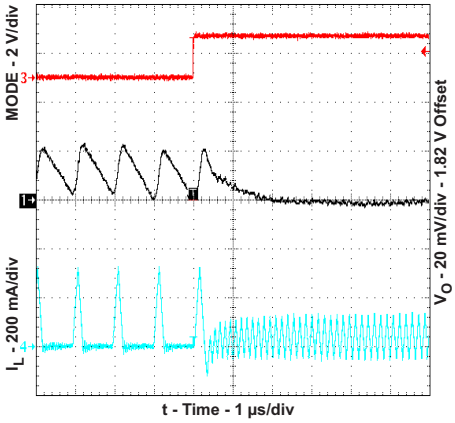
V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 100 mA MODE = High

Figure 32. PWM Operation



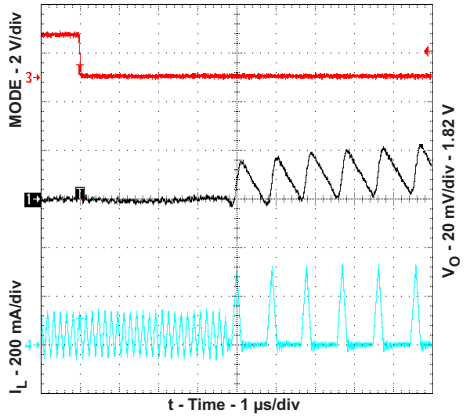
V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 40 mA MODE = Low

Figure 33. Power-Save Mode Operation



V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 40 mA

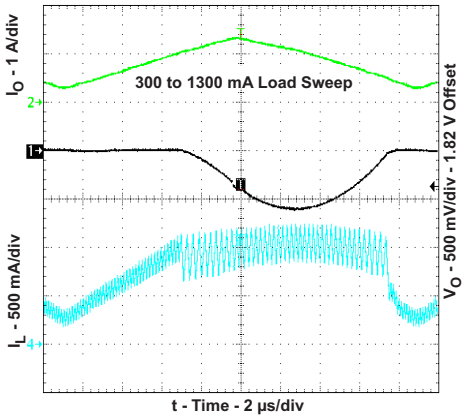
Figure 34. Mode Change Response



V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 40 mA

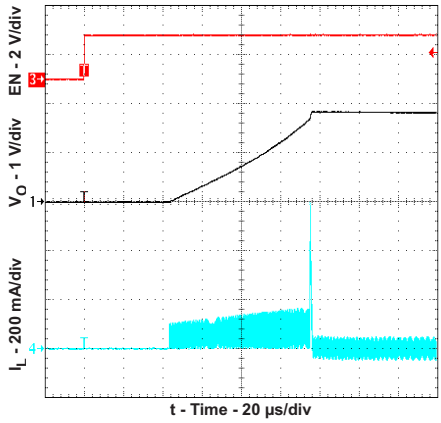
Figure 35. Mode Change Response

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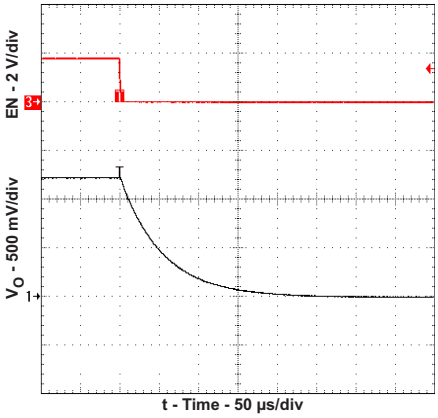
V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 40 mA
MODE = Low

Figure 36. Over-Current Fault Operation



V_{OUT} = 1.82 V V_{IN} = 3.6 V I_{OUT} = 0 mA
TPS62620 MODE = Low

Figure 37. Start-Up



V_{OUT} = 1.2 V V_{IN} = 3.6 V I_{OUT} = 0 mA
TPS62624 MODE = Low

Figure 38. Shutdown

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10 Power Supply Recommendations

The TPS6262x device family has no special requirements for its input power supply. The input power supply' s output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6262x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6262x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) should be taken in the output capacitor path, approximately 1 mm away from it. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

11.2 Layout Example

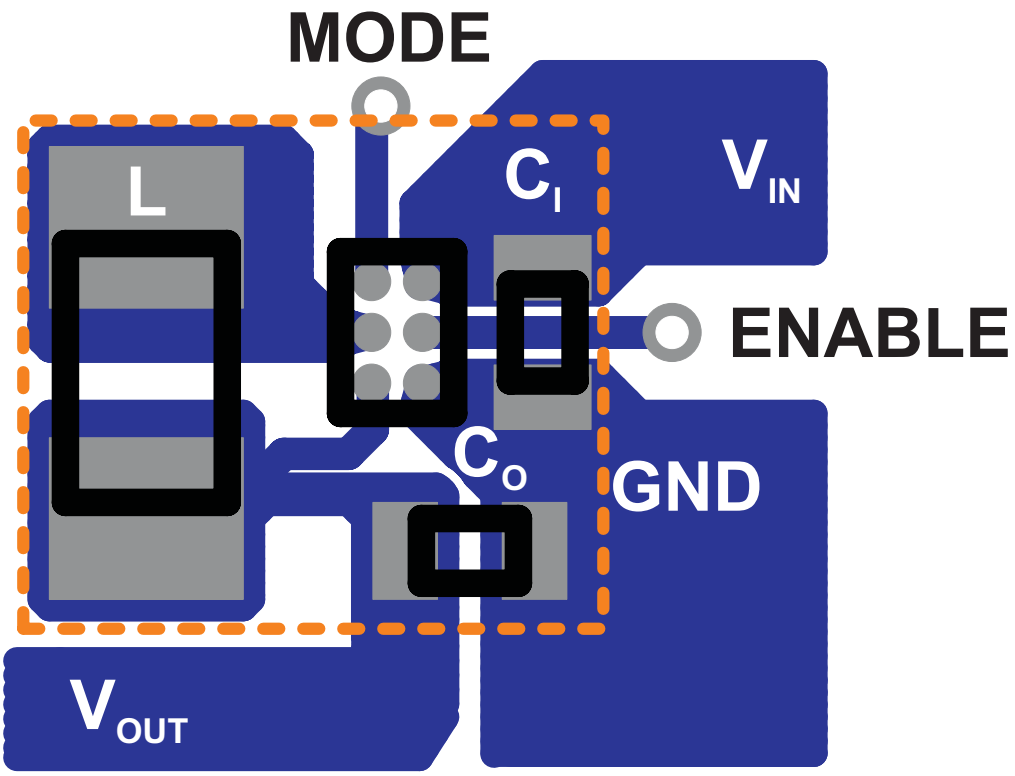


Figure 39. Suggested Layout (Top)

11.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS6262x devices is 105°C. The thermal resistance of the 6-pin CSP package (YFF-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{125°C/W} = 160\ mW \quad (3)$$

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62620	Click here	Click here	Click here	Click here	Click here
TPS62621	Click here	Click here	Click here	Click here	Click here
TPS62622	Click here	Click here	Click here	Click here	Click here
TPS62623	Click here	Click here	Click here	Click here	Click here
TPS62624	Click here	Click here	Click here	Click here	Click here
TPS62625	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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12.5 Glossary

SLYZ022 — *TI Glossary*.

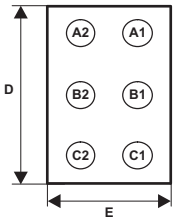
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

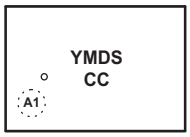
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Summary

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE
(TOP VIEW)



Code:

- YM — Year Month date code
- D — Day of Laser Mark
- S — Assembly site code
- CC — Chip code

13.2 Chip Scale Package Dimensions

The TPS6262x devices are available in an 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = 1.30 ±0.03 mm
- E = 0.926 ±0.03 mm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62620YFDR	ACTIVE	DSBGA	YFD	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GE	Samples
TPS62620YFDT	ACTIVE	DSBGA	YFD	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GE	Samples
TPS62620YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GF	Samples
TPS62620YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GF	Samples
TPS62621YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GH	Samples
TPS62621YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GH	Samples
TPS62622YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GV	Samples
TPS62622YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GV	Samples
TPS62623YFDR	ACTIVE	DSBGA	YFD	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	K3	Samples
TPS62623YFDT	ACTIVE	DSBGA	YFD	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	K3	Samples
TPS62623YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GZ	Samples
TPS62623YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GZ	Samples
TPS62624YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GX	Samples
TPS62624YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GX	Samples
TPS62625YFFR	ACTIVE	DSBGA	YFF	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	KC	Samples
TPS62625YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	KC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

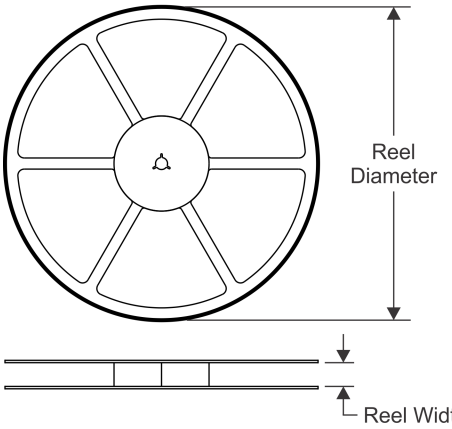
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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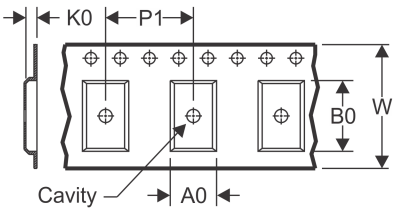
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

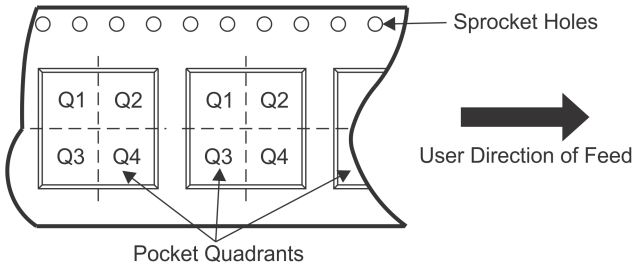


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

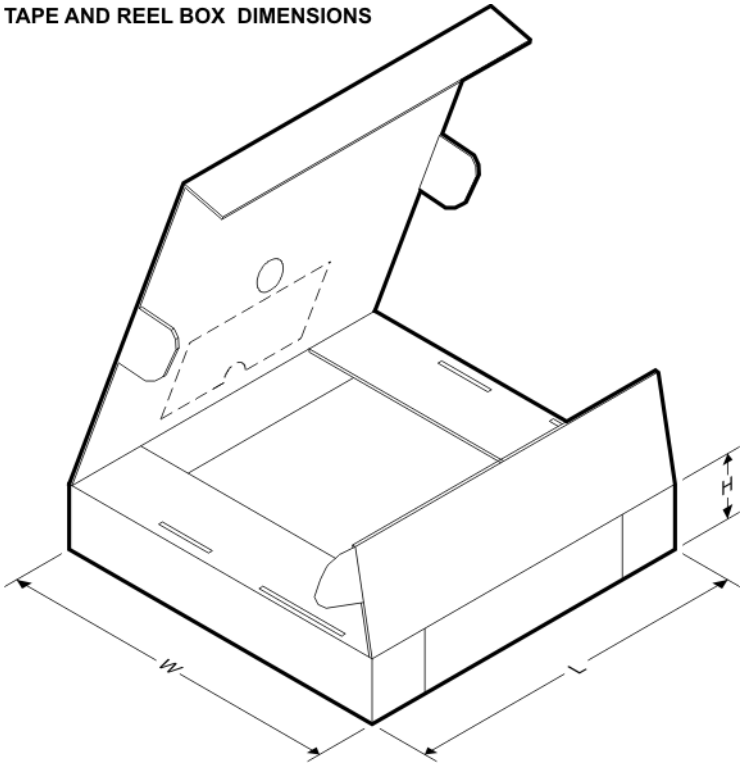
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62620YFDR	DSBGA	YFD	6	3000	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62620YFDR	DSBGA	YFD	6	3000	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62620YFDT	DSBGA	YFD	6	250	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62620YFDT	DSBGA	YFD	6	250	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62620YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62620YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62621YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62621YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62622YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62622YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62623YFDR	DSBGA	YFD	6	3000	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62623YFDT	DSBGA	YFD	6	250	180.0	8.4	1.03	1.53	0.56	4.0	8.0	Q1
TPS62623YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62623YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62624YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62624YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62625YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62625YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

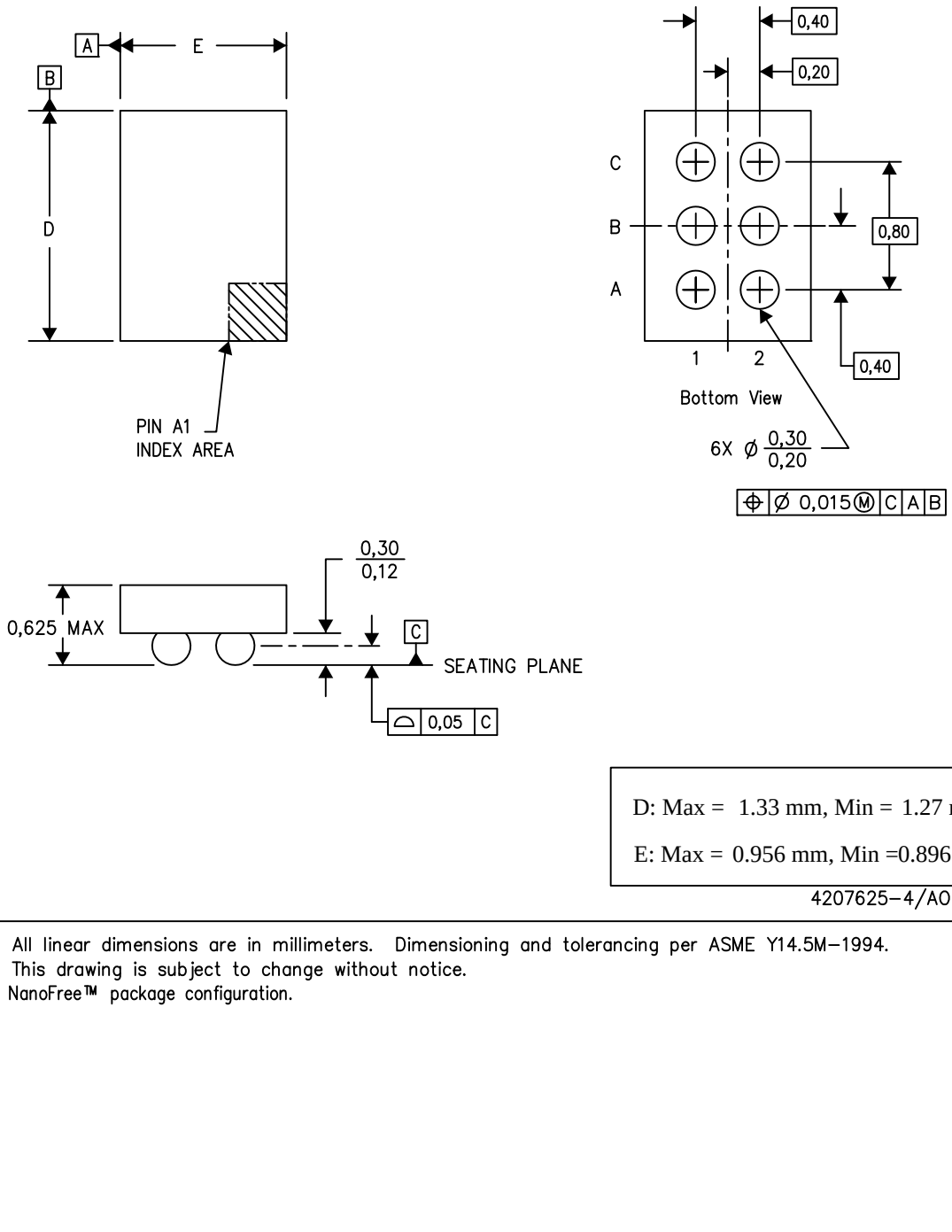
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62620YFDR	DSBGA	YFD	6	3000	220.0	220.0	34.0
TPS62620YFDR	DSBGA	YFD	6	3000	210.0	185.0	35.0
TPS62620YFDT	DSBGA	YFD	6	250	220.0	220.0	34.0
TPS62620YFDT	DSBGA	YFD	6	250	210.0	185.0	35.0
TPS62620YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62620YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62621YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62621YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62622YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62622YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62623YFDR	DSBGA	YFD	6	3000	220.0	220.0	34.0
TPS62623YFDT	DSBGA	YFD	6	250	220.0	220.0	34.0
TPS62623YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62623YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62624YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62624YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS62625YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62625YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

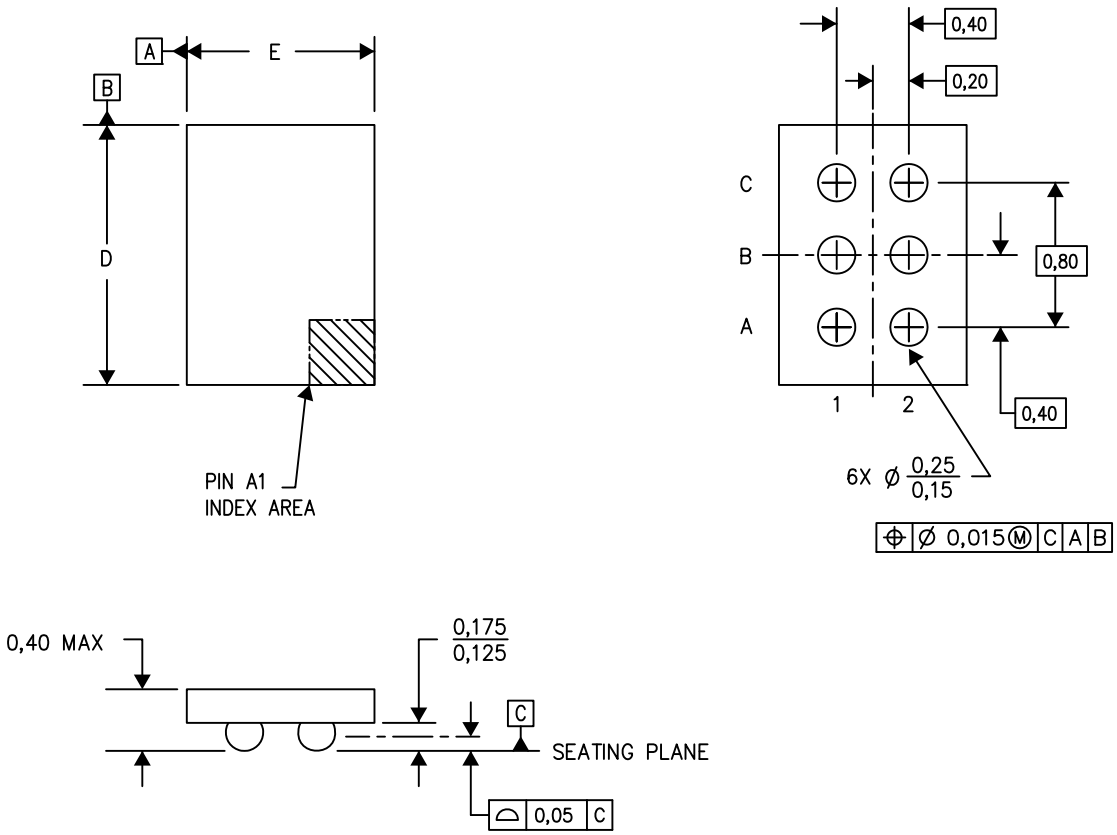
YFF (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YFD (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



D: Max = 1.33 mm, Min = 1.27 mm

E: Max = 0.956 mm, Min =0.896 mm

4209617–2/F 05/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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