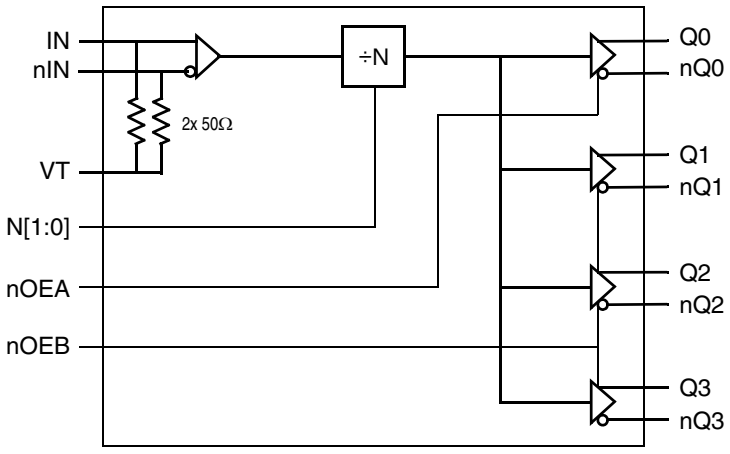
General Description

The 8P73S674 is a 1.8V LVPECL Clock Divider and Fanout Buffer. The device has been designed for clock signal division and fanout in wireless base station (radio and base band), high-end computing and telecommunication equipment. The device is optimized to deliver excellent phase noise performance. The 8P73S674 uses SiGe technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection. The device offers the frequency division by ÷1, ÷2, ÷4 and ÷8. Four low-skew 1.8V LVPECL outputs are available for and support clock output frequencies up to 1GHz (÷1 frequency division). 1.8V LVPECL outputs are terminated 50Ω to GND. Outputs can be disabled to save power consumption if not used. The device is packaged in a lead-free (RoHS 6) 20-lead VFQFN package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

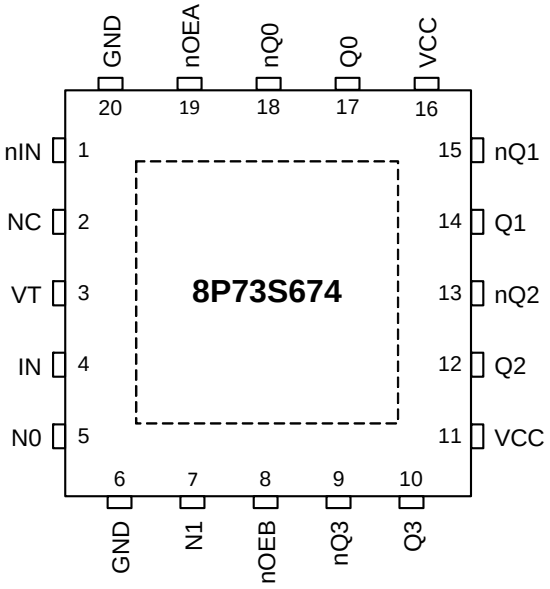
Features

- Clock signal division and distribution
- SiGe technology for high-frequency and fast signal rise/fall times
- Four low-skew LVPECL clock outputs
- Supports frequency division of ÷1, ÷2, ÷4 and ÷8
- Maximum Output frequency: 1GHz
- Output skew: 100ps (maximum)
- LVPECL output rise/fall time (20% - 80%): 220ps (maximum)
- 1.8V core and output supply mode
- Supports 1.8V I/O LVCMOS logic levels for all control pins
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) 20-lead VFQFN packaging

Block Diagram



Pin Assignment



20-pin, 2.15mm x 2.15mm, EPad, VFQFN Package

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Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	nIN	Input	—	Clock signal inverting differential input. Internal termination 50Ω to VT.
2	NC	Unused	—	Not connected.
3	VT	—	—	Leave open if IN, nIN is used with LVDS signals.
4	IN	Input	—	Clock signal non-inverting differential input. Internal termination 50Ω to VT.
5	N0	Input	Pulldown	Frequency divider control. 1.8V LVCMOS/LVTTL interface levels.
6	GND	Power	—	Power supply ground.
7	N1	Input	Pulldown	Frequency divider control. 1.8V LVCMOS/LVTTL interface levels.
8	nOEB	Input	Pulldown	Output enable control for the Q1, Q2 and Q3 outputs. 1.8V LVCMOS/LVTTL interface levels.
9	nQ3	Output	—	Differential clock output 3. 1.8V LVPECL output levels.
10	Q3	Output	—	
11	V_{CC}	Power	—	Supply voltage for the clock outputs.
12	Q2	Output	—	Differential clock output 2. 1.8V LVPECL output levels.
13	nQ2	Output	—	
14	Q1	Output	—	Differential clock output 1. 1.8V LVPECL output levels.
15	nQ1	Output	—	
16	V_{CC}	Power	—	Supply voltage for the clock outputs.
17	Q0	Output	—	Differential clock output 0. 1.8V LVPECL output levels.
18	nQ0	Output	—	
19	nOEA	Input	Pulldown	Output enable control for the Q0 output. 1.8V LVCMOS/LVTTL interface levels.
20	GND	Power	—	Power supply ground.
EPAD	GND_EP	Power	—	Exposed package pad negative supply voltage (GND). Return current path for the Q0, Q1, Q2 and Q3 outputs.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Truth Tables

Table 3A. N Clock Divider

Input		
N1	**N0**	**Divider Value**
0 (default)	0 (default)	÷1
0	1	÷2
1	0	÷4
1	1	÷8

Table 3B. nOEA Output Enable

Input	Output
nOEA	**Q0**
0 (default)	Output is enabled
1	Output is disabled in logic low state

Table 3C. nOEB Output Enable

Input	Output
nOEB	**Q1, Q2, Q3**
0 (default)	Outputs are enabled
1	Outputs are disabled in logic low state

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs	-0.5V to V_{CC} + 0.5V
Input Current, IN, nIN	±30mA
V_T Current, I_{VT}	±60mA
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Junction Temperature	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 1.8V ±0.15V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		1.65	1.8	1.95	V
I_{CC}	Power Supply Current	Outputs Unloaded		62	73	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 1.8V ±0.15V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.2		1.8	V
V_{IL}	Input Low Voltage			-0.3		0.3	V
I_{IH}	Input High Current	N0, N1, nOEA, nOEB	V_{CC} = 1.95V, V_{IN} = 1.95V			150	µA
I_{IL}	Input Low Current	N0, N1, nOEA, nOEB	V_{CC} = 1.95V, V_{IN} = 0V	-10			µA

Table 4C. Differential Input DC Characteristics, V_{CC} = 1.8V ±0.15V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	IN, nIN	Across IN and nIN with VT floated	70	100	130	Ω
I_{IN}	Input Current	IN, nIN				25	mA

Table 4D. LVPECL DC Characteristics, V_{CC} = 1.8V ±0.15V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[1]		V_{CC} – 1.1		V_{CC} – 0.75	V
V_{OL}	Output Low Voltage[1]				V_{CC} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing[1]		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to GND.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 1.8V ±0.15V, T_A = -40°C to +85°C[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Input Voltage Swing	IN, nIN		0.2		1	V
V_{DIFF_IN}	Differential Input Voltage Swing	IN, nIN		0.4		2	V
V_{CMR}	Common Mode Input Voltage[3]	IN, nIN		0.9		V_{CC} –V_{PP}/2	V
f_{OUT}	Output Frequency, Q[3:0]		N = ÷1			1000	MHz
			N = ÷2			500	MHz
			N = ÷4			250	MHz
			N = ÷8			125	MHz
f_{IN}	Input Frequency, IN, nIN					1000	MHz
*t*sk(o)	Output Skew[4, 5]				40	100	ps
t_{PD}	Propagation Delay		N = ÷1	200		600	ps
			N = ÷2, ÷4, ÷8	400		900	ps
*t*sk(pp)	Part-to-Part Skew[4, 6]					500	ps
t_R / t_F	Output Rise/Fall Time		10%-90%		270	410	ps
			20%-80%		150	220	ps
*t*jit(Ø)	Phase Jitter Noise Floor, >100kHz offset[7]		any Q, f_{OUT} = 1000MHz		-153		dBc/Hz
*t*jit(Ø)	Additive Phase Noise, RMS		122.88 MHz; 1kHz-40MHz		100	180	fs
			122.88 MHz; 12kHz-20MHz		60	120	fs
odc	Output Duty Cycle		50% Input Duty Cycle	45	50	55	%

NOTE 1: Outputs terminated with 50Ω to GND.

NOTE 2: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 3: Common mode input voltage is defined as the signal crosspoint.

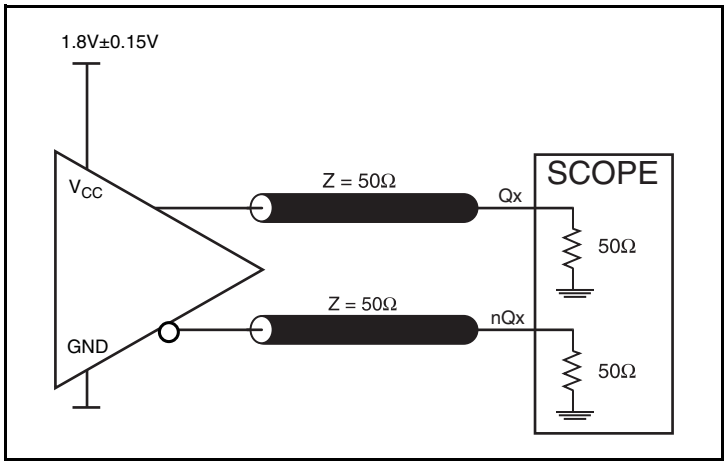
NOTE 4: This parameter is defined in accordance with JEDEC standard 65.

NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

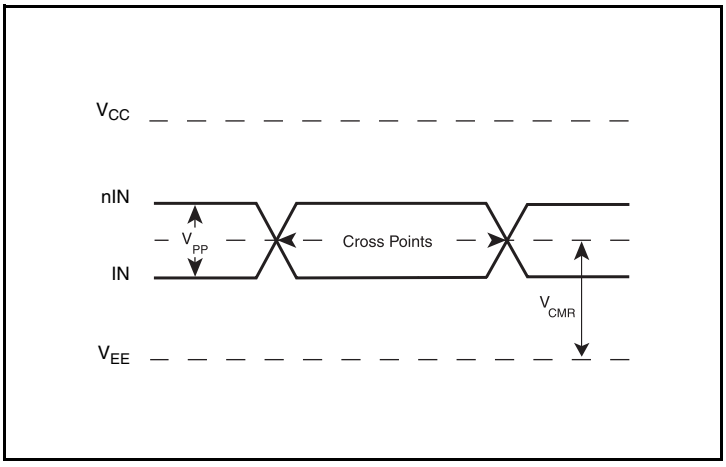
NOTE 6: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the output differential crosspoints.

NOTE 7: VCMR is set to 1.12V.

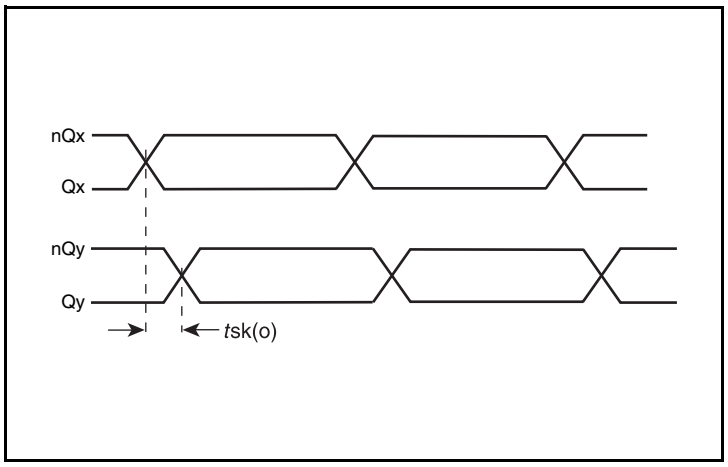
Parameter Measurement Information



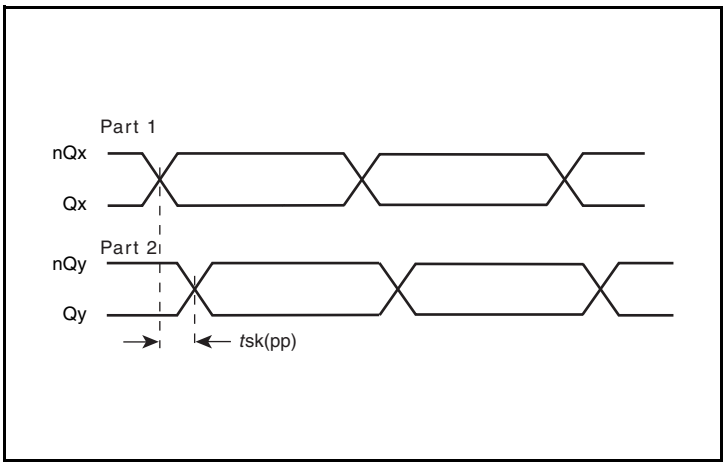
1.8V LVPECL Output Load Test Circuit



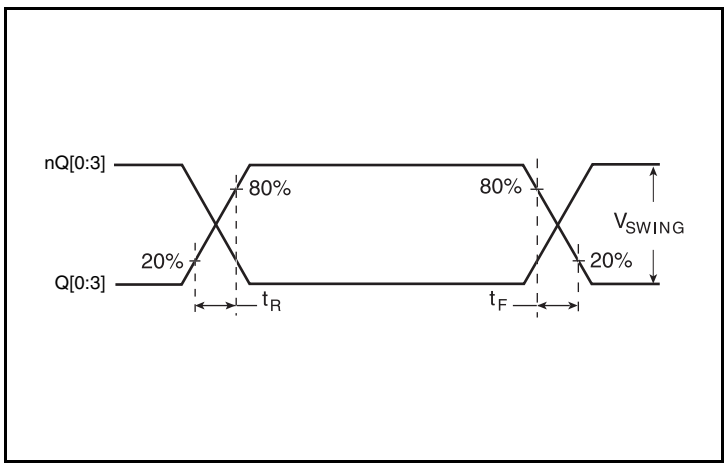
Differential Input Level



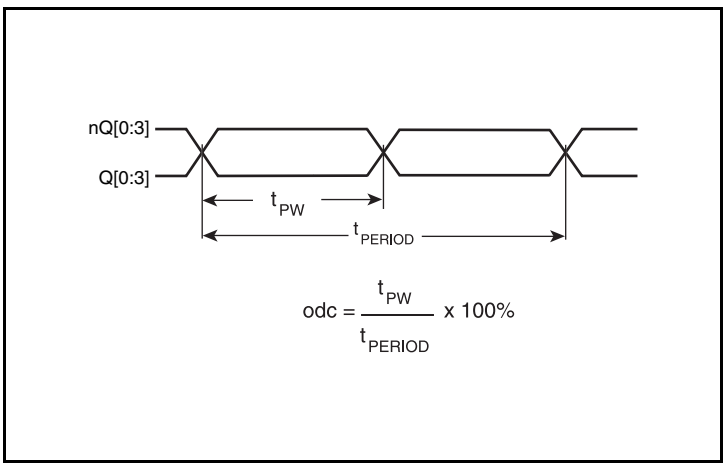
Output Skew



Part-to-Part Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 1*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

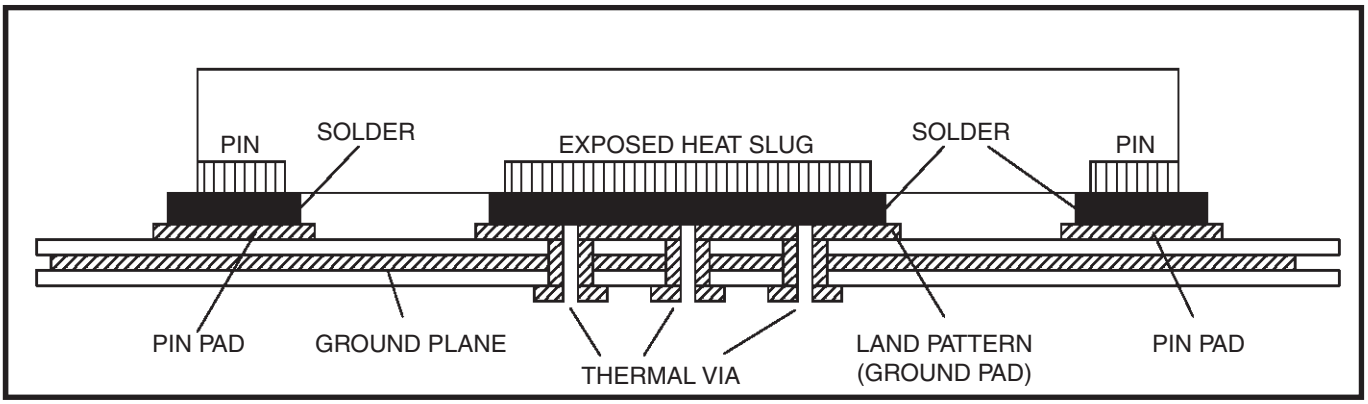


Figure 1. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

1.8V Differential Clock Input Interface

The IN /nIN accepts LVDS and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. *Figure 2A* to *Figure 2C* show interface examples for the IN /nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

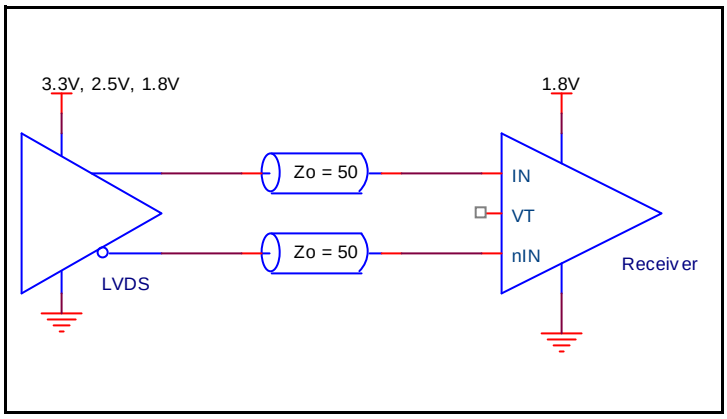


Figure 2A. Differential Input Driven by an LVDS Driver

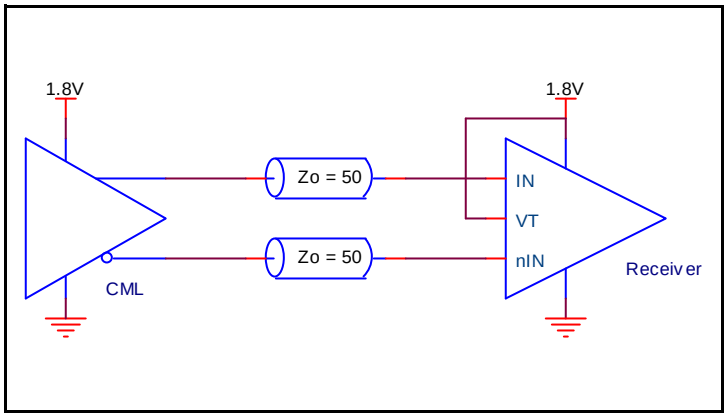


Figure 2B. Differential Input Driven by a CML Driver

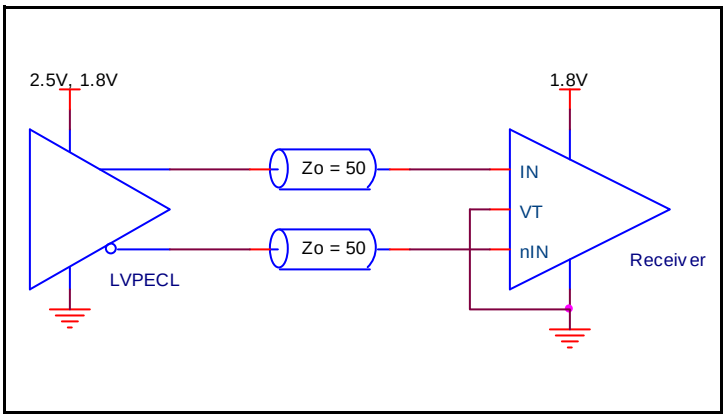


Figure 2C. Differential Input Driven by an LVPECL Driver

Power Considerations

This section provides information on power dissipation and junction temperature for the 8P73S674.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8P73S674 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 1.8V + 0.15V = 1.95V, which gives worst case results.

The following calculation is for 85°C. The maximum current at 85°C is 68.3mA.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{CC_MAX}$ = 1.95V * 68.3mA = **133.2mW**
- Power $(outputs)_{MAX}$ = **31.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 31.5mW = **126mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = 2 * [(I_{IN_MAX})^2 * 50\Omega] = 2 * (25mA)^2 * 50\Omega$ = **62.5mW**

Total Power$_{_MAX}$ = Power $(core)_{MAX}$ + Power $(outputs)_{MAX}$ + Power $(R_T)_{MAX}$ = 133.2+ 126mW + 62.5mW = **321.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 62.2°C/W per *Table 6* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.322W * 70.7°C/W = 108°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	70.7°C/W	67.0°C/W	65.3°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 3*.

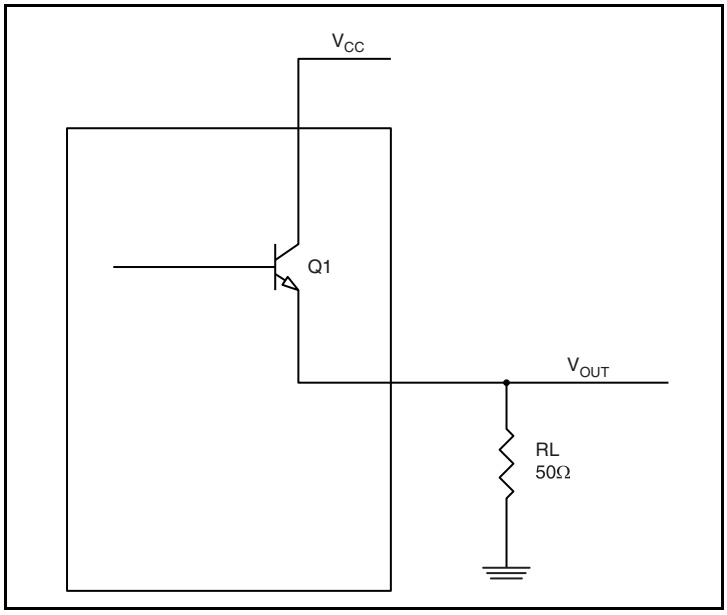


Figure 3. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} - 0.75V}$
  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} - 1.5V}$
  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX})/R_L] * (V_{CC_MAX} - V_{OH_MAX})$
$= [(V_{CC_MAX} - 0.75)/R_L] * (V_{CC_MAX} - V_{OH_MAX})$
$= [(1.95V - 0.75V)/50\Omega] * 0.75V =$ **18mW**

$Pd_L = [(V_{OL_MAX})/R_L] * (V_{CC_MAX} - V_{OL_MAX})$
$= [(V_{CC_MAX} - 1.5v)/R_L] * (V_{CC_MAX} - V_{OL_MAX})$
$= [(1.95V - 1.5V)/50\Omega] * 1.5V =$ **13.5mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.5mW**

Reliability Information

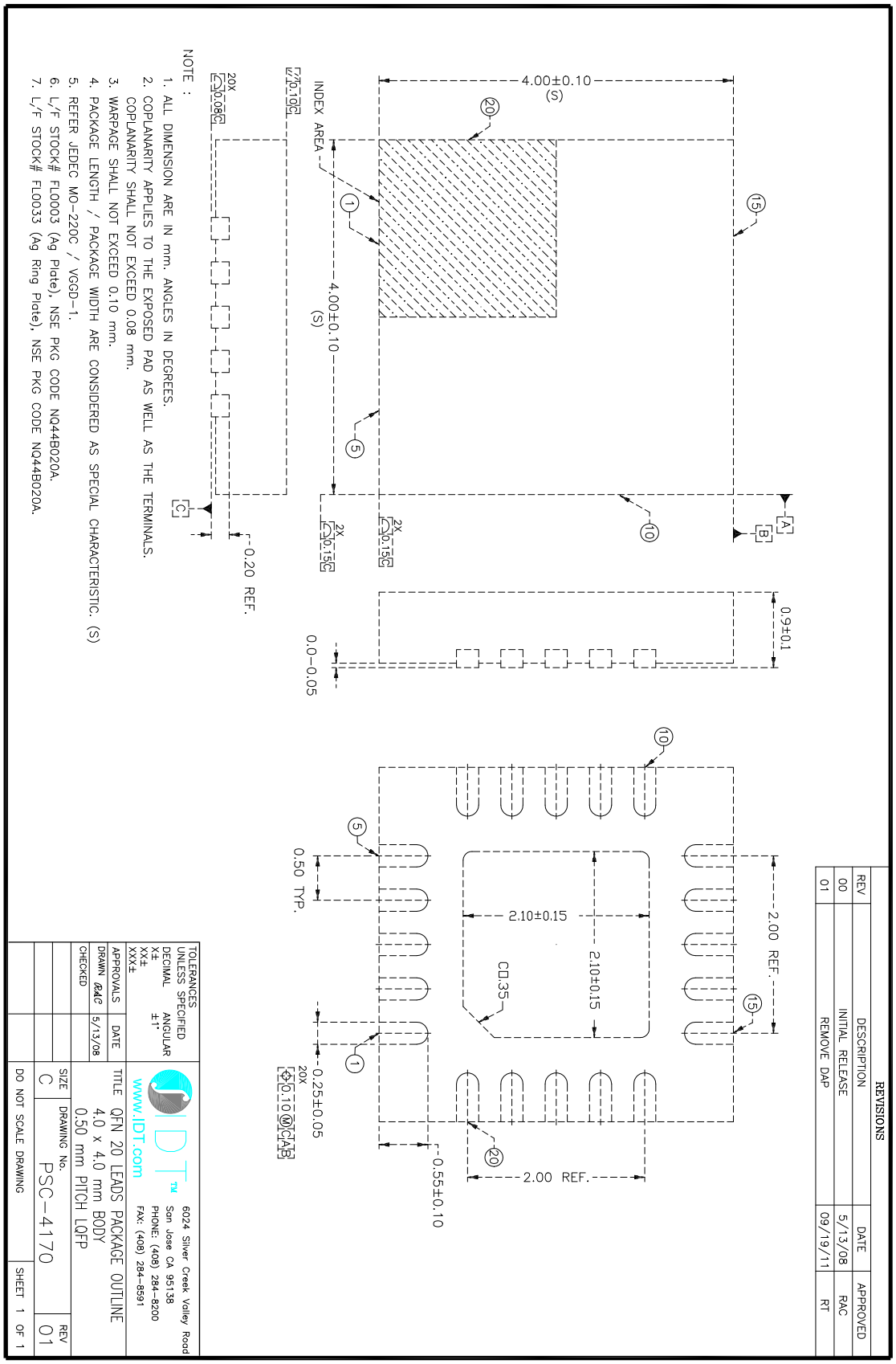
Table 7. θ_{JA} vs. Air Flow Table for a 20-Lead VFQFN

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	70.7°C/W	67.0°C/W	65.3°C/W

Transistor Count

The transistor count for the 8P73S674 is: 1,238

Package Information



Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8P73S674NLGI	8P73S674NLGI	20-Lead VFQFN, Lead-Free	Tray	-40°C to +85°C
8P73S674NLGI8	8P73S674NLGI	20-Lead VFQFN, Lead-Free	Tape & Reel	-40°C to +85°C



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