10-27GHz Bidirectionnal Detector

GaAs Monolithic Microwave IC

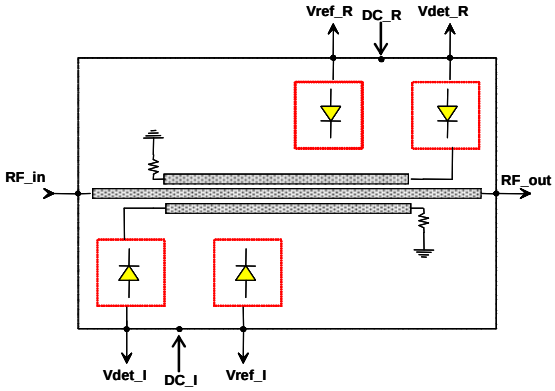
Description

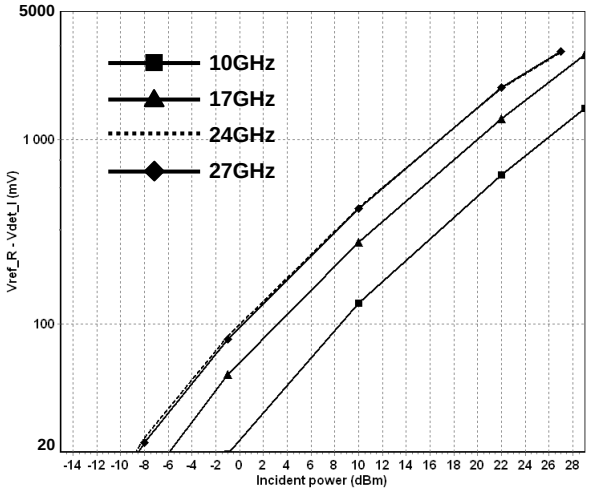
The CHE1260 is a bidirectionnal detector that integrates a passive bidirectionnal coupler, two matched detection diodes and two reference diodes.

It allows the measurement of transmitted and reflected power. It is designed for a wide range of applications where an accurate transmitted power control is required, typically commercial communication systems.

The circuit is manufactured with a Schottky diode MMIC process, 1µm gate length, via holes through the substrate and air bridges.

It is available in chip form.





Main Features

- Wide frequency range 10-27GHz
- Bidirectionnal detection
- 30dB dynamic range
- ESD protected
- Chip size: 1.41x1.41x0.1mm
- BCB layer protection

Main Characteristics

Tamb = +25°C, VDC = +4.5V (on DC_I and DC_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	10		27	GHz
IL	Insertion Loss		0.8		dB
Dr	Dynamic Range		20		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
Route Départementale 128 - B.P.46 - 91401 Orsay Cedex France
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Electrical Characteristics

Tamb = +25℃, VDC = +4.5V (on DC_I and DC_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	10		27	GHz
IL	Insertion Loss		0.8		dB
Cd	Coupler Directivity		13		dB
Dr	Dynamic Range : 10 - 12GHz 12 - 24GHz 24 - 27GHz		 22 20 15		 dB dB dB
Pd	Power detection: 10 - 17GHz 17 - 21GHz 21 - 24GHz 24 - 27GHz	 -1 -3 -6 -8			 dBm dBm dBm dBm
Vdetect_I	Voltage detection from transmitted power Vref_R – Vdet_I From Pd_min to Pd_max	20		3500	mV
Vdetect_R	Voltage detection from reflected power Vref_I – Vdet_R From Pd_min to Pd_max	20		3500	mV
RLin	Input return loss		-11	-8	dB
RLout	Output return loss		-11	-8	dB
VDC	Bias Voltage		4.5		V
IDC	Bias Current (on ports DC_I or DC_R)	25	33	45	µA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports but with 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes).

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter	Values	Unit
VDC	Bias voltage (on ports DC_I and DC_R)	6	V
Top	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃
P_max	Maximum power (for transmitted and/or reflected power)	30	dBm

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

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Typical on-wafer Sij parameters

Tamb = +25°C, Vdc = +4.5V (on DC_I and DC_R), 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes, page 8).

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S2 1)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
2	-32.9	54	-0.1	-13	-0.1	-13	-32.5	53
3	-30.0	52	-0.1	-20	-0.1	-20	-29.8	50
4	-27.7	50	-0.1	-27	-0.1	-27	-27.7	49
5	-25.8	47	-0.1	-33	-0.1	-33	-25.9	45
6	-24.1	42	-0.2	-40	-0.2	-40	-24.1	40
7	-22.6	36	-0.2	-46	-0.2	-46	-22.6	34
8	-21.3	31	-0.2	-53	-0.2	-53	-21.2	28
9	-20.0	25	-0.2	-60	-0.2	-60	-20.0	22
10	**-18.8**	**19**	**-0.3**	**-66**	**-0.2**	**-66**	**-18.8**	**17**
11	**-17.7**	**13**	**-0.3**	**-73**	**-0.3**	**-73**	**-17.7**	**10**
12	**-16.6**	**6**	**-0.3**	**-79**	**-0.3**	**-79**	**-16.6**	**4**
13	**-15.0**	**1**	**-0.4**	**-86**	**-0.4**	**-86**	**-15.0**	**-1**
14	**-14.2**	**-6**	**-0.4**	**-93**	**-0.4**	**-93**	**-14.3**	**-8**
15	**-13.6**	**-13**	**-0.5**	**-99**	**-0.5**	**-99**	**-13.5**	**-14**
16	**-12.9**	**-19**	**-0.5**	**-106**	**-0.5**	**-106**	**-12.8**	**-21**
17	**-12.3**	**-26**	**-0.5**	**-113**	**-0.5**	**-113**	**-12.2**	**-28**
18	**-11.8**	**-33**	**-0.6**	**-119**	**-0.6**	**-119**	**-11.8**	**-34**
19	**-11.4**	**-40**	**-0.6**	**-126**	**-0.6**	**-126**	**-11.3**	**-40**
20	**-11.0**	**-46**	**-0.7**	**-132**	**-0.7**	**-132**	**-11.0**	**-46**
21	**-10.7**	**-53**	**-0.7**	**-139**	**-0.7**	**-139**	**-10.6**	**-53**
22	**-10.5**	**-59**	**-0.8**	**-146**	**-0.8**	**-146**	**-10.4**	**-60**
23	**-10.4**	**-67**	**-0.8**	**-152**	**-0.8**	**-152**	**-10.2**	**-67**
24	**-10.8**	**-74**	**-0.9**	**-158**	**-0.9**	**-158**	**-10.5**	**-74**
25	**-10.9**	**-76**	**-0.9**	**-165**	**-0.9**	**-165**	**-10.8**	**-76**
26	**-10.7**	**-81**	**-0.9**	**-172**	**-0.9**	**-172**	**-10.8**	**-80**
27	**-11.0**	**-86**	**-0.9**	**-179**	**-0.9**	**-179**	**-10.8**	**-84**
28	-11.1	-90	-1.0	175	-1.0	175	-11.0	-89
29	-11.4	-95	-1.0	168	-0.9	168	-11.2	-93
30	-11.9	-100	-1.0	161	-1.0	161	-11.7	-97
31	-12.5	-104	-1.0	154	-1.0	154	-12.3	-101
32	-13.3	-108	-1.0	147	-1.0	147	-13.0	-103
33	-14.4	-108	-1.1	140	-1.1	140	-13.7	-105
34	-15.1	-104	-1.1	133	-1.1	133	-14.9	-103
35	-16.9	-108	-1.1	125	-1.1	125	-16.3	-104
36	-19.0	-99	-1.1	118	-1.1	118	-18.0	-92
37	-20.3	-79	-1.1	110	-1.1	110	-19.0	-74
38	-20.8	-51	-1.1	102	-1.1	102	-18.9	-51
39	-15.1	-34	-1.3	93	-1.3	93	-14.7	-38
40	-12.5	-33	-1.5	84	-1.5	84	-12.1	-36
41	-10.2	-37	-1.7	76	-1.7	76	-9.9	-37
42	-8.3	-41	-2.1	67	-2.0	67	-8.2	-42
43	-6.9	-47	-2.4	59	-2.4	59	-6.7	-47
44	-5.7	-53	-2.8	51	-2.8	51	-5.6	-52
45	-4.7	-59	-3.3	43	-3.3	43	-4.6	-57

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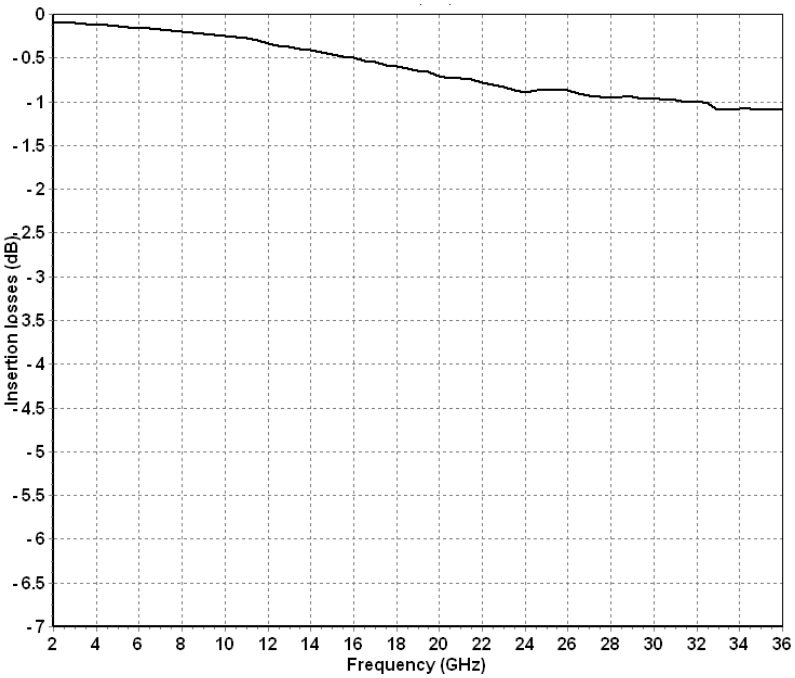
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Typical Measured Performance

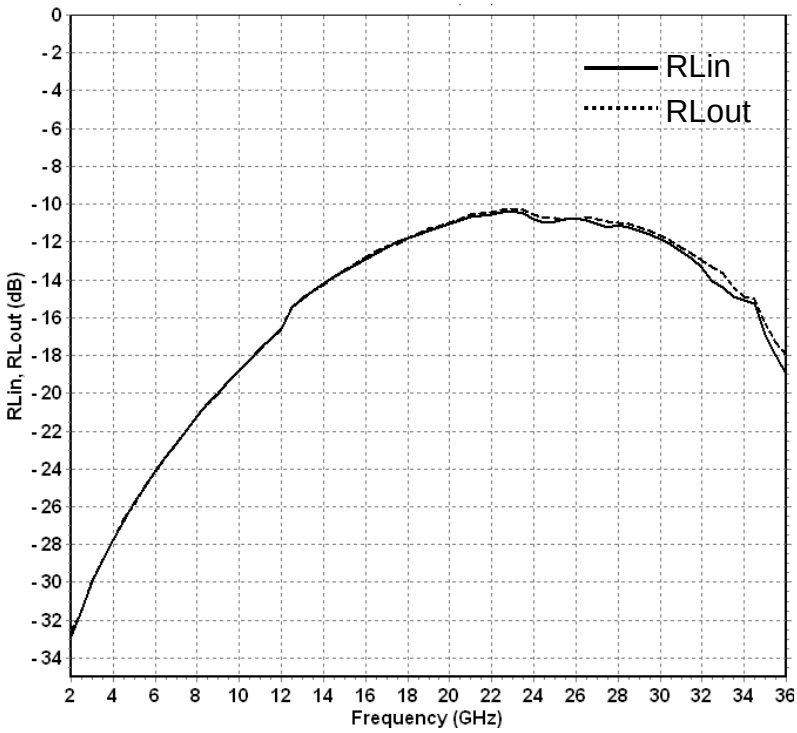
On-wafer measurements (without bonding wires at RF ports).

Tamb = +25℃, Vdc = +4.5V (on DC_I and DC_R), 100kΩ resistor in parallel on pads Vdet_I, Vref_I, Vdet_R and Vref_R (see notes, page 8).

Insertion losses versus frequency



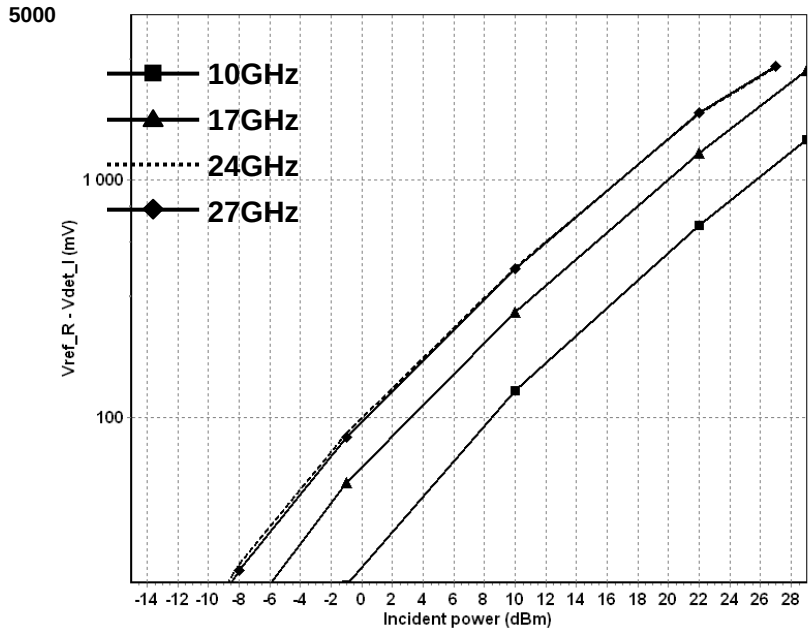
Input and output return losses versus frequency



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Incident power detection versus incident power @ different frequencies (Vdetect_I)



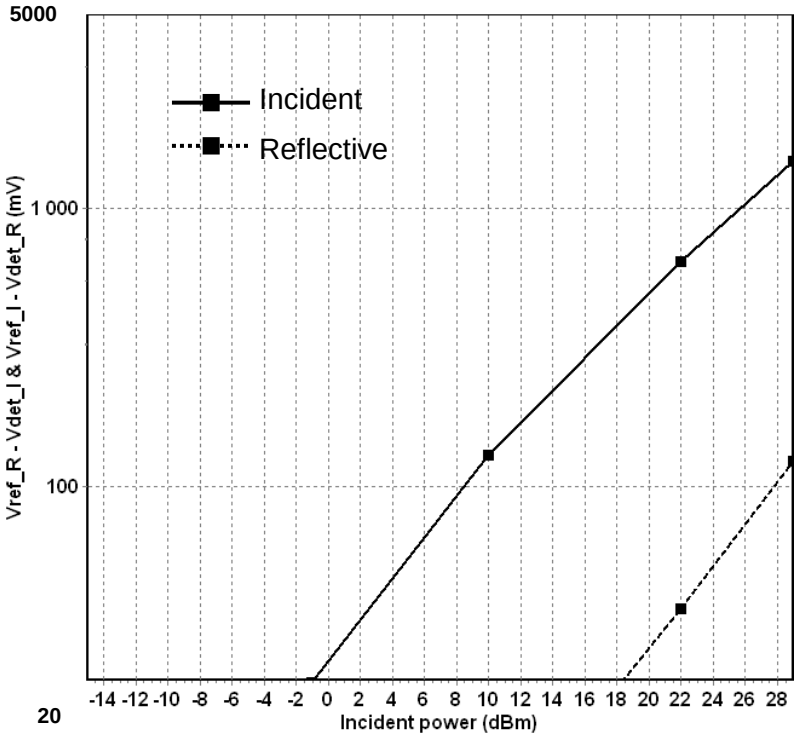
The CHE1260-98F is a bidirectionnal detector using a symmetrical bidirectionnal coupler. Therefore the incident power detection versus incident power is identical to the reflective power detection versus reflected power.

The reflective power detection versus incident power depends on both the coupler directivity and the reflective environment of the chip.

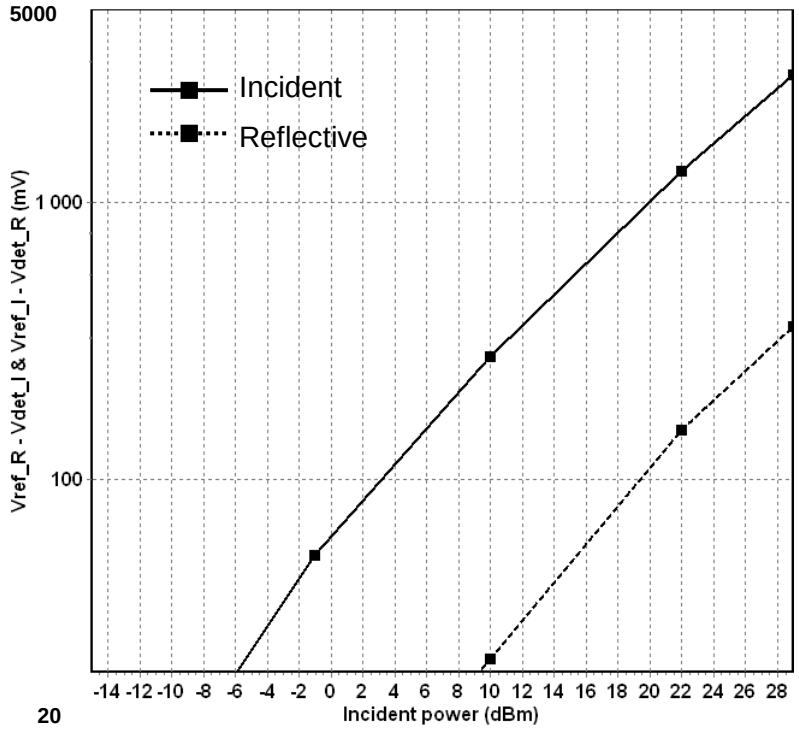
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Incident and reflected power detection versus incident power @ 10GHz (Vdetect_I & Vdetect_R)



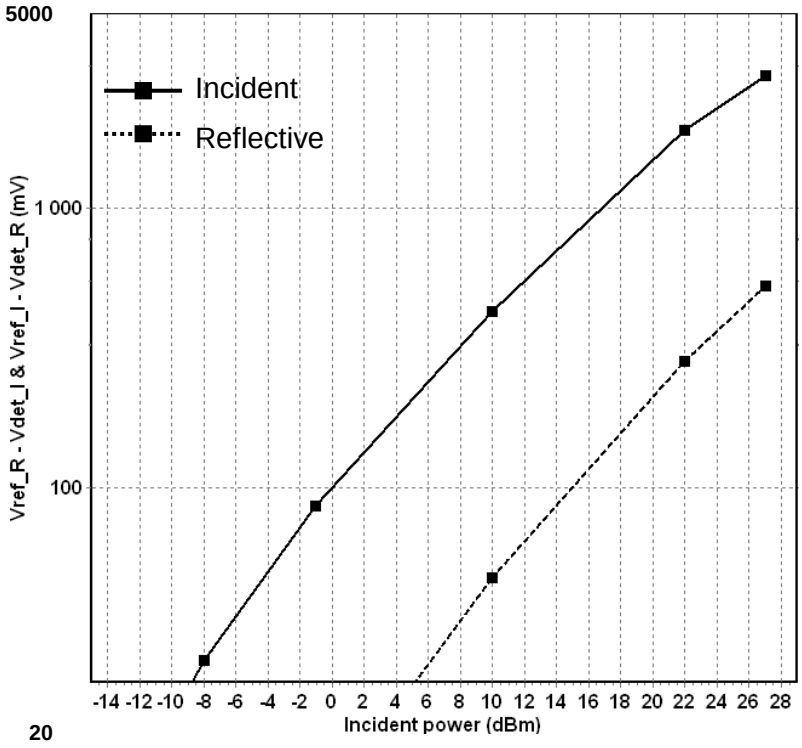
Incident and reflected power detection versus incident power @ 17GHz (Vdetect_I & Vdetect_R)



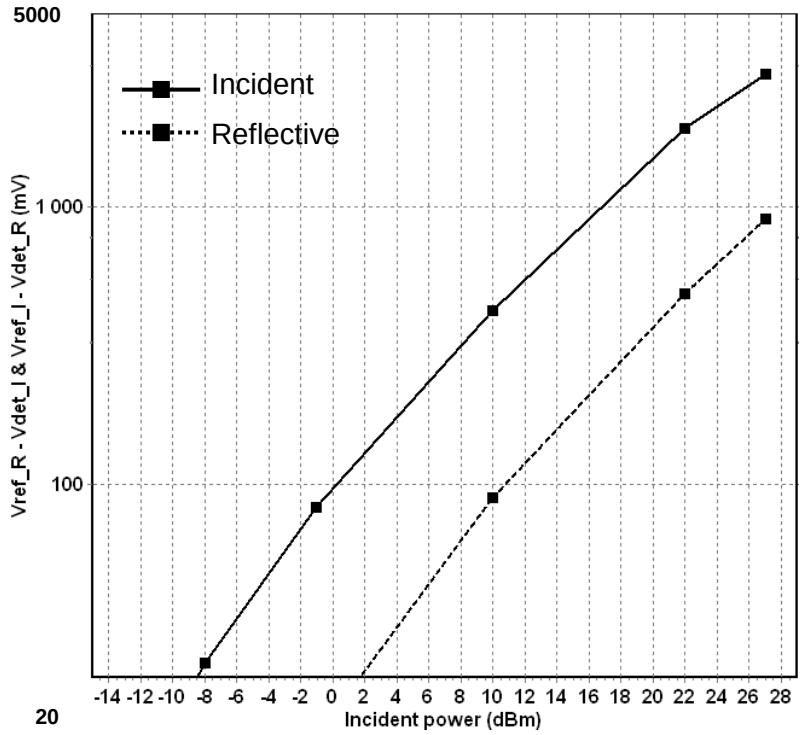
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Incident and reflected power detection versus incident power @ 24GHz (Vdetect_I & Vdetect_R)



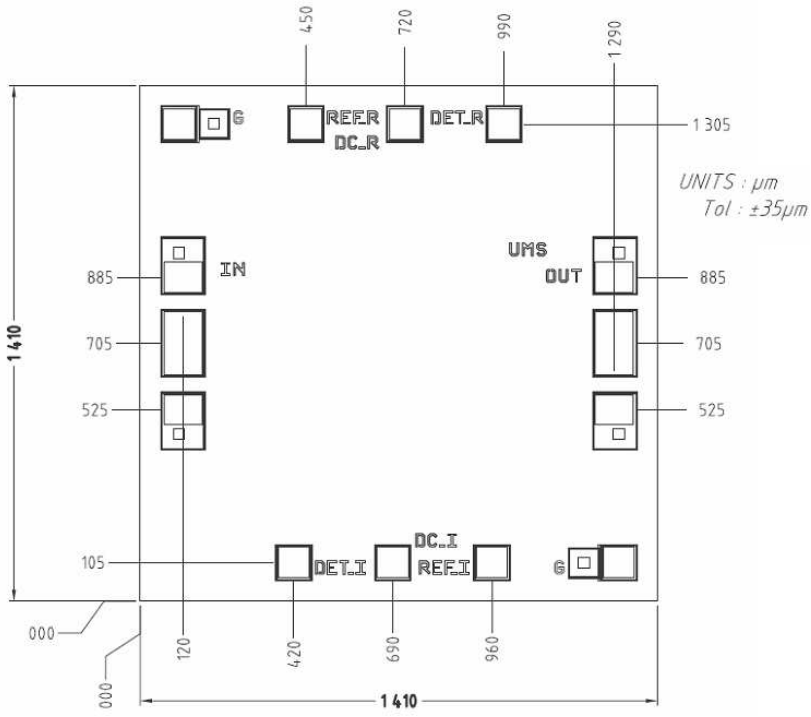
Incident and reflected power detection versus incident power @ 27GHz (Vdetect_I & Vdetect_R)



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Chip assembly and Mechanical data:



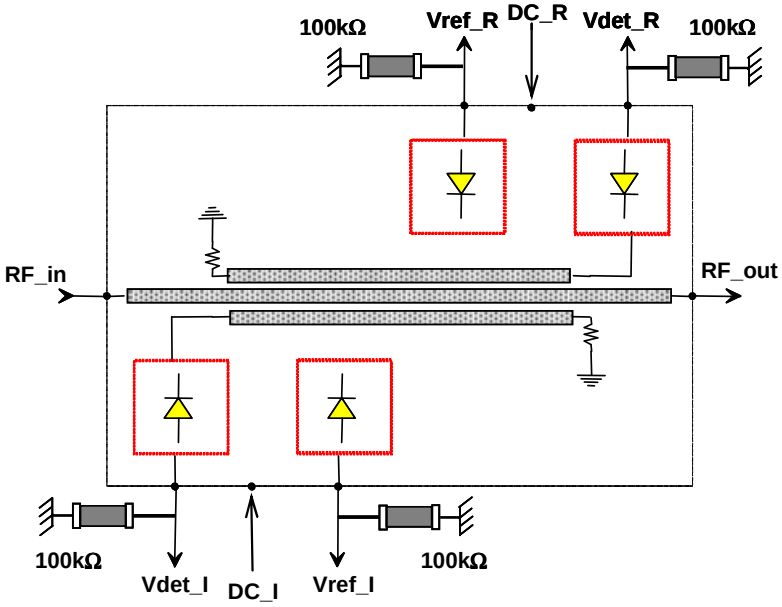
DC Pads Size: 100/100 µm, Chip thickness: 100 µm

Note: Supply feed might be capacitively bypassed. 25µm diameter gold wire is to be prefered.

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Notes



Recommended external resistors assembly

100kΩ resistors in parallel with Vdet_I, Vref_I, Vdet_R and Vref_R pads are recommended to provide the best behaviour in the whole operating temperature range.

Best accuracy is obtained when:

Vdetect_ I= Vref_R – Vdet_I
Vdetect_R= Vref_I – Vdet_R

As the voltage detection is the difference between Vref_X and Vdet_X (X= I or R), the external resistor value should be identical on these ports.
For information, a variation of 2% leads around 1mV variation of detected voltage.

ESD protections are implemented on Vdet_I, Vref_I, Vdet_R and Vref_R accesses.

Due to the BCB coating on the chip, qualification domain implies the chip must be glued.

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Ordering Information

Chip form: CHE1260-98F/00

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