CTLDM8002A-M621H

SURFACE MOUNT TLM™
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET





Top View



Bottom View

TLM621H CASE

MARKING CODE: CMA

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8002A-M621H is a very low profile (0.4mm) P-Channel enhancement-mode MOSFET in a small, thermal efficient, 1.5mm x 2mm TLM™ package.

FEATURES:

- Low $R_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small, Very Low Profile, **TLM™**

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS (T_A=25°C)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage	V_{DG}	50	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current	I_D	280	mA
Continuous Source Current (Body Diode)	I_S	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Maximum Pulsed Source Current	I_{SM}	1.5	A
Power Dissipation (Note 1)	P_D	1.6	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	75	°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}	V_{GS}=20V, V_{DS}=0V		100	nA
I_{GSSR}	V_{GS}=20V, V_{DS}=0V		100	nA
I_{DSS}	V_{DS}=50V, V_{GS}=0V		1.0	μA
I_{DSS}	V_{DS}=50V, V_{GS}=0V, T_j=125°C		500	μA
$I_{D(ON)}$	V_{GS}=10V, V_{DS}=10V	500		mA
BV_{DSS}	V_{GS}=0V, I_D=10μA	50		V

Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

PRELIMINARY

Central™
Semiconductor Corp.

PRELIMINARY

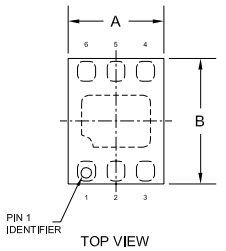
CTLDM8002A-M621H

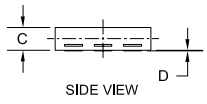
SURFACE MOUNT TLM™
P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET

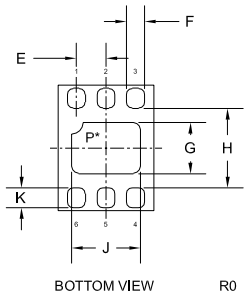
ELECTRICAL CHARACTERISTICS - Continued (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	2.5	V
$V_{DS(ON)}$	V_{GS}=10V, I_D=500mA		1.5	V
$V_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		0.15	V
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA		2.5	Ω
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA, T_j=125°C		4.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		3.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA, T_j=125°C		5.0	Ω
Y_{fs}	V_{DS} =10V, I_D=200mA	200		msec
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		7.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		70	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		15	pF
t_{on}	V_{DD}=30V, V_{GS}=10V, I_D=200mA		20	ns
t_{off}	R_G=25Ω, R_L=150Ω		20	ns
V_{SD}	V_{GS}=0V, I_S=115mA		1.3	V

TLM621H CASE - MECHANICAL OUTLINE







* Exposed pad P Internally connected to pins 3 and 4

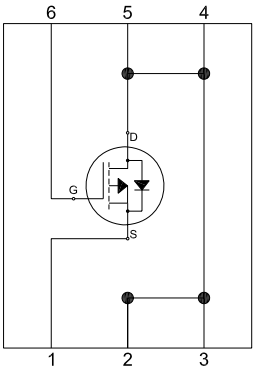
DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

TLM621H (REV:R0)

LEAD CODE:
1) SOURCE
2) DRAIN
3) DRAIN
4) DRAIN
5) DRAIN
6) GATE

MARKING CODE: CMA

PIN CONFIGURATION:



R0 (15-June 2006)