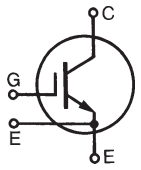
IXYS

Preliminary Technical Information

High Voltage IGBT IXGN100N170

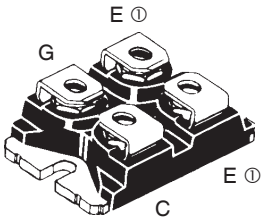
V_{CES} = 1700V
I_{C90} = 95A
$V_{CE(sat)}$ ≤ 3.0V



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1700	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1700	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	160	A
I_{C90}	T_C = 90°C	95	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA	V_{GE}= 15V, T_{VJ} = 125°C, R_G = 1Ω	I_{CM} = 200	A
(RBSOA)	Clamped inductive load @ 0.8 • V_{CES}		
t_{sc}	V_{GE}= 15V, V_{CE} = 1250V, T_J = 125°C	10	µs
(SCSOA)	R_G = 10Ω, non repetitive		
P_C	T_C = 25°C	735	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
V_{ISOL}	50/60Hz t = 1min	2500	V~
	I_{ISOL} ≤ 1mA t = 1s	3000	V~
M_d	Mounting torque	1.5/13	Nm/lb.in.
	Terminal connection torque (M4)	1.3/11.5	Nm/lb.in.
Weight		30	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 3mA, V_{GE} = 0V	1700			V
$V_{GE(th)}$	I_C = 8mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}			50	µA
	V_{GE} = 0V T_J = 125°C			5	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	I_C = 100A, V_{GE} = 15V, Note 1		2.5	3.0	V

SOT-227B, miniBLOC
E153432



G = Gate, C = Collector, E = Emitter
① either emitter terminal can be used as Main or Kelvin Emitter

Features

- Optimized for low conduction and switching losses
- Square RBSOA
- Isolation voltage 3000 V~
- High current handling capability
- International standard package

Advantages

- High power density
- Low gate drive requirement

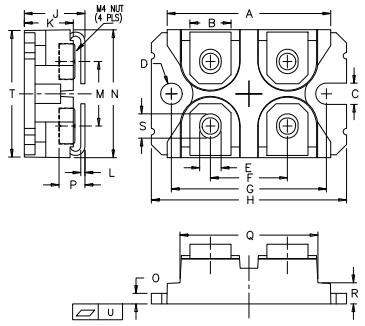
Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Welding Machines

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Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 60A, V_{CE} = 10V, Note 1	36	64	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0 V, f = 1MHz		9220	pF
C_{oes}			455	pF
C_{res}			150	pF
$Q_{g(on)}$	I_C = 100A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		425	nC
Q_{ge}			65	nC
Q_{gc}			186	nC
$t_{d(on)}$	**Resistive load, T_J = 25°C**		35	ns
t_{ri}	I_C = 100A, V_{GE} = 15V		192	ns
$t_{d(off)}$	V_{CE} = 0.5 • V_{CES}, R_G = 1Ω		285	ns
t_{fi}			395	ns
$t_{d(on)}$	**Resistive load, T_J = 125°C**		35	ns
t_{ri}	I_C = 100A, V_{GE} = 15V		250	ns
$t_{d(off)}$	V_{CE} = 0.5 • V_{CES}, R_G = 1Ω		285	ns
t_{fi}			435	ns
R_{thJC}				0.17 °C/W
R_{thCK}			0.05	°C/W

SOT-227B miniBLOC (IXGN)



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.240	1.255	31.50	31.88
B	.307	.323	7.80	8.20
C	.161	.169	4.09	4.29
D	.161	.169	4.09	4.29
E	.161	.169	4.09	4.29
F	.587	.595	14.91	15.11
G	1.186	1.193	30.12	30.30
H	1.496	1.505	38.00	38.23
J	.460	.481	11.68	12.22
K	.351	.378	8.92	9.60
L	.030	.033	0.76	0.84
M	.496	.506	12.60	12.85
N	.990	1.001	25.15	25.42
O	.078	.084	1.98	2.13
P	.195	.235	4.95	5.97
Q	1.045	1.059	26.54	26.90
R	.155	.174	3.94	4.42
S	.186	.191	4.72	4.85
T	.968	.987	24.59	25.07
U	-.002	.004	-0.05	0.1

Note: 1. Pulse test, t ≤ 300µs; duty cycle, d ≤ 2%.

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25ºC

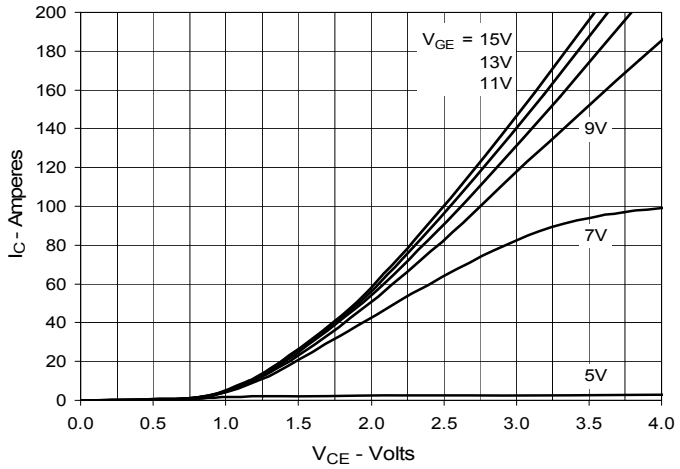


Fig. 2. Extended Output Characteristics @ 25ºC

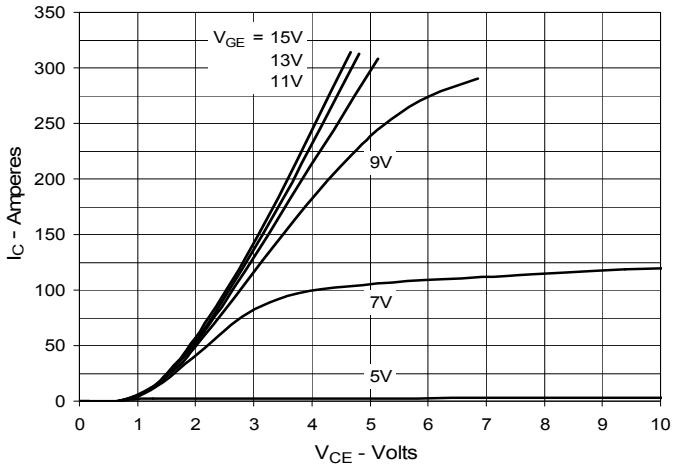


Fig. 3. Output Characteristics @ 125ºC

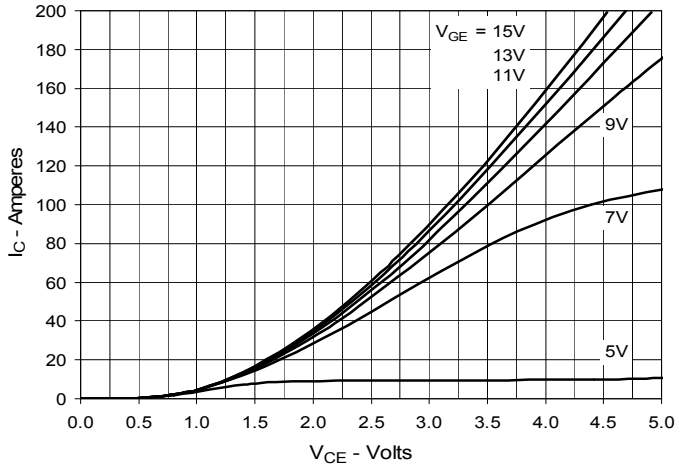


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

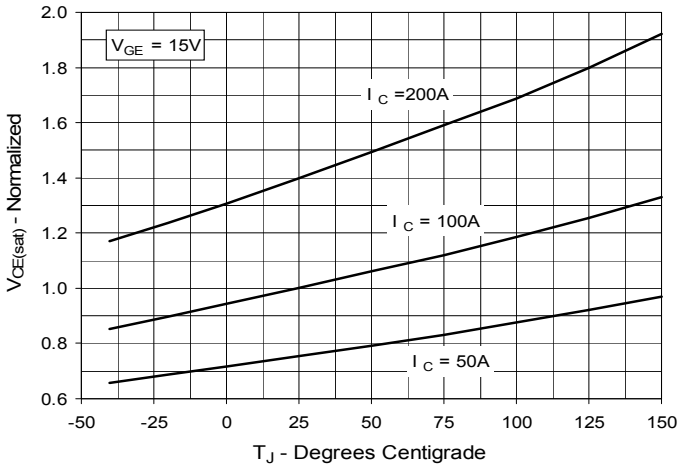


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

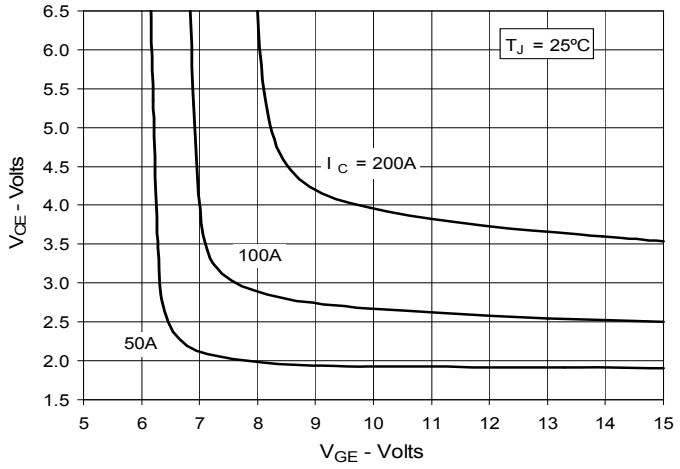
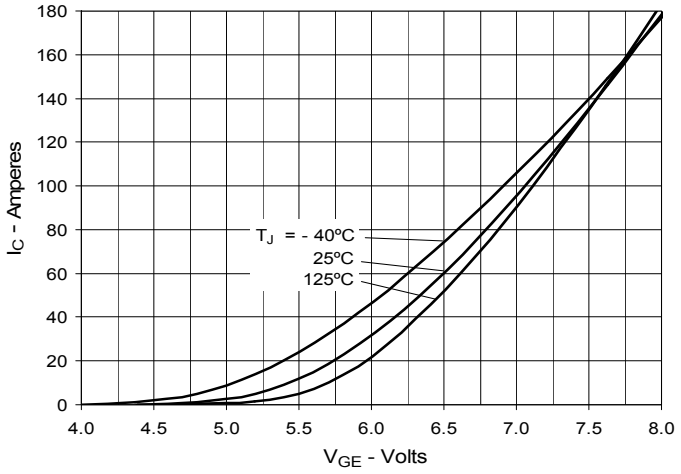


Fig. 6. Input Admittance



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Fig. 7. Transconductance

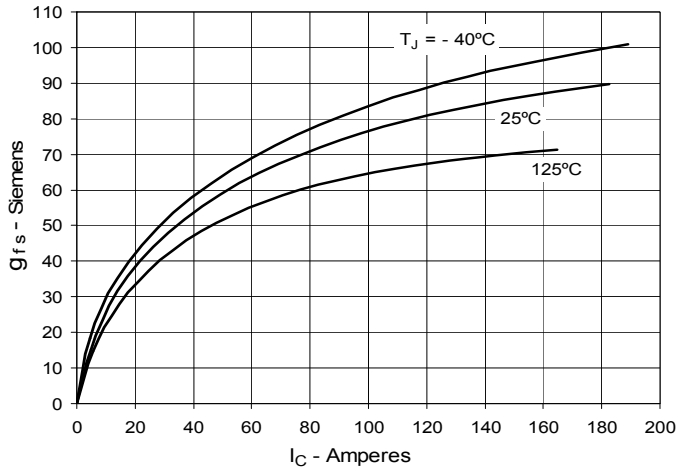


Fig. 8. Gate Charge

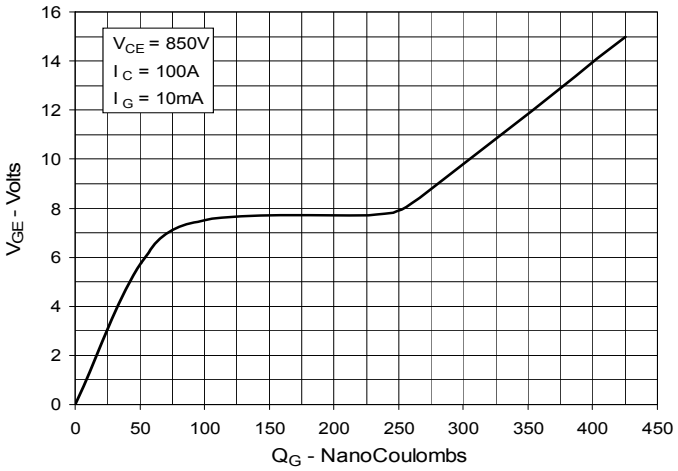


Fig. 9. Reverse-Bias Safe Operating Area

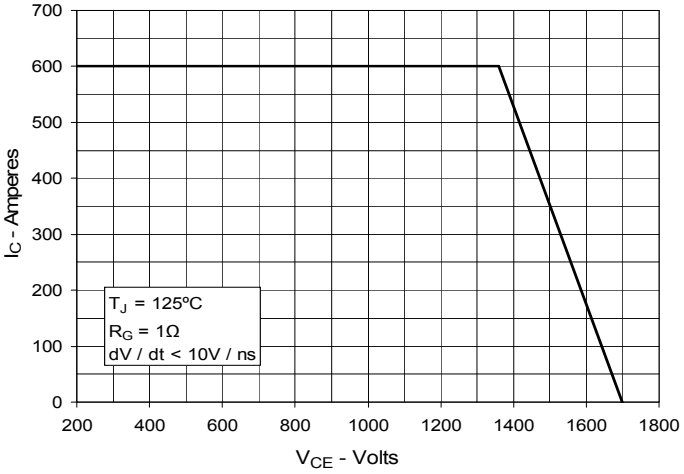


Fig. 10. Capacitance

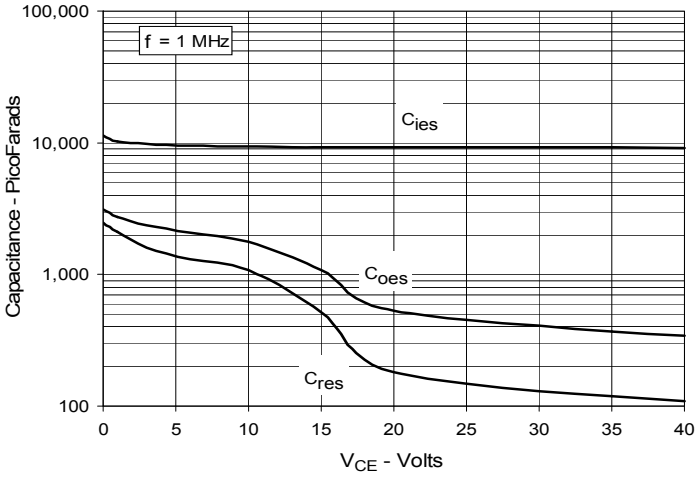
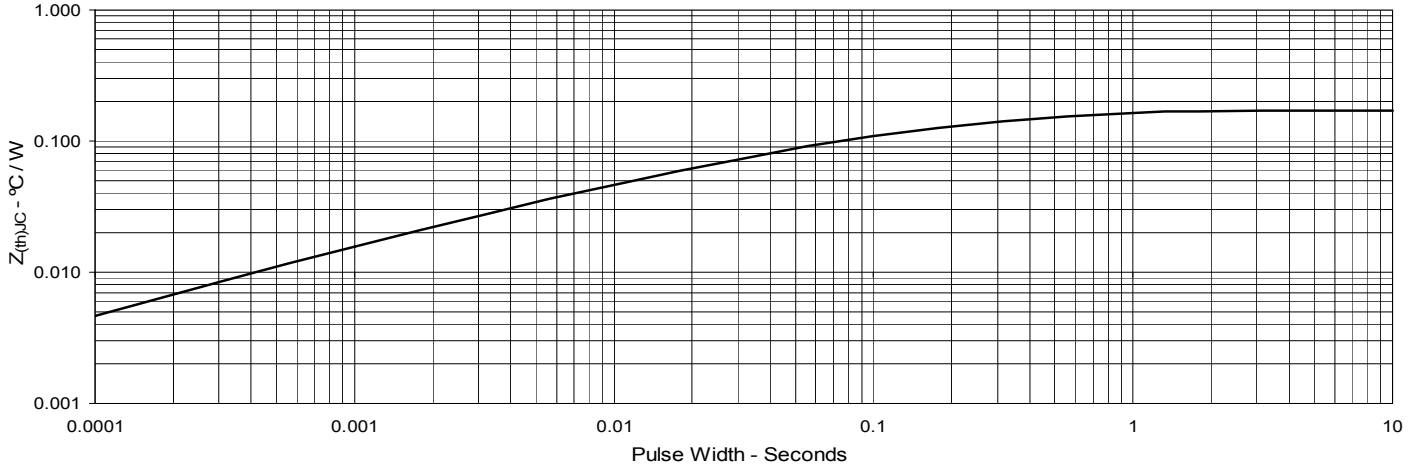


Fig. 11. Maximum Transient Thermal Impedance



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Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

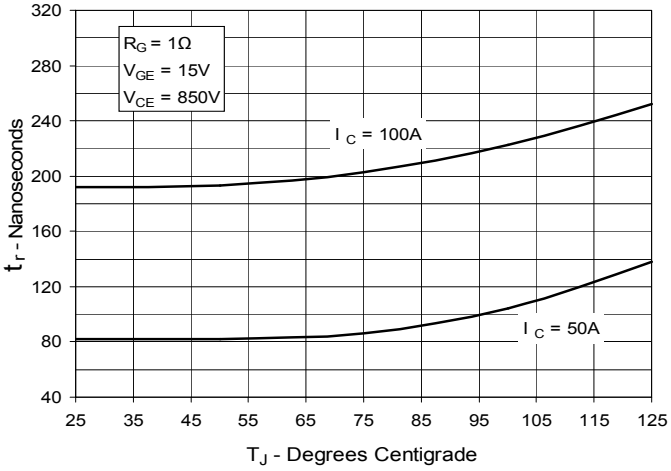


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

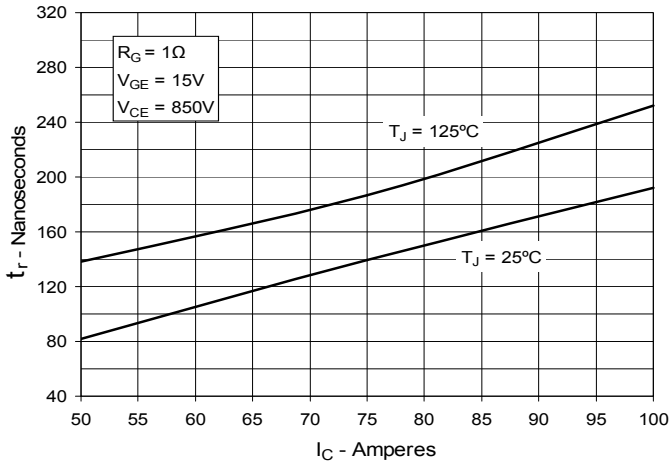


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

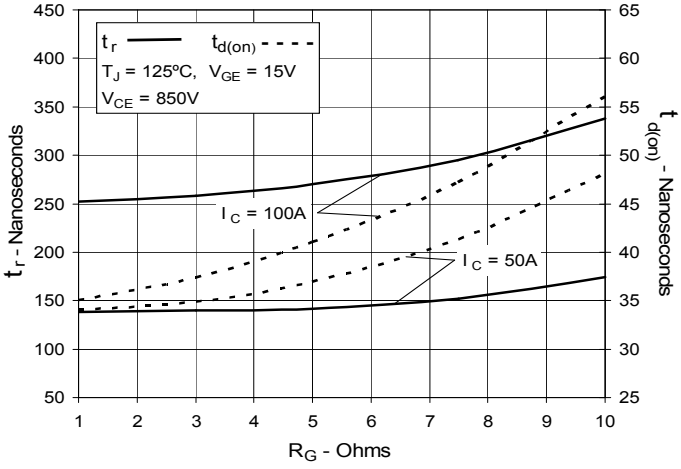


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

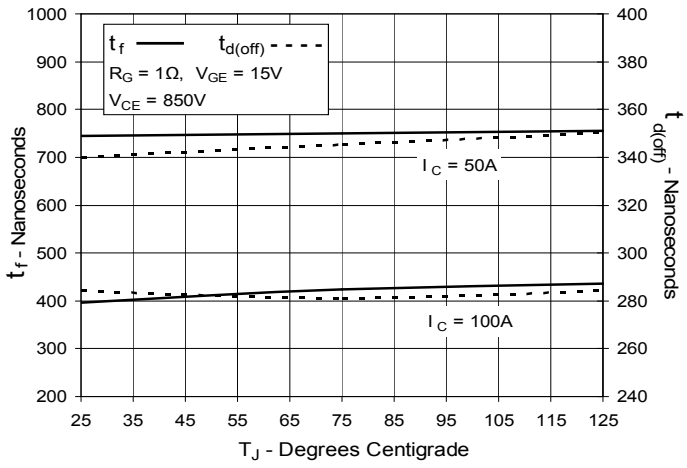


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

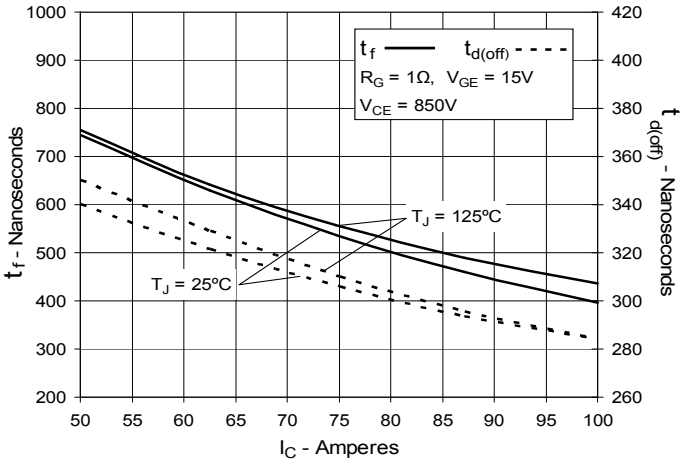
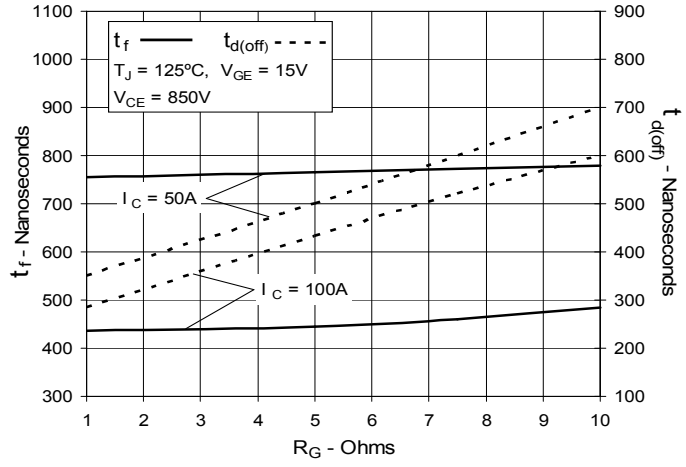


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance



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