

TISP8200HDM BUFFERED P-GATE SCR DUAL
TISP8201HDM BUFFERED N-GATE SCR DUAL

COMPLEMENTARY BUFFERED-GATE SCRS FOR DUAL POLARITY SLIC OVERVOLTAGE PROTECTION

TISP820xHDM Overvoltage Protectors

High Performance Protection for SLICs with +ve & -ve Battery Supplies

TISP8200HDM Negative Overvoltage Protector
– Wide -20 to -110 V Programming Range
– Low +15 mA Max. Gate Triggering Current
– High -150 mA Min. Holding Current

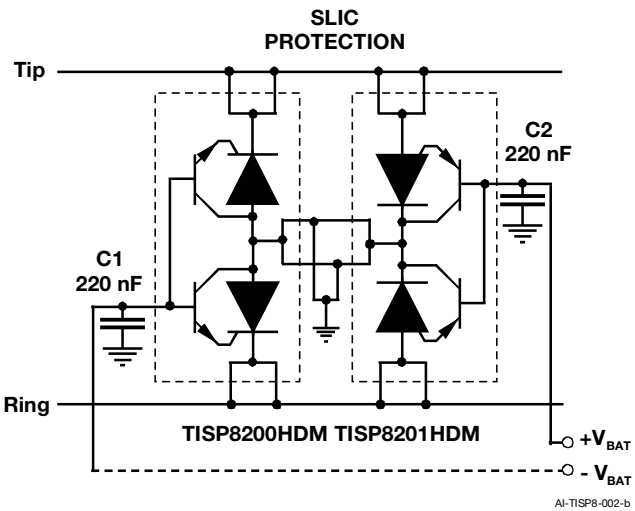
TISP8201HDM Positive Overvoltage Protector
– Wide +20 to +110 V Programming Range
– Low -15 mA Max. Gate Triggering Current
– +20 mA Min. Holding Current

Rated for International Surge Wave Shapes

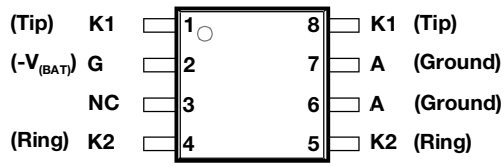
Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	500
10/700	ITU-T K.20/21/45	150
10/1000	GR-1089-CORE	100

.....UL Recognized Component

Circuit Application Diagram



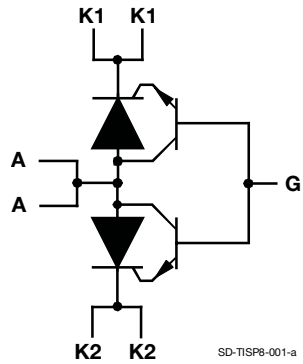
TISP8200HDM 8-SOIC (210 mil) Package (Top View)



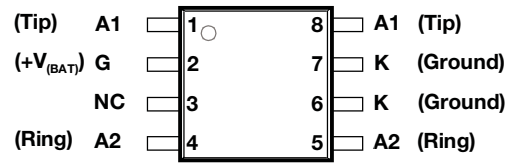
NC - No internal connection
Terminal typical application names shown in parenthesis

MD-8SOIC(210)-007-a

TISP8200HDM Device Symbol



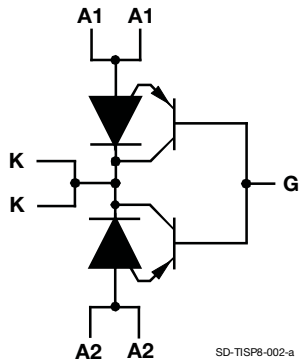
TISP8201HDM 8-SOIC (210 mil) Package (Top View)



NC - No internal connection
Terminal typical application names shown in parenthesis

MD-8SOIC(210)-008-a

TISP8201HDM Device Symbol



*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
OCTOBER 2005 — REVISED MAY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Description

The TISP8200HDM/TISP8201HDM combination has been designed to protect dual polarity supply rail monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. Protection against negative overvoltages is given by the TISP8200HDM. Protection against positive overvoltages is given by the TISP8201HDM. Both parts are in 8-SOIC (210 mil) surface mount packages.

The TISP8200HDM has an array of two buffered P-gate SCRs with a common anode connection. Each SCR cathode and gate has a separate terminal connection. The NPN buffer transistors reduce the gate supply current. In use, the cathodes of the TISP8200HDM SCRs are connected to the two conductors of the POTS line. The gates are connected to the appropriate negative voltage battery feed of the SLIC driving the line conductor pair, so that the TISP8200HDM protection voltage tracks the SLIC negative supply voltage. The anode of the TISP8200HDM is connected to the SLIC common. Negative overvoltages are initially clipped close to the SLIC negative supply by emitter follower action of the NPN buffer transistor. If sufficient clipping current flows, the SCR will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of the SCR helps prevent d.c. latchup.

The TISP8201HDM has an array of two buffered N-gate SCRs with a common cathode connection. Each SCR anode and gate has a separate terminal connection. The PNP buffer transistors reduce the gate supply current. In use, the anodes of the TISP8201HDM SCRs are connected to the two conductors of the POTS line. The gates are connected to the appropriate positive voltage battery feed of the SLIC driving that line pair, so that the TISP8201HDM protection voltage tracks the SLIC positive supply voltage. The cathode of the TISP8201HDM is connected to the SLIC common. Positive overvoltages are initially clipped close to the SLIC positive supply by emitter follower action of the PNP buffer transistor. If sufficient clipping current flows the SCR will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides the SLIC pulls the conductor voltage down to its normal negative value and this commutates the conducting SCR into a reverse biased condition.

How to Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP8200HDM	8-SOIC (210 mil)	Embossed Tape Reeled	TISP8200HDMR-S	8200H	2000
TISP8201HDM			TISP8201HDMR-S	8201H	

TISP8200HDM Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0	V_{DRM}	-120	V
Repetitive peak reverse voltage, V_{GA} = -70 V	V_{RRM}	120	
Non-repetitive peak impulse current (see Notes 1, 2 and 3) 2/10 µs (Telcordia GR-1089-CORE, 2/10 µs voltage wave shape) 5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45) 10/1000 µs (Telcordia GR-1089-CORE, 10/1000 µs voltage wave shape)	I_{PPSM}	 -500 -150 -100	A
Non-repetitive peak on-state current, 50/60 Hz (see Notes 1, 2, 3 and 4) 10 ms 1 s 7 s 900 s	I_{TSM}	 60 14 7 3.5	A
Junction temperature	T_J	-55 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values. The rated current values may be applied to any cathode-anode terminal pair.
3. Rated currents only apply if pins 1 & 8 (K1,Tip) are connected together, pins 4 & 5 (K2, Ring) are connected together and pins 6 & 7 (A, Ground) are connected together.
4. These non-repetitive rated terminal currents are for the TISP8200HDM and TISP8201HDM together. Device (A)-terminal positive current values are conducted by the TISP8201HDM and (K)-terminal negative current values by the TISP8200HDM.

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TISP8201HDM Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GA} = 0	V_{DRM}	120	V
Repetitive peak reverse voltage, V_{GK} = 70 V	V_{RRM}	-120	
Non-repetitive peak impulse current (see Notes 5, 6 and 7)			
2/10 µs (Telcordia GR-1089-CORE, 2/10 µs voltage wave shape)	I_{PPSM}	500	A
5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45)		150	
10/1000 µs (Telcordia GR-1089-CORE, 10/1000 µs voltage wave shape)		100	
Non-repetitive peak on-state current, 50/60 Hz (see Notes 5, 6, 7 and 8)			
10 ms	I_{TSM}	60	A
1 s		14	
7 s		7	
900 s		3.5	
Junction temperature	T_J	-55 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 5. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.

6. These non-repetitive rated currents are peak values. The rated current values may be applied to any cathode-anode terminal pair.
7. Rated currents only apply if pins 1 & 8 (A1, Tip) are connected together, pins 4 & 5 (A2, Ring) are connected together and pins 6 & 7 (K, Ground) are connected together.
8. These non-repetitive rated terminal currents are for the TISP8200HDM and TISP8201HDM together. Device (A)-terminal positive current values are conducted by the TISP8201HDM and (K)-terminal negative current values by the TISP8200HDM.

Recommended Operating Conditions

See Figure 3	Min	Typ	Max	Unit
C1, C2 Gate decoupling capacitor		220		nF

TISP8200HDM Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$, V_{GK} = 0				-5	µA
I_{RRM}	Repetitive peak reverse current	$V_R = V_{RRM}$, V_{GA} = -70 V				5	µA
$V_{(BO)}$	Breakover voltage	dv/dt = -250 V/ms, R_{SOURCE} = 300 Ω, V_{GA} = -80 V				-82	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ -1000 V/µs, Linear voltage ramp, Maximum ramp value = -500 V di/dt = -20 A/µs, Linear current ramp, Maximum ramp value = -10 A V_{GA} = -80 V				-90	V
I_H	Holding current	(I_K) I_T = -1 A, di/dt = 1 A/ms, V_{GA} = -80 V		-150			mA
I_{GT}	Gate trigger current	(I_K) I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{GA} = -80 V				15	mA
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, Gate open	V_D = -2 V			65	pF
			V_D = -50 V			30	

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TISP8201HDM Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$, $V_{GA} = 0$				5	µA
I_{RRM}	Repetitive peak reverse current	$V_R = V_{RRM}$, $V_{GK} = 70$ V				-5	µA
$V_{(BO)}$	Breakover voltage	dv/dt = 250 V/ms, R_{SOURCE} = 300 Ω, V_{GK} = 80 V				82	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ 1000 V/µs, Linear voltage ramp, Maximum ramp value = 500 V di/dt = 20 A/µs, Linear current ramp, Maximum ramp value = 10 A V_{GK} = 80 V				90	V
I_H	Holding current	(I_A) I_T = 1 A, di/dt = -1 A/ms, V_{GK} = 80 V		20			mA
I_{GT}	Gate trigger current	(I_A) I_T = 5 A, $t_{p(g)}$ ≥ 20 µs, V_{GK} = 80 V				-15	mA
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, Gate open	V_D = 2 V			50	pF
			V_D = 50 V			30	

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-7 PCB, EIA/JESD51-2 Environment, P_{TOT} = 4 W (See Note 9)		55		°C/W

NOTE 9. EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

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Parameter Measurement Information

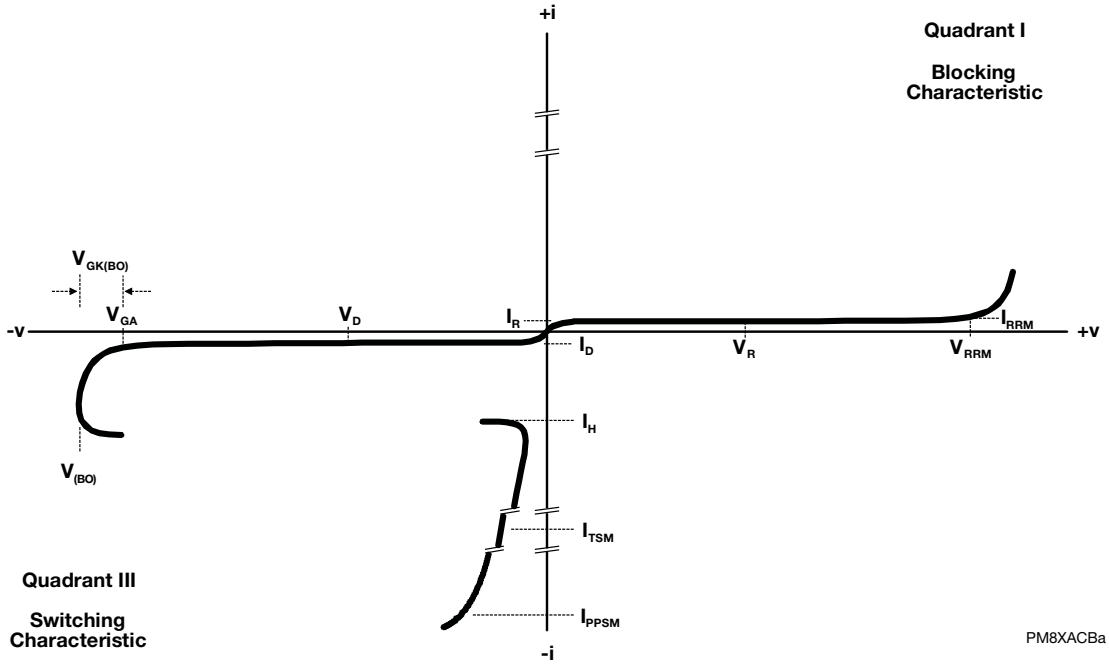


Figure 1. TISP8200HDM KA Terminal Characteristic

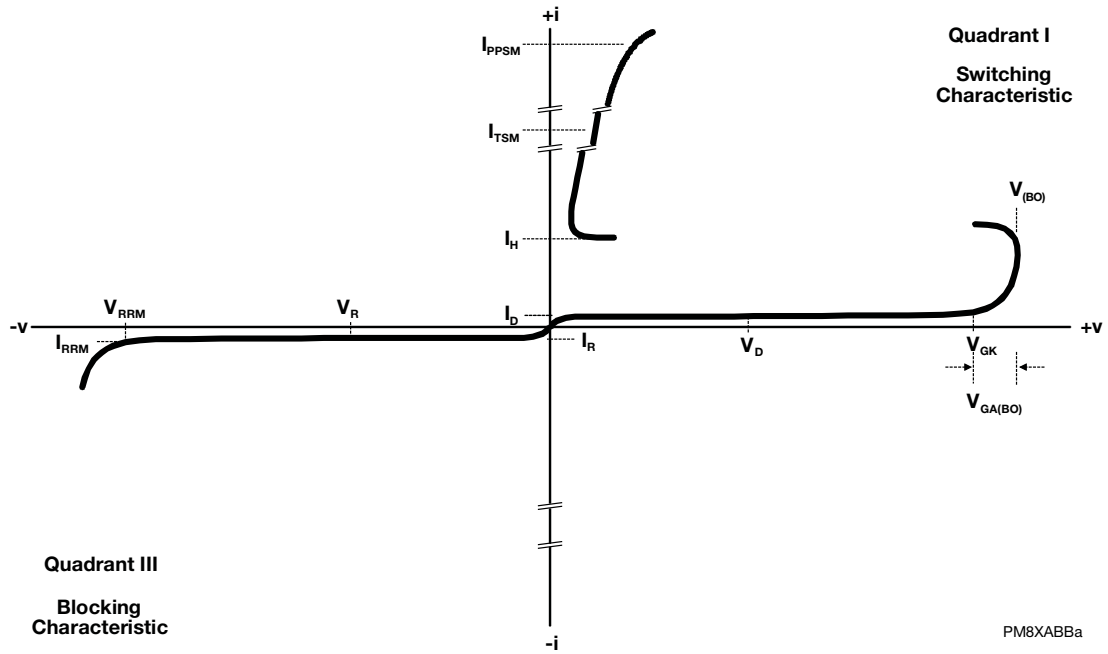


Figure 2. TISP8201HDM AK Terminal Characteristic

Applications Information

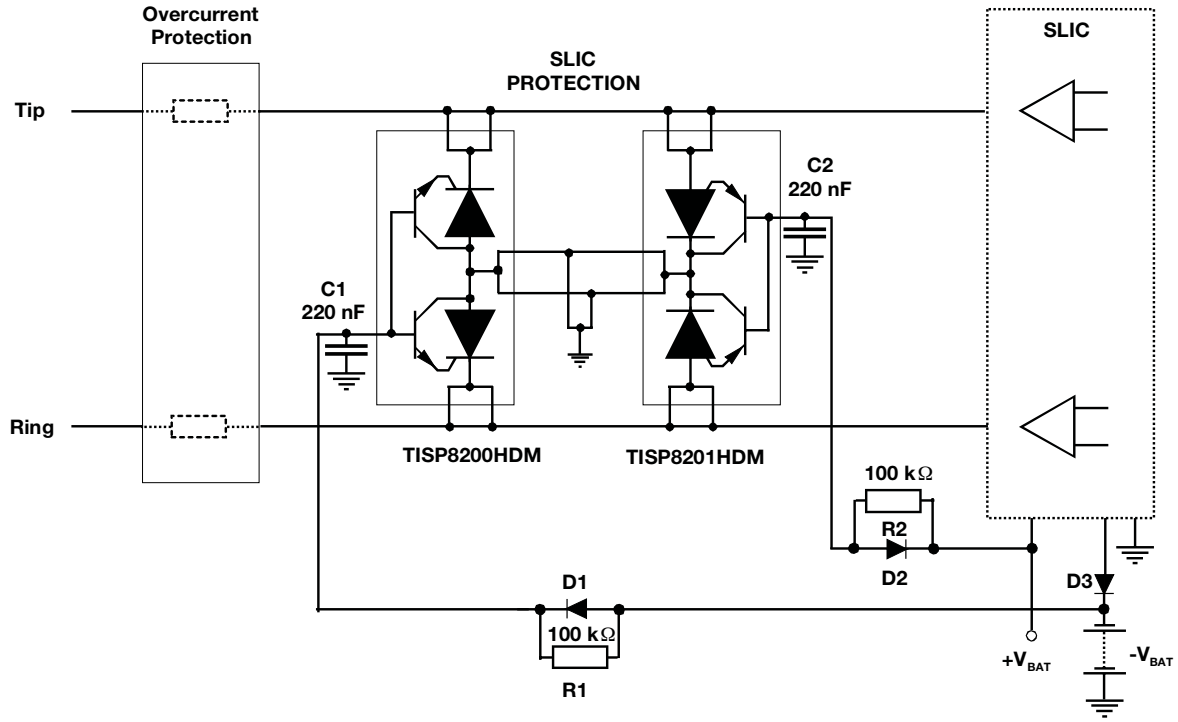


Figure 3. Typical Application Circuit

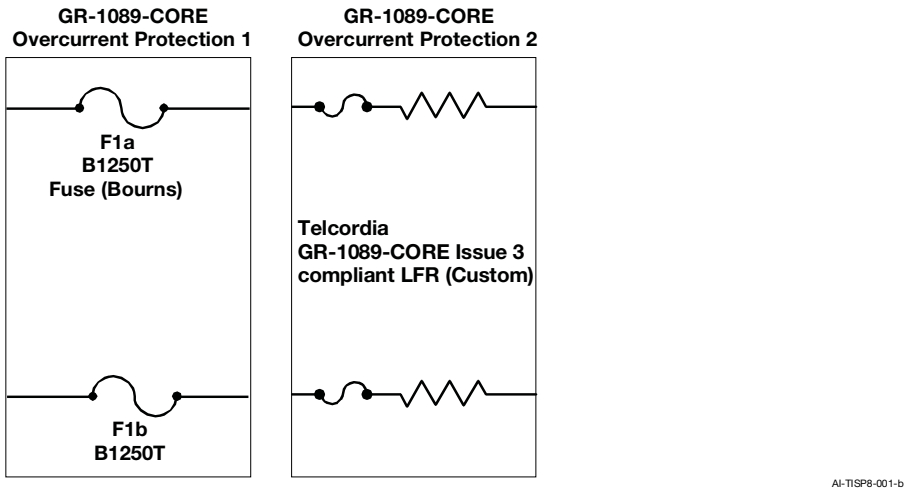


Figure 4. Typical Overcurrent Protection

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