Not recommended for new designs –
Please use 25AA320A or 25LC320A.

25AA320/25LC320/25C320

32K SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
25AA320	1.8-5.5V	1 MHz	I
25LC320	2.5-5.5V	2 MHz	I,E
25C320	4.5-5.5V	3 MHz	I,E

Features:

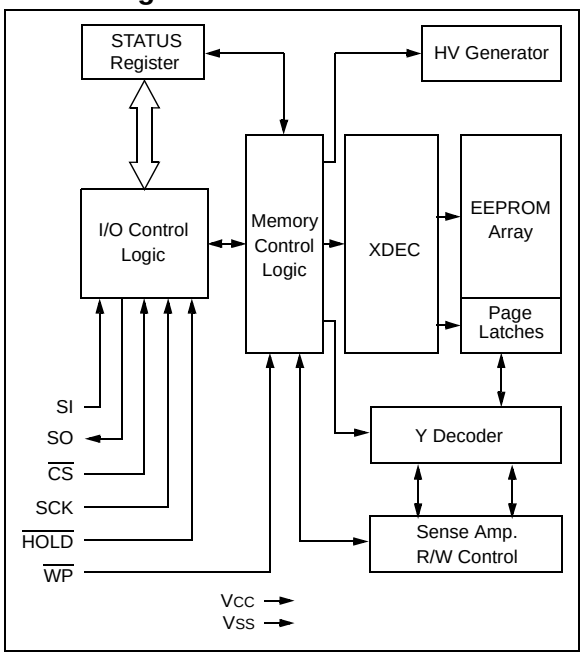
- Low-Power CMOS Technology:
  - Write current: 3 mA maximum
  - Read current: 500 µA, typical
  - Standby current: 500 nA, typical
- 4096 x 8 Bit Organization
- 32 Byte Page
- Write Cycle Time: 5 ms Maximum
- Self-Timed Erase and Write Cycles
- Block Write Protection:
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
  - Power on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability:
  - Endurance: 1M E/W cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- 8-Pin PDIP, SOIC and TSSOP Packages
- 14-Lead TSSOP Package
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description:

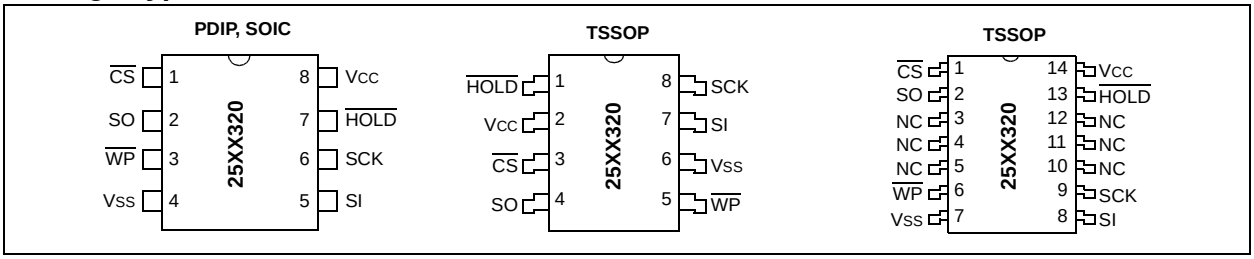
The Microchip Technology Inc. 25AA320/25LC320/25C320 (25XX320*) are 32 Kbit serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

Block Diagram



Package Types



*25XX320 is used in this document as a generic part number for the 25AA320/25LC320/25C320 devices.

© 2008 Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC + 1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 125°C

ESD protection on all pins.....4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Max.**	**Units**	**Conditions**
D1	VIH1	High-level input voltage	2.0	VCC+1	V	VCC ≥ 2.7V **(Note)**
D2	VIH2		0.7 VCC	VCC+1	V	VCC< 2.7V **(Note)**
D3	VIL1	Low-level input voltage	-0.3	0.8	V	VCC ≥ 2.7V **(Note)**
D4	VIL2		-0.3	0.3 VCC	V	VCC < 2.7V **(Note)**
D5	VOL	Low-level output voltage	—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D6	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA
D7	ILI	Input leakage current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
D8	ILO	Output leakage current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
D9	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(Note)**
D10	ICC Read	Operating Current	— —	1 500	mA µA	VCC = 5.5V; FCLK = 3.0 MHz; SO = Open VCC = 2.5V; FCLK = 2.0 MHz; SO = Open
D11	ICC Write		— —	5 3	mA mA	VCC = 5.5V VCC = 2.5V
D12	ICCS	Standby Current	— —	5 1	µA µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS $\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS

Note: This parameter is periodically sampled and not 100% tested.

© 2008 Microchip Technology Inc.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	F_{CLK}	Clock Frequency	— — —	3 2 1	MHz MHz MHz	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
2	T_{CSS}	$\overline{CS}$ Setup Time	100 250 500	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
3	T_{CSH}	$\overline{CS}$ Hold Time	150 250 475	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
4	T_{CSD}	$\overline{CS}$ Disable Time	500	—	ns	—
5	T_{SU}	Data Setup Time	30 50 50	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
6	T_{HD}	Data Hold Time	50 100 100	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
7	T_R	CLK Rise Time	—	2	µs	**(Note 1)**
8	T_F	CLK Fall Time	—	2	µs	**(Note 1)**
9	T_{HI}	Clock High Time	150 230 475	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
10	T_{LO}	Clock Low Time	150 230 475	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
11	T_{CLD}	Clock Delay Time	50	—	ns	—
12	T_{CLE}	Clock Enable Time	50	—	ns	—
13	T_V	Output Valid from Clock Low	— — —	150 230 —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
14	T_{HO}	Output Hold Time	0	—	ns	**(Note 1)**
15	T_{DIS}	Output Disable Time	— — —	200 250 —	ns ns ns	V_{CC} = 4.5V to 5.5V **(Note 1)** V_{CC} = 2.5V to 5.5V **(Note 1)** V_{CC} = 1.8V to 5.5V
16	T_{HS}	$\overline{HOLD}$ Setup Time	100 100 200	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
17	T_{HH}	$\overline{HOLD}$ Hold Time	100 100 200	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
18	T_{HZ}	$\overline{HOLD}$ Low to Output High-Z	100 150 200	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V **(Note 1)** V_{CC} = 2.5V to 5.5V **(Note 1)** V_{CC} = 1.8V to 5.5V
19	T_{HV}	$\overline{HOLD}$ High to Output Valid	100 150 200	— — —	ns ns ns	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V V_{CC} = 1.8V to 5.5V
20	T_{WC}	Internal Write Cycle Time	—	5	ms	—
21	—	Endurance	1M	—	E/W Cycles	**(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at: www.microchip.com.

FIGURE 1-1: HOLD TIMING

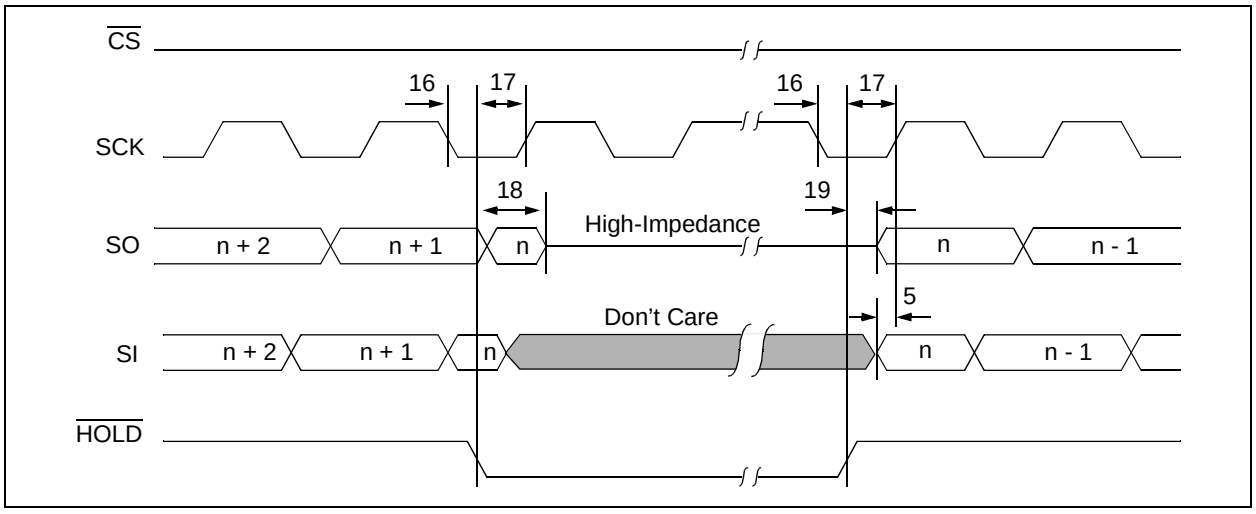


FIGURE 1-2: SERIAL INPUT TIMING

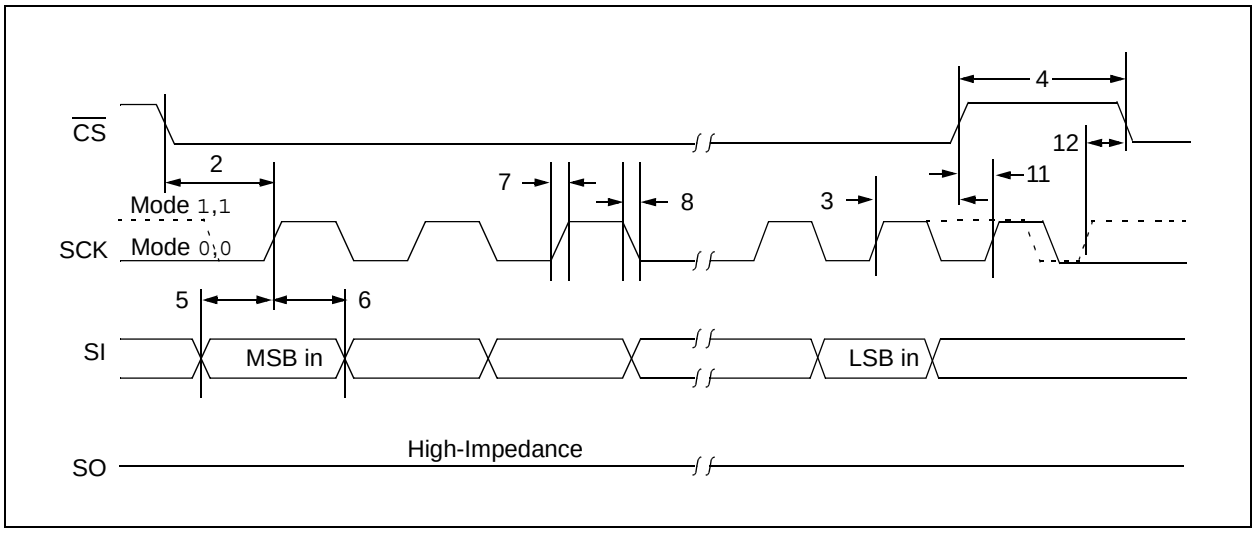
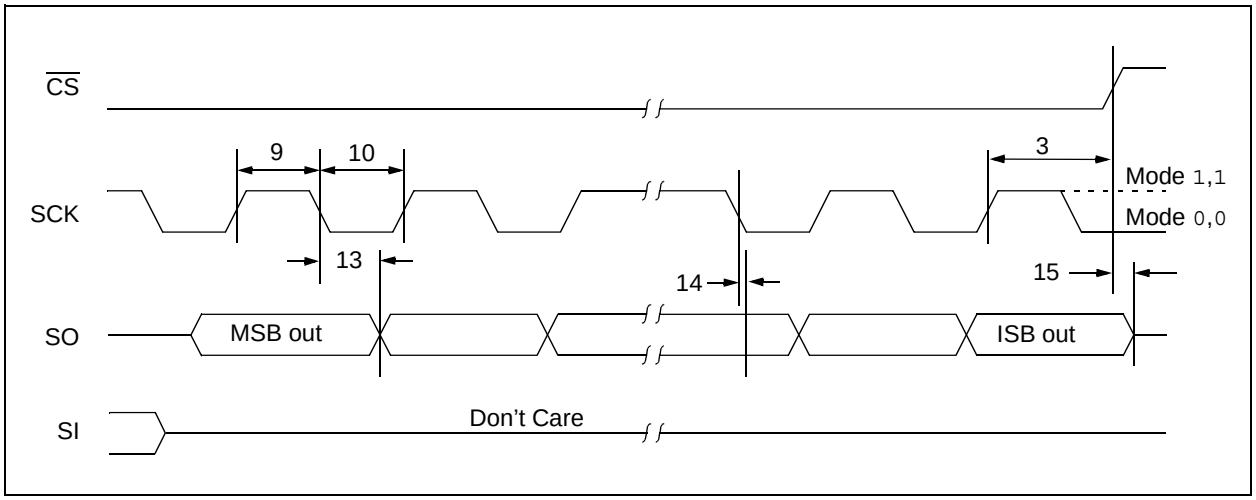


FIGURE 1-3: SERIAL OUTPUT TIMING



© 2008 Microchip Technology Inc.

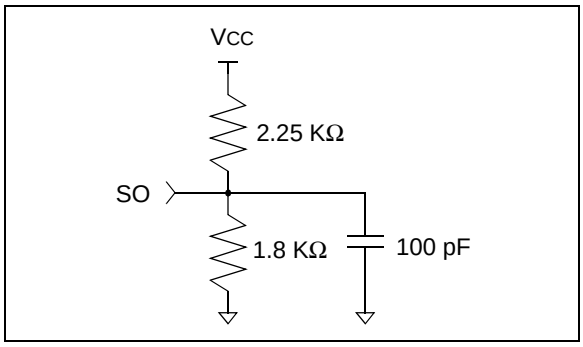
TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**(Note 1)**
V_{HI} = 4.0V	**(Note 2)**
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For $V_{CC} \leq 4.0V$

2: For $V_{CC} > 4.0V$

FIGURE 1-4: AC TEST CIRCUIT



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	8-pin TSSOP	14-lead TSSOP	Description
$\overline{CS}$	1	1	3	1	Chip Select Input
SO	2	2	4	2	Serial Data Output
NC	—	—	—	3,4,5	Not Connected
$\overline{WP}$	3	3	5	6	Write-Protect Pin
Vss	4	4	6	7	Ground
SI	5	5	7	8	Serial Data Input
SCK	6	6	8	9	Serial Clock Input
NC	—	—	—	10,11,12	Not Connected
$\overline{HOLD}$	7	7	1	13	Hold Input
Vcc	8	8	2	14	Supply Voltage

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX320. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25XX320 in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX320. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25XX320 while in the middle of a serial sequence without having to re-transmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX320 must remain selected during this sequence. The SI, SCK, and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

© 2008 Microchip Technology Inc.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles Of Operation

The 25XX320 are 4096 byte Serial EEPROMs designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25XX320 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25XX320 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

3.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 25XX320 followed by the 16-bit address, with the four MSBs of the address being "don't care" bits. After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (0FFFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25XX320, the write enable latch must be set by issuing the `WREN` instruction (Figure 3-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX320. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a `WRITE` instruction, followed by the 16-bit address, with the four MSBs of the address being "don't care" bits, and then the data to be written. Up to 32 bytes of data can be sent to the 25XX320 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with `xxxx xxxx xxx0 0000` and ends with `xxxx xxxx xxx1 1111`. If the internal address counter reaches `xxxx xxxx xxx1 1111` and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
`READ`	`0000 0011`	Read data from memory array beginning at selected address
`WRITE`	`0000 0010`	Write data to memory array beginning at selected address
`WRDI`	`0000 0100`	Reset the write enable latch (disable write operations)
`WREN`	`0000 0110`	Set the write enable latch (enable write operations)
`RDSR`	`0000 0101`	Read STATUS register
`WRSR`	`0000 0001`	Write STATUS register

FIGURE 3-1: READ SEQUENCE

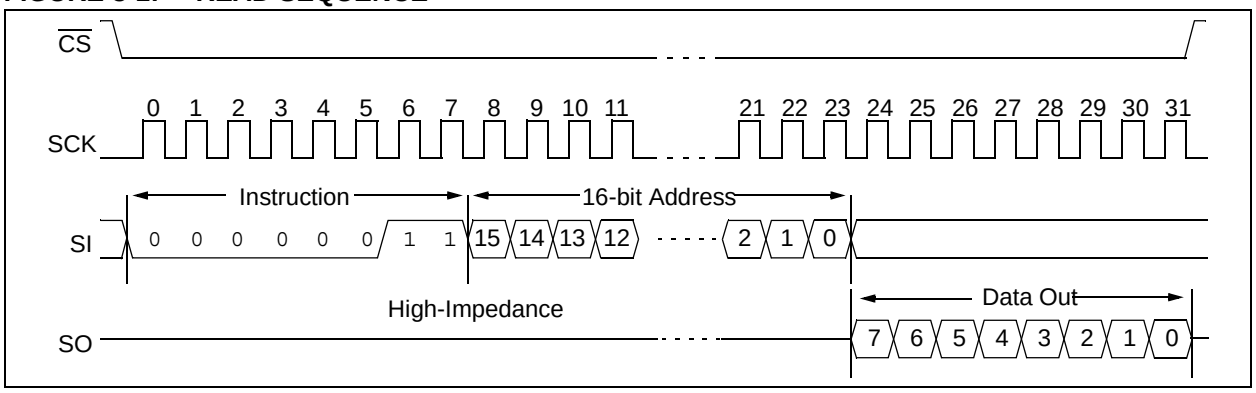


FIGURE 3-2: BYTE WRITE SEQUENCE

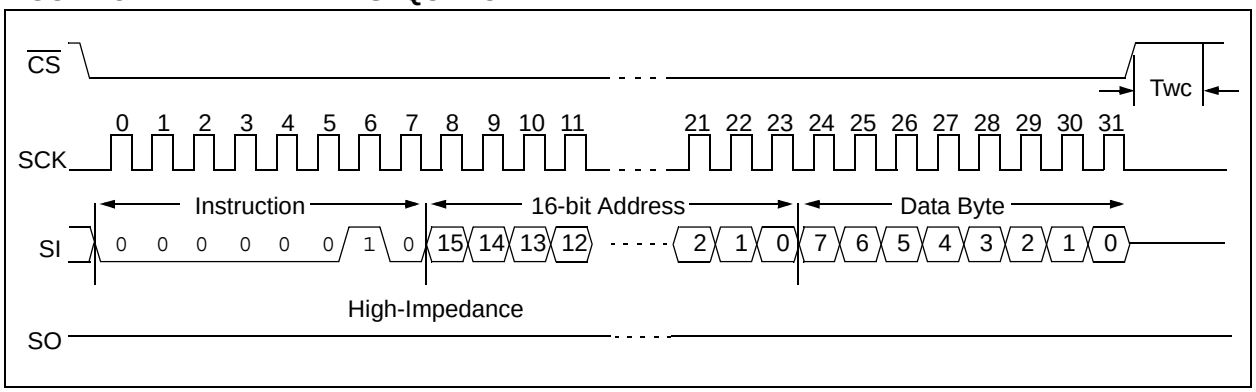
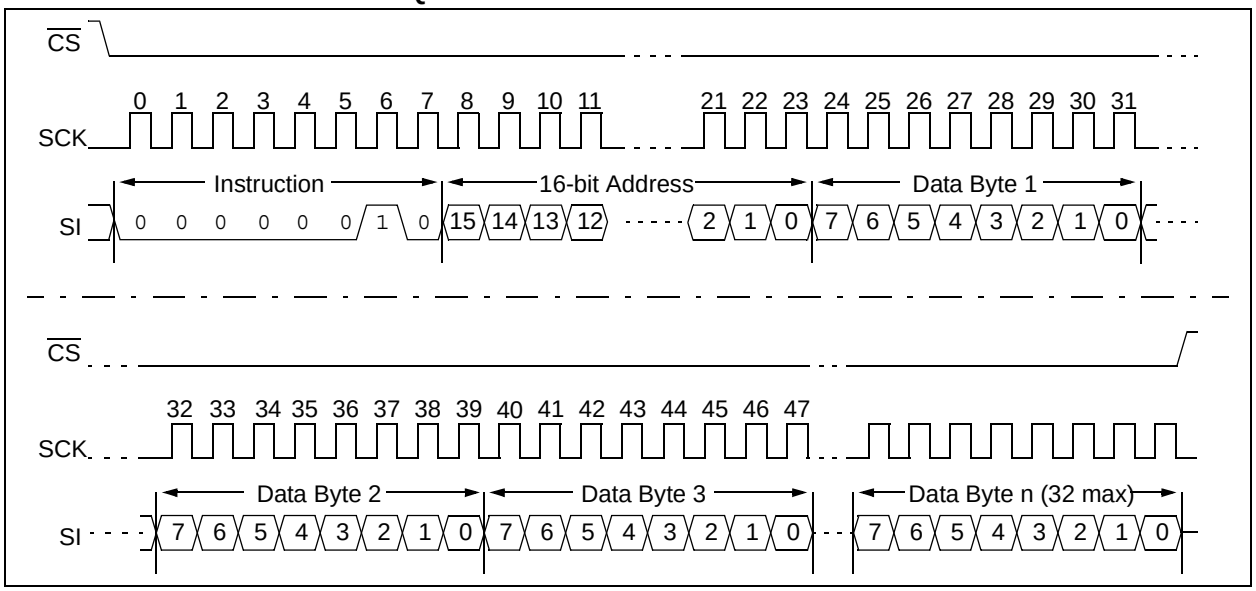


FIGURE 3-3: PAGE WRITE SEQUENCE



© 2008 Microchip Technology Inc.

3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX320 contains a write enable latch. See Table 3-3 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 3-4: WRITE ENABLE SEQUENCE

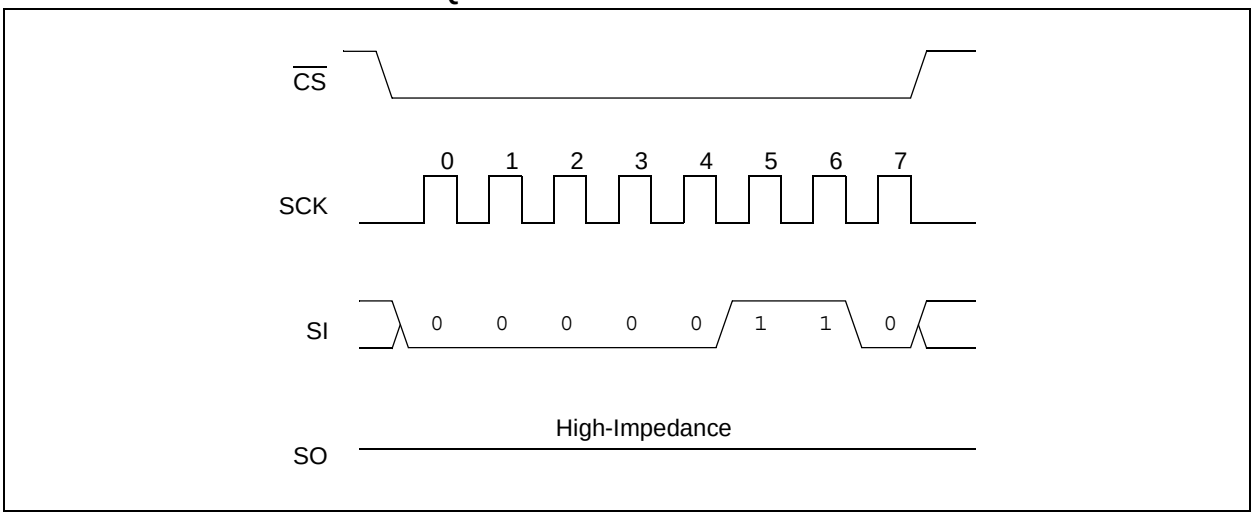
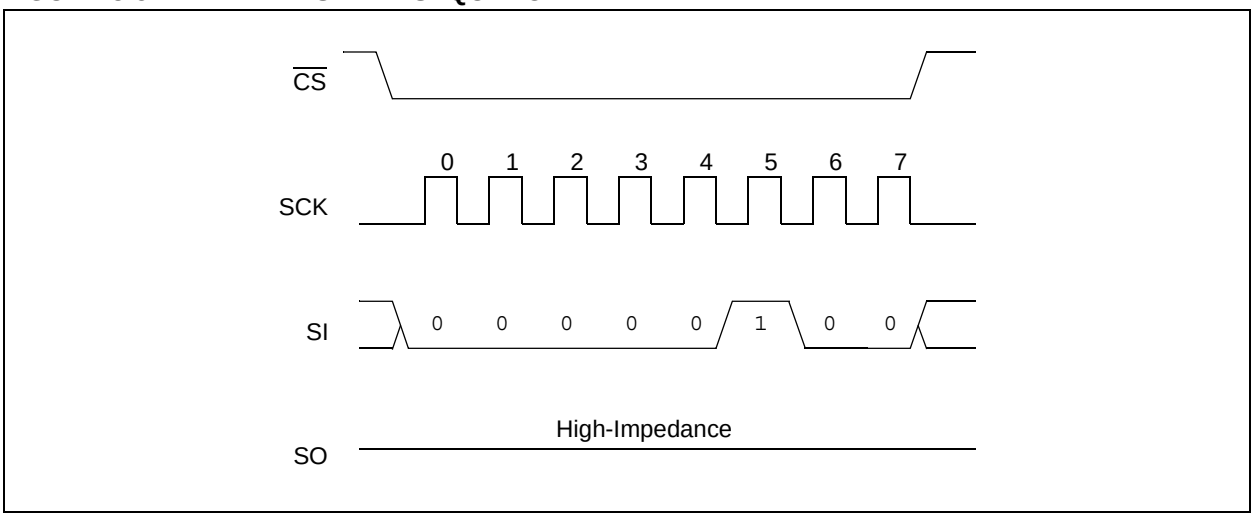


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

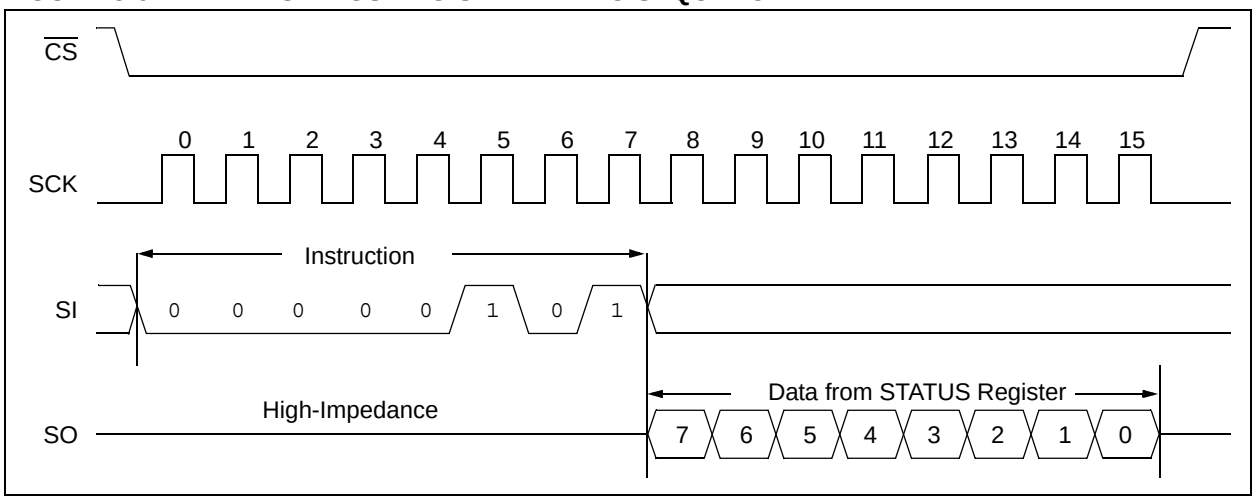
The **Write-In-Process (WIP)** bit indicates whether the 25XX320 is busy with a write operation. When set to a '1', a write is in progress; when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. This bit is read-only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile.

See Figure 3-6 for the RDSR timing sequence.

FIGURE 3-6: READ STATUS REGISTER TIMING SEQUENCE



© 2008 Microchip Technology Inc.

3.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as shown in Table 3-2.

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low.

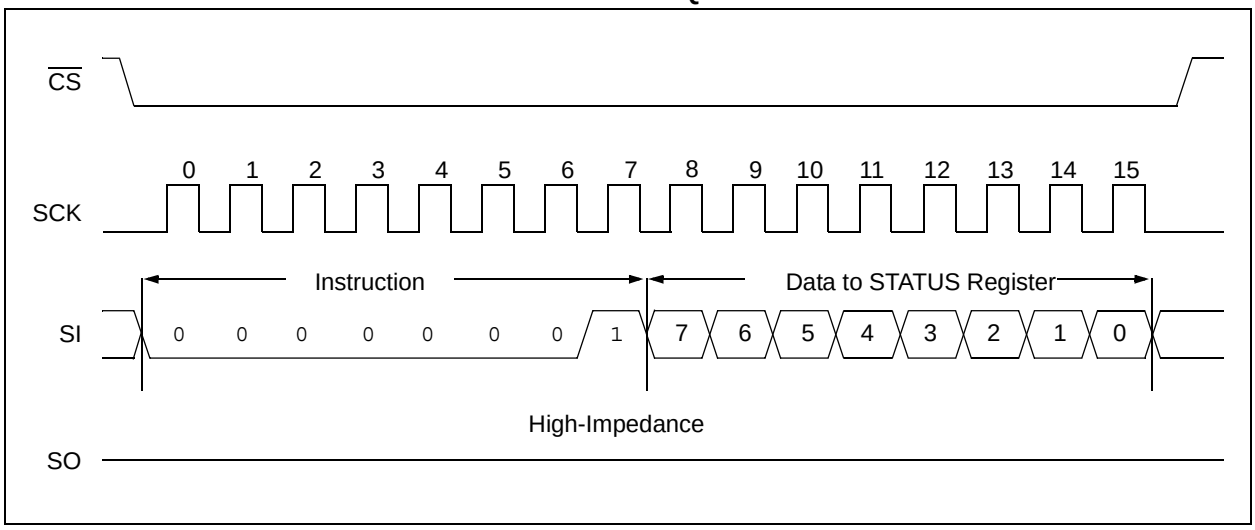
When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 3-3 for a matrix of functionality on the WPEN bit.

See Figure 3-7 for the WRSR timing sequence.

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (0C00h-0FFFh)
1	0	upper 1/2 (0800h-0FFFh)
1	1	all (0000h-0FFFh)

FIGURE 3-7: WRITE STATUS REGISTER TIMING SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A WRITE ENABLE instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

3.8 Power-On State

The 25XX320 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A low level on $\overline{CS}$ is required to enter active state

TABLE 3-3: WRITE-PROTECT FUNCTIONALITY MATRIX

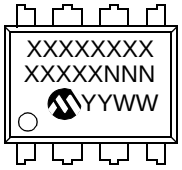
WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	STATUS Register
x	x	0	Protected	Protected	Protected
0	x	1	Protected	Writable	Writable
1	Low	1	Protected	Writable	Protected
x	High	1	Protected	Writable	Writable

© 2008 Microchip Technology Inc.

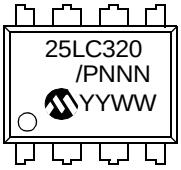
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

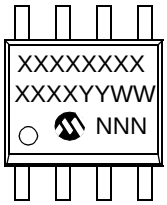
8-Lead PDIP (300 mil)



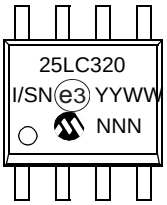
Example:



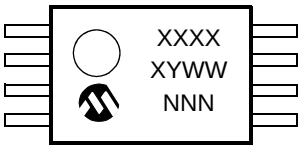
8-Lead SOIC (150 mil)



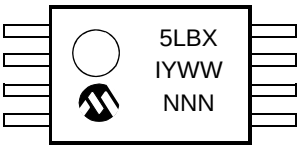
Example:



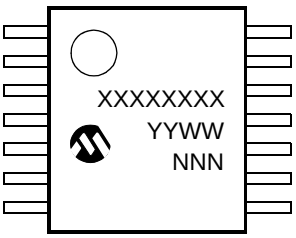
8-Lead TSSOP



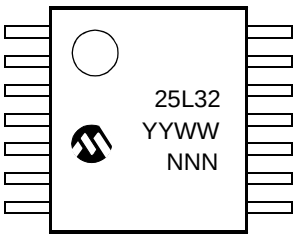
Example:



14-Lead TSSOP



Example:



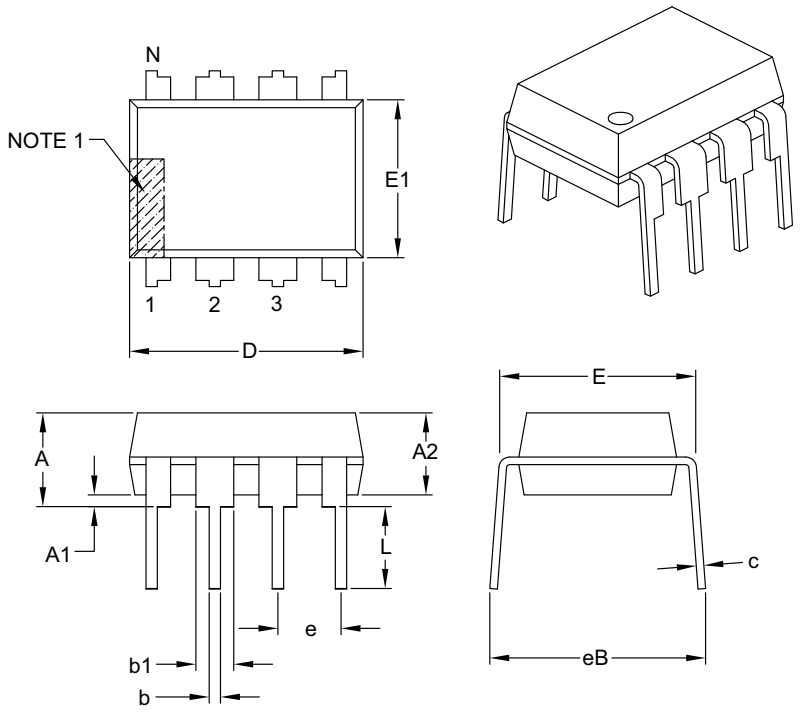
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard marking consists of Microchip part number, year code, week code, and traceability code. For device markings beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

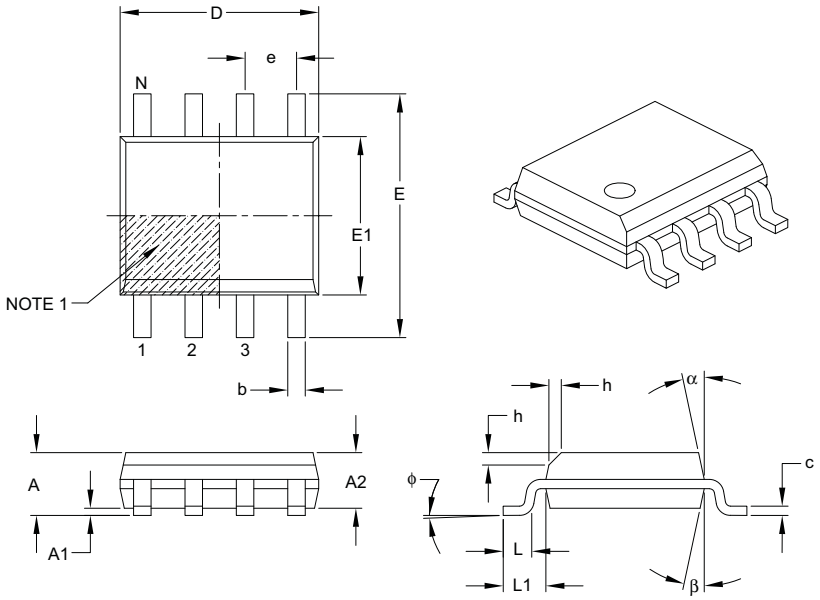
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

© 2008 Microchip Technology Inc.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

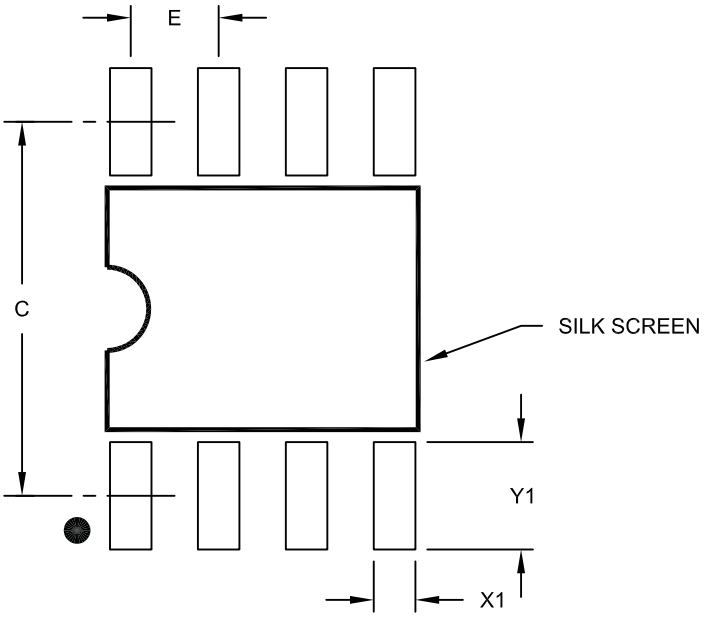
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

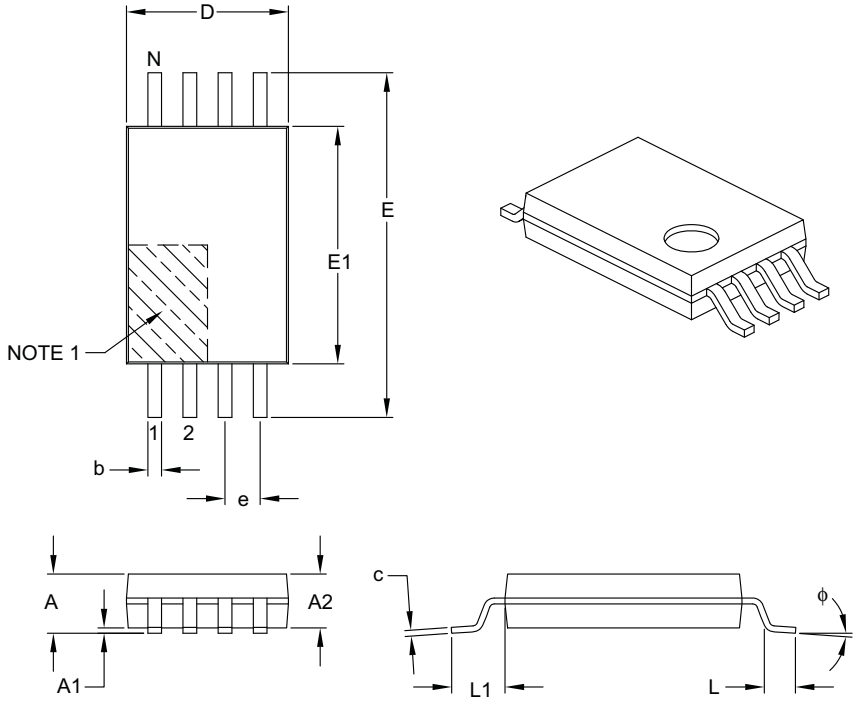
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

© 2008 Microchip Technology Inc.

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

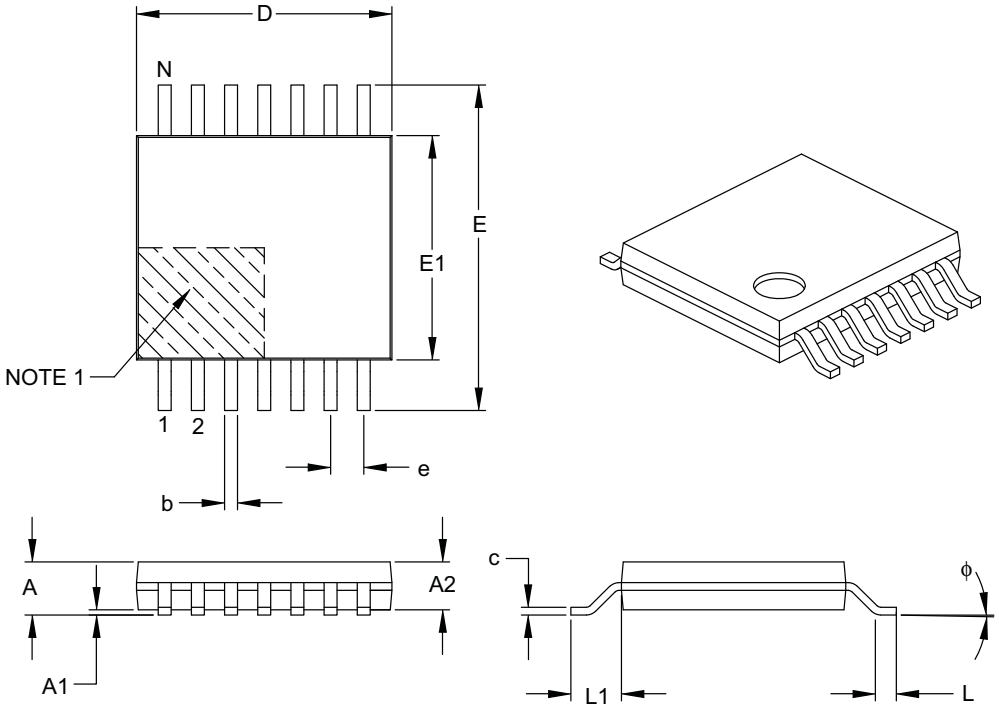
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

© 2008 Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.

Revision E

Revise Endurance from 100K to 1M.

Revision F (June 2008)

Added “Not Recommended” note; Updated Packaging;
General updates.

NOTES:

© 2008 Microchip Technology Inc.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: 25AA320/25LC320/25C320 Literature Number: DS21227F

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

© 2008 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	25AA320:		32 Kbit 1.8V SPI Serial EEPROM
	25AA320T:		32 Kbit 1.8V SPI Serial EEPROM (Tape and Reel)
	25AA320X		32-bit 1.8V SPI Serial EEPROM in alternate pinout (ST only)
	25AA320XT		32-bit 1.8V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
	25LC320:		32 Kbit 2.5V SPI Serial EEPROM
	25LC320T:		32 Kbit 2.5V SPI Serial EEPROM (Tape and Reel)
	25LC320X		32-bit 2.5V SPI Serial EEPROM in alternate pinout (ST only)
	25LC320XT		32-bit 2.5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
	25C320:		32 Kbit 5V SPI Serial EEPROM
	25C320T:		32 Kbit 5V SPI Serial EEPROM (Tape and Reel)
	25C320X		32-bit 5V SPI Serial EEPROM in alternate pinout (ST only)
	25C320XT		32-bit 5V SPI Serial EEPROM in alternate pinout Tape and Reel (ST only)
Temperature Range:	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Package:	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm body), 8-lead
	ST14	=	Plastic TSSOP (4.4 mm body), 14-lead

Examples:

a) 25LC320-I/SN: Industrial Temp., SOIC package

b) 25LC320T-I/SN: Tape and Reel, Industrial Temp., SOIC package

c) 25LC320-E/SN: Extended Temp., SOIC package

d) 25C320-I/SN: Industrial Temp., SOIC package

e) 25C320T-I/SN: Tape and Reel, Industrial Temp., SOIC package

f) 25C320-I/ST: Industrial Temp., TSSOP package

g) 25C320-E/SN: Extended Temp., SOIC package

NOTES:

© 2008 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, rfPIC and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, PICkit, PICDEM, PICDEM.net, PICtail, PIC^{32} logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2008, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/02/08

© 2008 Microchip Technology Inc.