FAN7685/FAN7686/FAN7687

PC Power Supply Output Monitoring IC

Features

- PC Power Supply Outputs Supervisory Circuitry
- Few External Components
- Over Voltage Protection for 3.3V, 5V and 12V Outputs
- Under Voltage Protection for 3.3V, 5V and 12V Outputs
- Over Current Protection for 3.3V, 5V and 12V Outputs
- Dual Over Current Portection for 12V Outputs(FAN7687)
- Fault Protection Output With Open Drain Output
- Open Drain Power Good Output
- 300ms Power Good Delay
- 38ms $\overline{\text{PSON}}$ On/Off Delay
- 73us Debounce
- 2.3ms $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$ Turn Off Delay
- Latch Function Controlled by $\overline{\text{PSON}}$

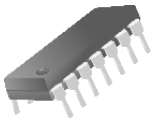
Typical Application

- PC Switching Mode Power Supply

Description

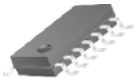
The FAN7685/FAN7686/FAN7687 is a complete output supervisory circuitry intended for use in the secondary side of the switched mode power supply. It provides overvoltage protection (OVP), undervoltage protection(UVP), overcurrent protection (OCP), and power good signal generator to monitor and control the outputs of the switching power supply system. Remote on/off($\overline{\text{PSON}}$) control and some precision protection features are also implemented.
It directly senses all the output rails for OVP, UVP, and OCP without external divider resistors. As for output control, power good output(PGO) and fault protection output($\overline{\text{FPO}}$) are included. The FAN7685/FAN7686/FAN7687 offers a simple and cost effective solution with minimum number of external components and greatly reduces PCB board space for power supply.

14DIP



1

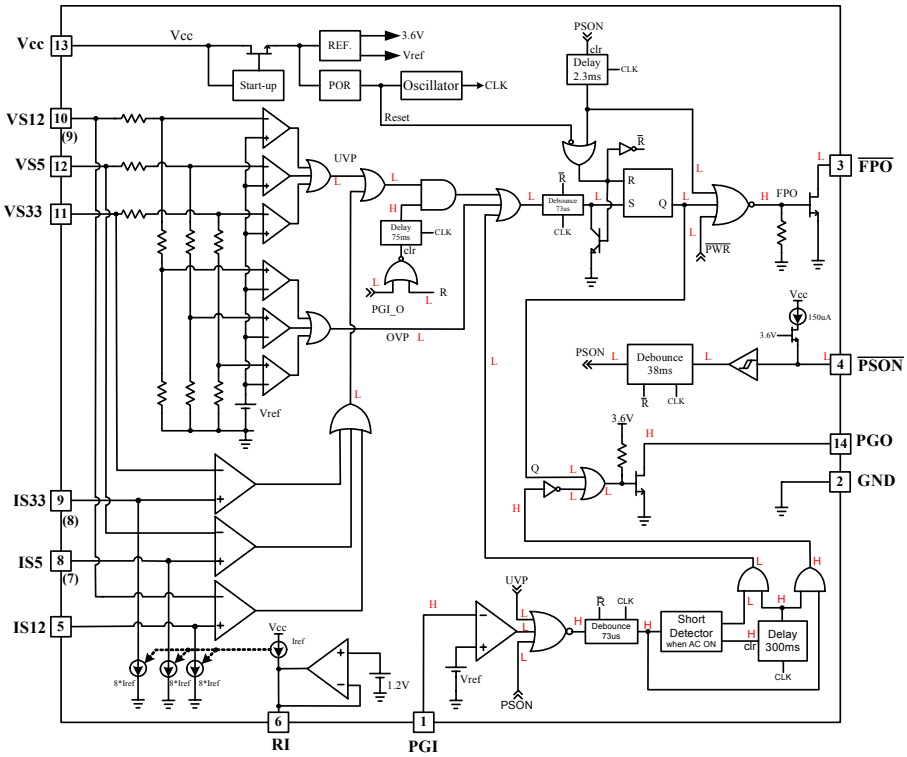
14SOP



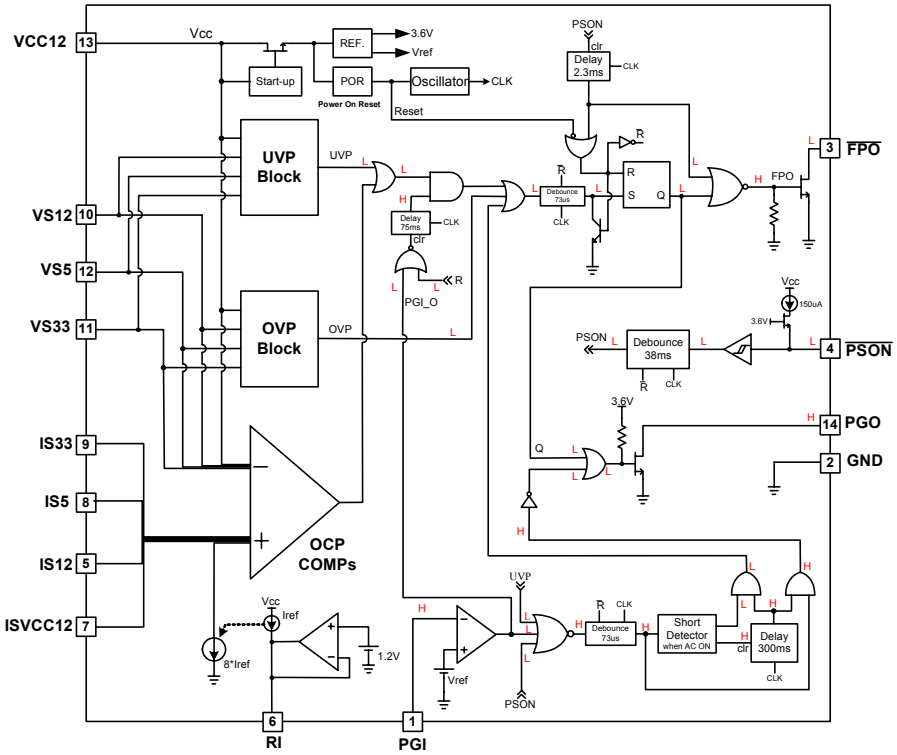
1

©2004 Fairchild Semiconductor Corporation

Internal Block Diagrams

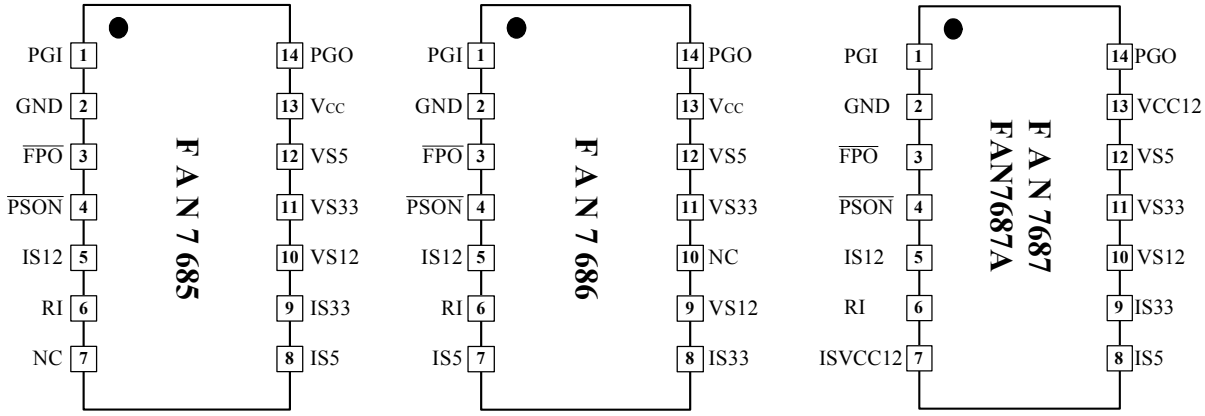


FAN7685
(FAN7686)



FAN7687
FAN7687A

Pin Assignments



Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	PGI	I	Power Good Input
2	GND	-	Ground
3	$\overline{\text{FPO}}$	O	Fault Protection Output, Open Drain Output
4	$\overline{\text{PSON}}$	I	Remote On/Off Control Input
5	IS12	I	12V Over Current Protection
6	RI	O	Reference Current Setting Resistor
7	NC		No Connection(FAN7685)
	IS5*	I	5V Over Current Protection(FAN7686)
	ISVCC12**	I	12V-II Over Current Protection(FAN7687)
8	IS5	I	5V Over Current Protection(FAN7685/7)
	IS33*	I	3.3V Over Current Protection(FAN7686)
9	IS33	I	3.3V Over Current Protection(FAN7685/7)
	VS12*	I	12V Output Over/Under Voltage Protection(FAN7686)
10	VS12	I	12V Output Over/Under Voltage Protection(FAN7685/7)
	NC*		No Connection(FAN7686)
11	VS33	I	3.3V Output Over/Under Voltage Protection
12	VS5	I	5V Output Over/Under Voltage Protection
13	Vcc	I	Supply Voltage(FAN7675/6)
	VCC12**	I	Supply Voltage & 12V-II OV/UV Protectioin(FAN7687)
14	PGO	O	Power Good Output, Open Drain Output

Notes :
* : FAN7686 Pin Definitions
** : FAN7687/FAN7687A Pin Definitions

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}, VCC12	16	V
Input Voltage	$V_{\overline{PSON}}$, VS5, VS33, V_{PGI}, IS5, IS33	8	V
	VS12, IS12, ISVCC12	16	
Output Voltage	V_{PGO}	8	V
	$V_{\overline{FPO}}$	16	
Operating Temperature	Topr	-40 ~ 125	°C
Storage Temperature	Tstg	-55 ~ 150	°C
Power Dissipation	P_D	1	W

*Note : Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Recommended Operating Conditions

Characteristic		Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}, VCC12	4		15	V
Input Voltage	$V_{\overline{PSON}}$, VS5, VS33, V_{PGI}, IS5, IS33	-	-	7	V
	VS12, IS12, ISVCC12	-	-	15	
Output Voltage	V_{PGO}	-	-	7	V
	$V_{\overline{FPO}}$	-	-	15	V
Output Sink Current	$I_{\overline{FPO}}$	-	-	30	mA
	I_{PGO}	-	-	10	mA
Supply Voltage Rising Time, See Note1	tr	1			ms
Output Current for RI	$I_{O(RI)}$	12.5	-	62.5	uA

Note

1. V_{CC} slew rate must be less than 14V/ms.

Electrical Characteristics(VCC = 5V, Ta=25°C, unless otherwise specified)

Over Voltage Protection, Under Voltage Protection and FPO

Parameter		Test Condition	Min.	Typ.	Max.	Unit
Over Voltage Threshold	VS33		3.9	4.1	4.3	V
		FAN7687A	3.77		4.06	
	VS5		5.8	6.1	6.4	
		FAN7687A	5.71		6.16	
	VS12, VCC12		13.3	13.8	14.3	
		FAN7687A(VS12)	13.71		14.79	
		FAN7687A(VCC12)	13.42		14.5	
Under Voltage Threshold	VS33		2.55	2.69	2.83	V
		FAN7687A	2.88		3.02	
	VS5		4.1	4.3	4.5	
		FAN7687A	4.37		4.58	
	VS12, VCC12		8.8	9.3	9.8	
		FAN7687A(VS12)	10.5		11.0	
		FAN7687A(VCC12)	10.21		10.71	
Ratio of Current Sense Sink Current to Current Sense Setting Pin(RI) Source Current	Iref	Resistor at RI=30kΩ, 0.1% Resistor	7.6	8	8.4	
Offset Voltage of OCP Comparator	V_{offset}	$V_{\overline{PSON}}$=0V	-5	-	5	mV
Leakage Current($\overline{FPO}$)	I_{LKGI}	$V_{\overline{FPO}}$ = 5V	-	-	5	uA
Low Level Output Voltage($\overline{FPO}$)	V_{OLI}	$I_{\overline{FPO}}$=10mA	-	-	0.3	V
		$I_{\overline{FPO}}$=30mA	-	-	0.7	

PGI and PGO

Input Threshold Voltage(PGI)	V_{PGI}		1.16	1.20	1.24	V
Leakage Current(PGO)	I_{LKG2}	V_{PGO} = 5V	-	-	5	uA
Low Level Output Voltage(PGO)	V_{OL2}	I_{PGO}=10mA	-	-	0.4	V

$\overline{PSON}$ Control

Input Pull-up Current	$I_{\overline{PSON}}$	$V_{\overline{PSON}}$ = 0V	-	150	-	uA
High-Level Input Voltage	V_{IHPS}		2.4	-	-	V
Low-Level Input Voltage	V_{ILPS}		-	-	1.2	V

Total Device

Supply Current	I_{CC}	$V_{\overline{PSON}}$ = 5V	-	-	1	mA

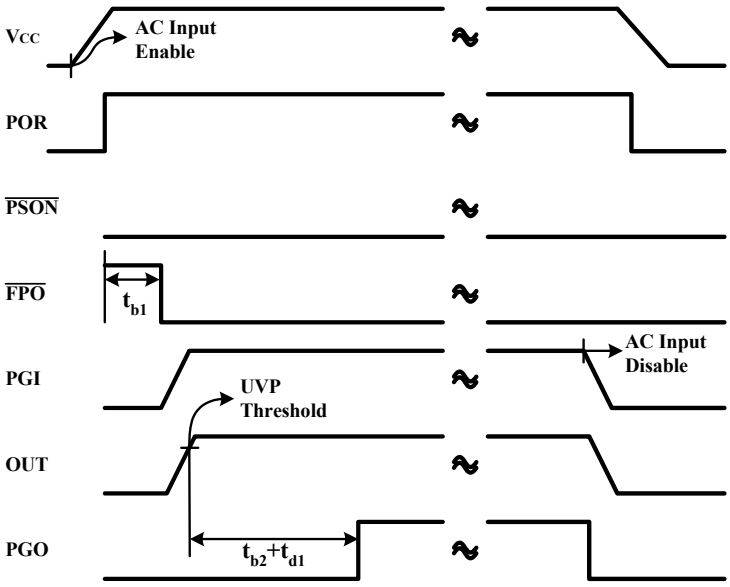
Switching Characteristics

Debounce Time($\overline{PSON}$)	t_{b1}		25	38	51	ms
Noise Debounce Time	t_{b2}*		50	73	100	us
PGO Delay Time(PGI to PGO)	t_{d1}		200	300	410	ms
Internal UVP Delay Time	t_{d2}	$\overline{FPO}$ goes low and every time PGI > 1.2	51	75	102	ms
	t_{d4}*	$\overline{FPO}$ goes low and everytime PGI<1.2	200	300	410	ms
$\overline{PSON}$ off to $\overline{FPO}$ Delay Time	t_{d3}		t_{b1}+1.6	t_{b1}+2.3	t_{b1}+3.2	ms

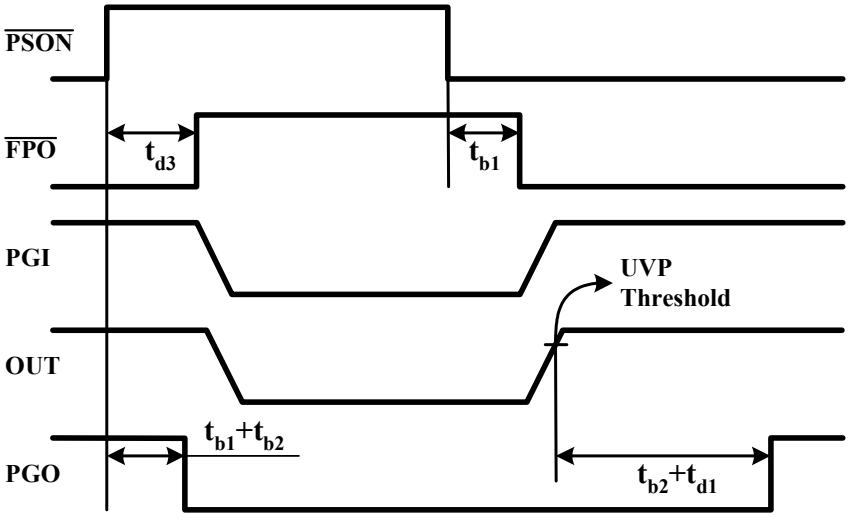
* : These parameters although guaranteed over the recommended operating conditions, are not 100% tested in production.

Timing Chart

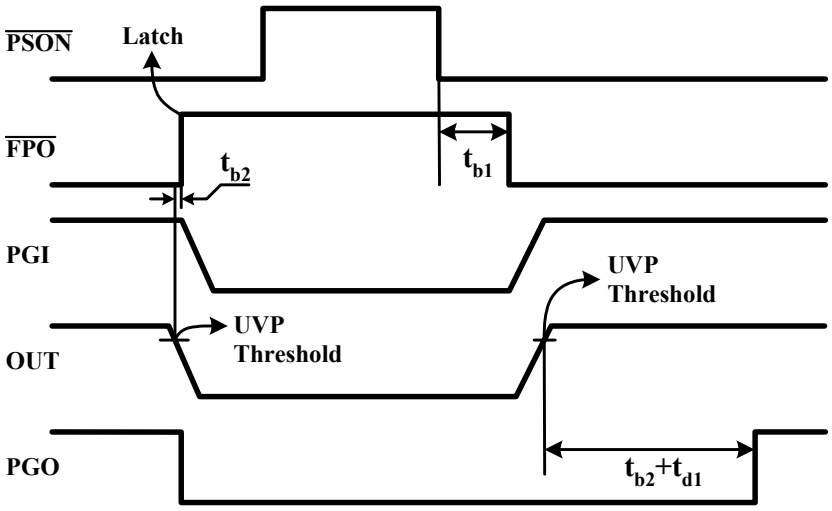
1) AC Input ON/OFF - Normal State



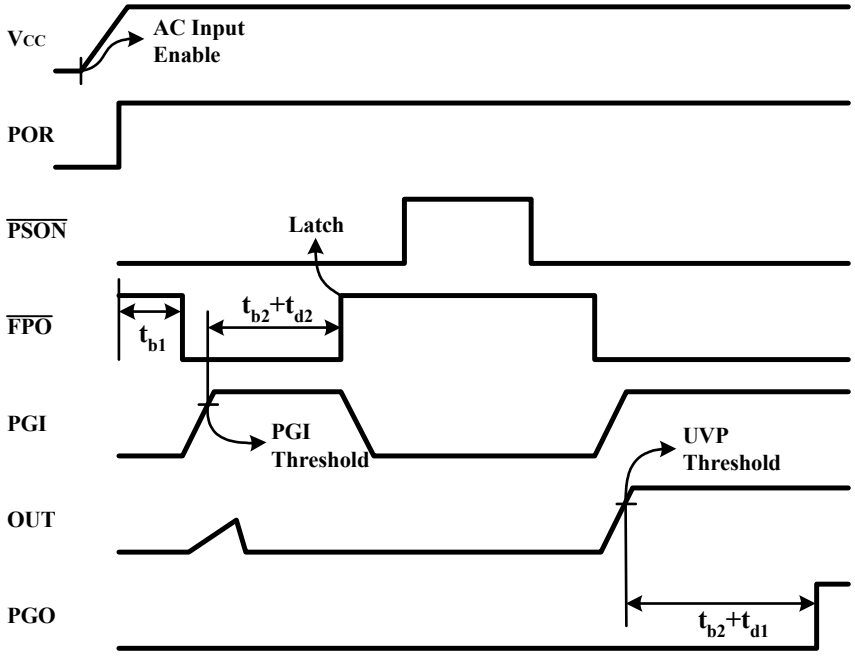
2) $\overline{\text{PSON}}$ ON/OFF - Normal State



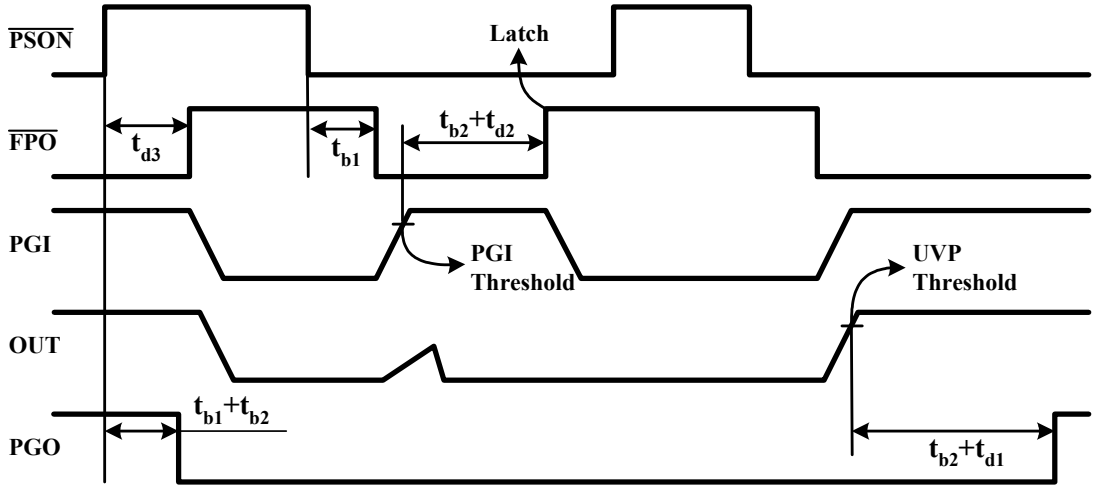
3) Under Voltage at Normal State



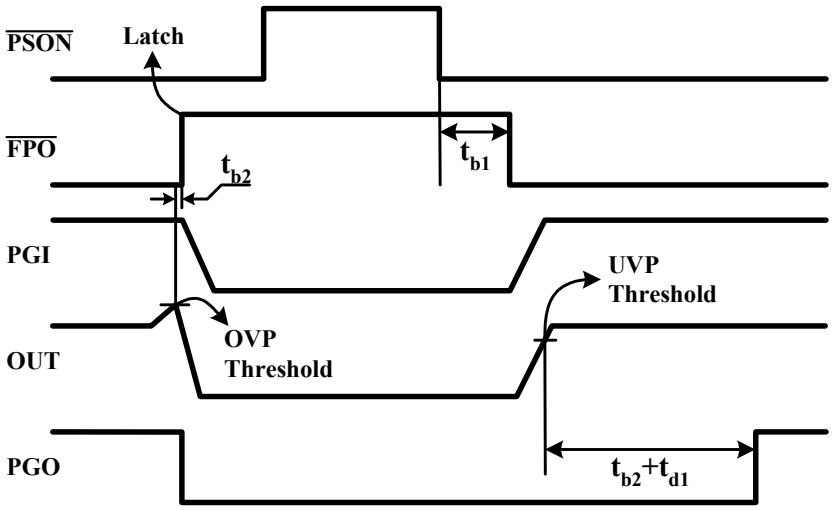
4) Under Voltage at AC Input ON



5) Under Voltage at $\overline{\text{PSON}}$ ON/OFF

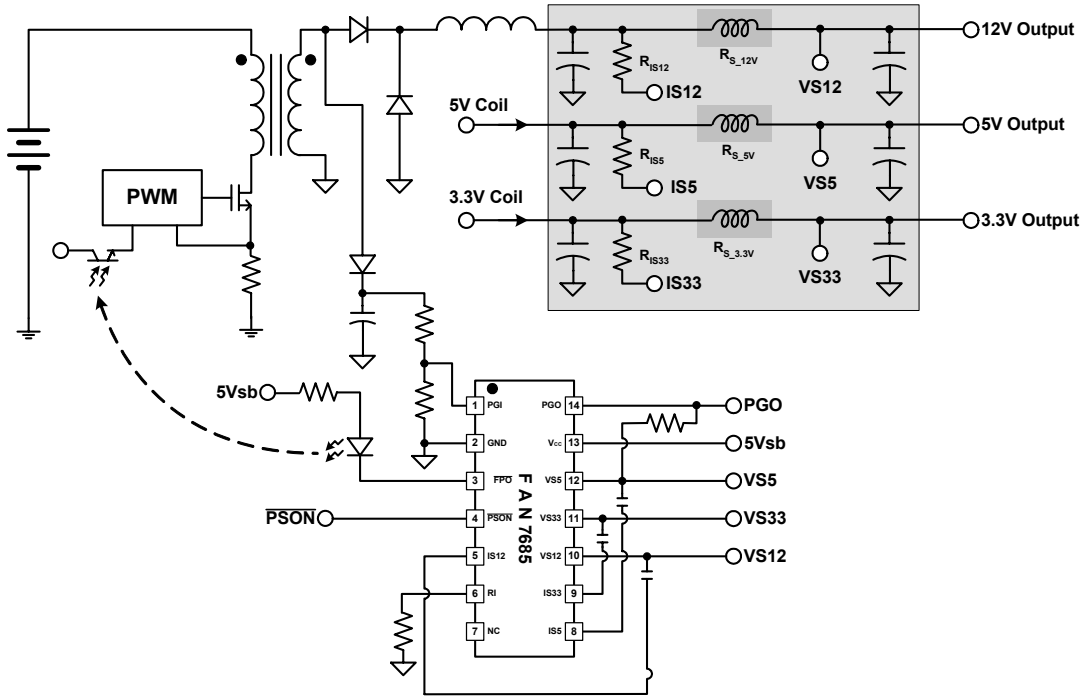


6) Over Voltage at $\overline{\text{PSON}}$ ON/OFF

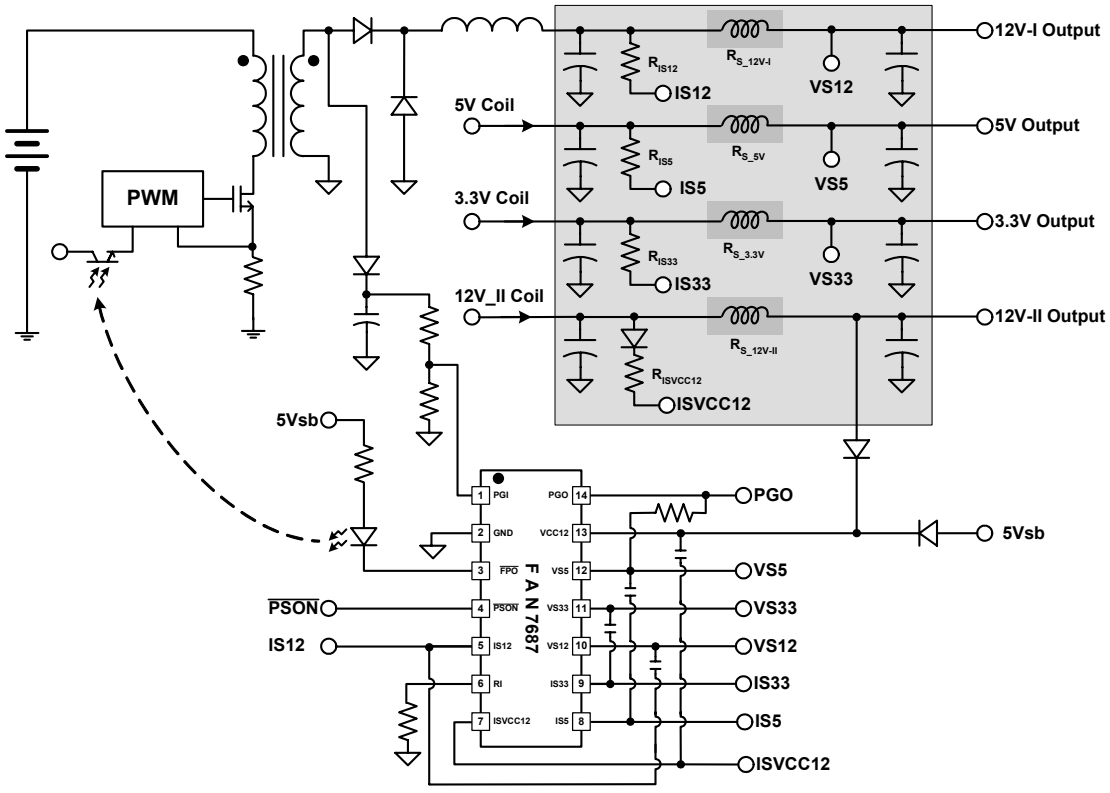


Typical Application Circuits

FAN7685 Application Circuit



FAN7687 Application Circuit

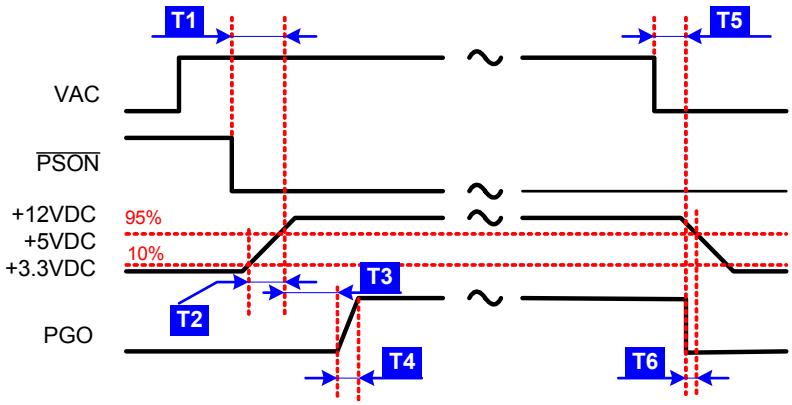


Application Information

Power Good(PGO) and Power Good Delay

A PC power supply is commonly designed to provide the motherboard with a power good signal, which is defined by the computer manufacturers. If the +3.3V, +5V, and +12V outputs are above the undervoltage threshold limit, the PC power supply makes the power good signal high. At this time the power supply should be able to provide enough power to assure continuous operation within the specification. Conversely, when one of the +3.3V, +5V, or +12V outputs falls below the undervoltage threshold or rises above the overvoltage threshold, or when main power has been turned off for a sufficiently long time so that power supply operation is no longer assured, a PGO signal will be a low state.

The AC input, power good(PGO), remote on/off($\overline{\text{PSON}}$), and +3.3V/+5V/+12V supply rails are shown in the below figure.



Although there is no requirement to meet specific timing parameters, the following signal timings are recommended :

-T1(Power On Time) : T1 < 500ms
-T2(Rise Time) : 0.1ms ≤ T2 ≤ 20ms
-T3(PGO Delay) : 100ms < T3 <500ms
-T4(PGO Delay Risetime) : T4 ≤ 10ms
-T5(AC Loss to PGO Hold-Up Time) : T5 ≥ 16ms
-T6(Power Down Warning) : T6 ≥ 1ms

Furthermore, motherboards should be designed to comply with the above recommended timing range. If timings other than these are implemented or required, that information should be clearly specified.

The FAN7685/FAN7686/FAN7687 provide a power good(PGO) signal for the +3.3V, +5V and +12V supply voltage rails and a separate power good input(PGI). An internal delay circuit is used to generate a 300ms power good delay.

If voltages at PGI(+1.2V), VS33(+3.3V), VS5(+5V), and VS12(+12V) rise above the undervoltage threshold, the open drain power good output(PGO) will go high after a delay of 300ms. When the PGI voltage or any of +3.3V, +5V, and +12V rails drops below the undervoltage threshold, the PGO signal will be disabled immediately.

Power Supply Remote On/Off($\overline{\text{PSON}}$) and Fault Protection Output($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turn on and power saving functions, a PC power supply will require two characteristics. One is a dc power supply remote on/off function; the other is standby power to achieve very low power consumption of the PC power supply. Thus, the main power needs to be shut down.

The power supply remote on/off($\overline{\text{PSON}}$) is an active-low signal that turns on all of the main power rails including the +3.3V, +5V, and +12V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output($\overline{\text{FPO}}$) also goes high. Thus, the main power rails can not deliver current and are held at 0V.

When the $\overline{\text{FPO}}$ signal is held high due to a fault condition, the fault status will be latched and the outputs of the main power rails can not deliver current and are held at 0V. Toggling the $\overline{\text{PSON}}$ input signal from low to high will reset the fault protection latch. During this fault condition only the standby power is not affected.

When the $\overline{\text{PSON}}$ input signal goes from high to low or low to high, the 38ms debounce block will be active to avoid that a glitch on the $\overline{\text{PSON}}$ input may disable/enable the $\overline{\text{FPO}}$ output. When the $\overline{\text{PSON}}$ is set low, the undervoltage function is disabled for 75ms to avoid turn-on failure. At turn-off, there is an additional delay of 2.3ms from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$.

Power should be delivered to the rails only when the $\overline{\text{PSON}}$ signal is held at ground potential, thus the $\overline{\text{FPO}}$ becomes a low

state after a debounce of 38ms. The $\overline{FPO}$ pin can be connected to +5V(or up to +15V) through a pull-up resistor.

Under Voltage Protection

The FAN7685/FAN7686/FAN7687 provide undervoltage protection(UVP) for the +3.3V, +5V, and +12V power rails. When an undervoltage condition appears at one of the VS33(+3.3V), VS5(+5V), or VS12(+12V) input pins for more than 73us, the PGO goes low and $\overline{FPO}$ output goes high. Also, this fault condition will be latched until the $\overline{PSON}$ is toggled from low to high or the Vcc falls below a minimum operating voltage.

When the power supply is turned on by the AC input or $\overline{PSON}$, an internal UVP delay time is 75ms. But at normal state an UVP delay time is only a 73us debounce time. The need for undervoltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery powered or hand-held equipment since the TTL or CMOS logic often malfunctions under UVP condition.

Over Voltage Protection(OVP)

The overvoltage protection(OVP) of the FAN7685/FAN7686/FAN7687 monitor +3.3V, +5V, and +12V. When an overvoltage condition appears at one of the +3.3V, +5V, or +12V input pins for more than 73us, the $\overline{FPO}$ output goes high and the PGO goes low. Also, this fault condition will be latched until the $\overline{PSON}$ is toggled from low to high or Vcc drops below a minimum operating voltage. During overvoltage condition, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage to the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

Because TTL and CMOS circuits are very vulnerable to overvoltage, it is becoming industry standard to provide overvoltage protection on all +3.3V, +5V, and +12V outputs. Therefore, not only the +3.3V and +5V rails for the logic circuits on the motherboard need to be protected, but also the +12V peripheral devices such as the hard disk, floppy disk, and CD-ROM players etc., need to be protected.

Over Current Protection

In bridge or forward type, off-line switching power supplies, usually designed from medium to large power, the overload protection design needs to be very precise. Most of these types of power supplies are sensing the output current for an overload condition. The trigger point needs to be set higher than the maximum load in order to prevent false turn-on.

During safety testing the power supply might have tied the output voltage direct to ground. If this happens during the nomal operating, this is called a short-circuit or over current condition. When it happens before the power supply turns on, this is called a short-circuit power supply turn-on. It can happen during the design period, in the production line, at quality control inspection or at the end user. The FAN7685/FAN7686/FAN7687 provide an UVP and OCP with a 75ms delay after $\overline{PSON}$ is set low.

The FAN7685/FAN7686/FAN7687 provide overcurrent protection(OCP) for the 3.3V, 5V, and 12V rails. When an overcurrent condition appears at the OCP comparator input pins for more than 73us, the $\overline{FPO}$ output goes high and PGO goes low. Also, this fault condition will be latched until $\overline{PSON}$ is toggled from low to high or Vcc is removed.

The resistor connected between the RI pin and the GND pin will introduce an accurate $I_{O(RI)}$ for the OCP function. Of course, a more accurate resistor tolerance will be better. The formula for choosing the RI resistor is $V_{RI}/I_{O(RI)}$. The $I_{O(RI)}$ range is from 12.5uA to 62.5uA. Four OCP comparators and the $I_{O(RI)}$ section are supplied by VS12. Current drawn from the VS12pin is less than 1mA.

Following is an example on calculating OCP for the 12V rail :

$$RI = \frac{V_{RI}}{I_{O(RI)}} = \frac{1.2V}{20uA} = 60k\Omega$$

$$I_{O(RI)} \times K \times R_{(IS12)} = R_{(sense)} \times I_{(OCP-Trip)}$$

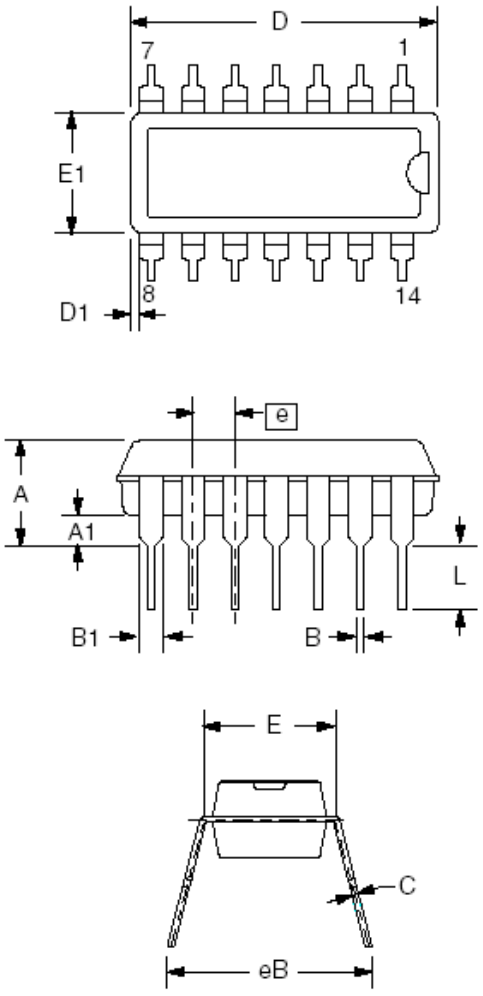
$$I_{(OCP-Trip)} = 20u \times 8 \times 560\Omega / (0.01\Omega) = 9.2A$$

Mechanical Dimensions

Package

Dimensions in millimeters/inches

14-DIP



Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.014	.20	.36	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

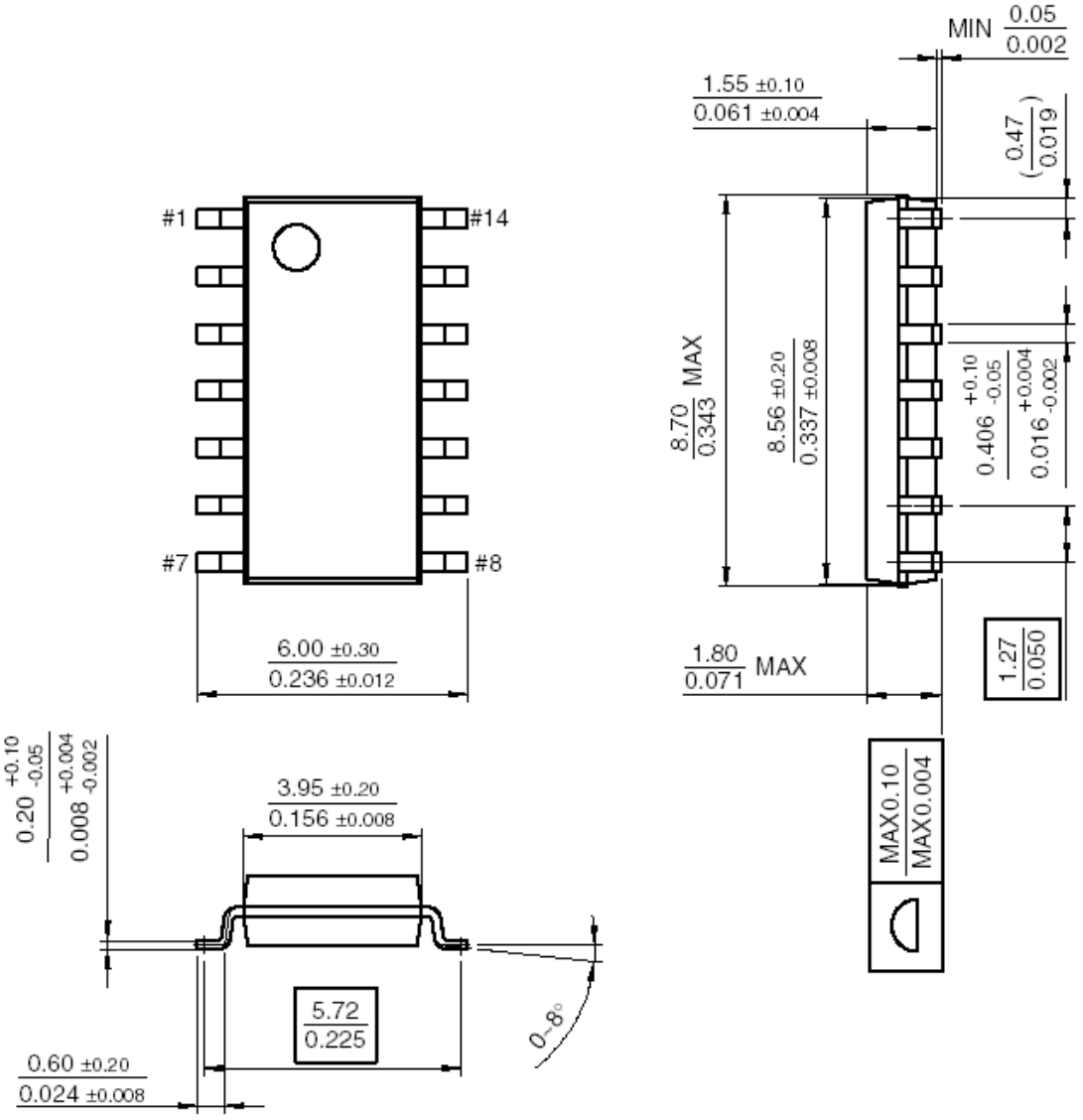
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.

Mechanical Dimensions

Package

Dimensions in millimeters/inches

14-SOP



Ordering Information

Product Number	Package	Operating Temperature	Packing
FAN7685N	14DIP	-40 ~ 125°C	Tube
FAN7686N			
FAN7687N			
FAN7687AN			
FAN7685M	14SOP	-40 ~ 125°C	Tube
FAN7686M			
FAN7687M			
FAN7687AM			
FAN7685MX	14SOP	-40 ~ 125°C	Tape & Reel
FAN7686MX			
FAN7687MX			
FAN7687AMX			

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2004 Fairchild Semiconductor Corporation