TPA6166A2 3.5-mm Jack Detect and Headset Interface IC

1 Features

- Ultra Low-Power, High-Performance DirectPath™ Class-G Headphone Amplifier
  - Ground-Centered Output Eliminates DC-Blocking Capacitors
  - 30 mW/Ch into 32 Ω / Ch at 1% THD+N
  - –42 dB to +6 dB Volume Control
  - 2.0 µV Output Noise at –42 dB Gain
  - 91-dB PSRR
  - Ground Loop Rejection for Reducing Crosstalk
- Fully Differential Mic Preamplifier With Variable Gain and 3.4-µV Low Noise
  - Integrated AC-Coupling Capacitor
  - Ground Loop Rejection for Reducing Headphone to Mic Crosstalk
- Choice of Two Mic Bias Voltages: 2.0 V and 2.6 V
  - 92-dB PSRR
  - Integrated Programmable Mic Bias Resistor
- Advanced Accessory Insertion, Removal, and Type Detection
- Passive Multi-button Support Using 10-Bit SAR ADC
  - Implements Proprietary Scheme to Reduce Error Caused by Audio Playback Signal in Presence of Finite Resistance on Headset Ground Return Path
- Integrated Level-4 IEC ESD Protection on Jack Connected Pins (on EVM)
- Ultra Low-Power Chip Shutdown Mode
- I^2C Interface
- Short-Circuit Protection
- 0.4-mm Pitch 25-Ball WCSP

2 Applications

- Smart Phones and Wireless Handsets
- Portable Tablets
- Notebook PCs and Docking Stations

3 Description

The TPA6166A2 single-chip headset interface IC simplifies the challenges of detecting what kind of device an end user has plugged into the headphone jack while delivering excellent audio quality. The device enables smaller end products by integrating a high-performance, low-power DirectPath variable-attenuation class-G stereo headphone amplifier, variable-gain microphone preamplifier with bias with advanced accessory detection circuitry, all in a tiny 5-mm × 5-mm terminal, 0.4-mm pitch WCSP package.

The class-G headphone amplifier maximizes battery life by adjusting the supply voltage of the headphone amplifier based on audio signal level. With 8-µV output noise at 0-dB gain and PSRR of 91 dB, the headphone amplifier provides excellent audio performance. DirectPath eliminates the need for DC-blocking capacitors. The microphone preamplifier has two programmable gains of 12 dB and 24 dB, and 3.4 µV input referred noise.

The microphone bias voltage has two programmable settings of 2 V and 2.6 V. The bias output drives up to 1.2 mA of current, has a low output noise of 2 µV, and 92-dB PSRR, providing excellent rejection of power supply noise in wireless handsets.

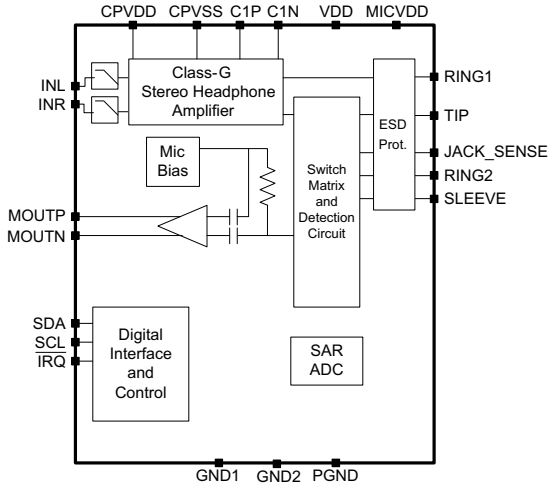
The advanced accessory detection algorithm automatically detects six supported accessories and enables or disables internal components.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6166A2	WSCP (25)	2.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2014) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

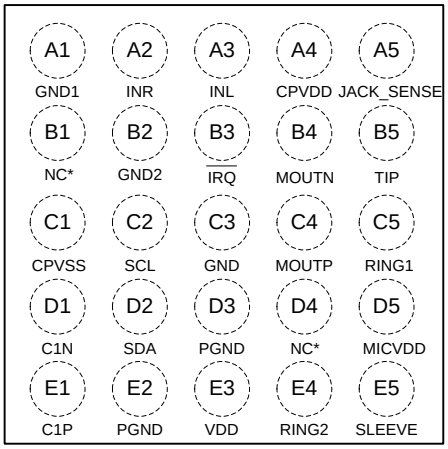
Changes from Original (January 2014) to Revision A **Page**

- Changed to new data sheet format ... 1
- Added specifications and application information ... 1
- Changed status to Production Data ... 1

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5 Pin Configuration and Functions

YFF Package
Top View



All NC pins should be left floating. Do not connect them to GND.

Pin Functions

PIN		I/O / TYPE	DESCRIPTION
NAME	NO.		
GND1	A1	P	Analog / digital ground 1
INR	A2	I	Headphone right channel input
INL	A3	I	Headphone left channel input
CPVDD	A4	I	Headphone charge-pump positive supply (internally generated). Connect a 1-µF capacitor to ground.
JACK_SENSE	A5	I/O	Connect to headset jack terminal 5 (for mechanical switch). If mechanical switch is not available, then this terminal can be kept floating.
NC (Floating)	B1	O	Leave floating (no connection)
GND2	B2	I	Ground 2 - Connect to ground 1 on board.
$\overline{IRQ}$	B3	O	Active low interrupt output
MOUTN	B4	O	Microphone preamplifier negative output
TIP	B5	O	Left headphone / line output. Connect to headset jack TIP (terminal 1).
CPVSS	C1	I	Headphone charge-pump negative supply (internally generated). Connect a 1-µF capacitor to ground.
SCL	C2	I	I^2C clock line
GND	C3	I	Connect to ground
MOUTP	C4	O	Microphone preamplifier positive output
RING1	C5	O	Right headphone / line output. Connect to headset jack RING1 (terminal 2).
C1N	D1	P	Charge pump flying capacitor positive terminal
SDA	D2	I/O	I^2C data line
PGND	D3, E2	P	Power ground
NC (Floating)	D4	O	Leave floating (no connection)
MICVDD	D5	P	Analog supply
C1P	E1	P	Charge pump flying capacitor negative terminal
VDD	E3	P	Analog / digital supply
RING2	E4	I/O	Connect to headset jack RING2 (terminal 3)
SLEEVE	E5	I/O	Connect to headset jack SLEEVE (terminal 4)

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range, T_A = 25°C (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, VDD	–0.3	2	V
Microphone supply voltage, MICVDD	–0.3	3.9	V
Output continuous total power dissipation	See *Thermal Information*		
Storage temperature, T_{stg}	–65	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
VDD	Supply voltage		1.7	1.9	V
MICVDD	Microphone supply voltage		2.4	3.6	V
T_A	Operating temperature		–25	85	°C
$C_{L,Max}$	Maximum load capacitance	Line Driver Application, R_L = 10 kΩ, A_V ≥ 0 dB, specified by design		470	pF
		Line Driver Application, R_L = 10 kΩ, A_V ≤ 0 dB, LO_EXT_STAB = 1, specified by design		470	
		Headphone Application, R_L = 32 Ω, specified by design		200	
T_J	Operating junction temperature		–25	150	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPA6166A2 YFF (WSCP) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18	
$R_{\theta JB}$	Junction-to-board thermal resistance	38	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	36	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

VDD =00 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_{HP} = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Input logic high	SDA, SCL		1.4			V
V_{IL}	Input logic low	SDA, SCL				0.4	V
V_{OL}	Output logic low	$\overline{IRQ}$	I_{OL} = 3 mA pullup current			0.2×VDD	V
$\|I_{IH}\|$	Logic high input leakage current	SDA, SCL				1	µA
$\|I_{IL}\|$	Logic low input leakage current	SDA, SCL				1	µA
$\|I_{OH}\|$	Logic high output leakage current	$\overline{IRQ}$	V_{IRQ} = 3.3 V			1	µA
Power consumption		Audio playback (both channels), no signal into 32 Ω	I_{VDD}		2.38		mA
			I_{MICVDD}		0.21		mA
			P_{CONS} (1)		4.91		mW
		Audio playback (both channels), 100-µW output into 32 Ω	I_{VDD}		3.74		mA
			I_{MICVDD}		0.21		mA
			P_{CONS} (1)		7.35		mW
		2-way call, no signal into 32 Ω	I_{VDD}		2.36		mA
			I_{MICVDD}		0.96		mA
			P_{CONS} (1)		6.35		mW
		2-way call, 100-µW output into 32 Ω	I_{VDD}		3.68		mA
			I_{MICVDD}		0.96		mA
			P_{CONS} (1)		8.74		mW
		Accessory not inserted	I_{VDD}		10.84		µA
			I_{MICVDD}		1.05		µA
			P_{CONS} (1)		22.7		µW
		Accessory not inserted, mechanical switch is open (JACK_SENSE=1)	I_{VDD}		150.9		µA
			I_{MICVDD}		1.05		µA
			P_{CONS} (1)		278.3		µW
		Accessory inserted and in sleep mode	I_{VDD}		108.1		µA
			I_{MICVDD}		1.06		µA
			P_{CONS} (1)		197.8		µW

(1) Total power consumption from VDD and MICVDD.

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6.6 Electrical Characteristics, Audio Amplifiers

VDD = 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_L = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HEADPHONE AND LINE-OUT AMPLIFIERS							
	Programmable gain range			-42		6	dB
$A_{V,Max}$		A_V = 6 dB		5.0	6.0	7.0	dB
$A_{V,Min}$		A_V = -42 dB		-43	-42	-41	dB
	Gain step size	-42 dB ≤ A_V ≤ 6 dB			1		dB
ΔA_V	Gain matching	Between left and right channels		–0.5		0.5	dB
	Mute attenuation				103.7		dB
P_O	Output power	THD+N = 1%, f = 1 kHz, R_L = 32 Ω, single channel on			29.1		mW
		THD+N = 1%, f = 1 kHz, R_L = 32 Ω, C both channels on			23.2		
		THD+N = 1%, f = 1 kHz, R_L = 16 Ω, single channel on			43.0		
		THD+N = 1%, f = 1 kHz, R_L = 16 Ω, The processing of Request 596221 was completed at 10:19 on 28 Jan 2015. Click here to access the data Click here to access the HTML data both channels on			30.2		
THD+N	Total harmonic distortion plus noise	R_L = 16 Ω, P_O = 10 mW, f = 1 kHz			0.021%		
		R_L = 16 Ω, P_O = 0.1 mW, f = 1 kHz			0.057%		
		R_L = 10 kΩ, V_{OUT} = 1 V_{RMS}, f = 1 kHz			0.014%		
PSRR	Power supply rejection ratio	f = dc, VDD = 1.7 V to 1.9 V, A_V = 0 dB		70	91		dB
		f = 217 Hz, 100 mV_{P-P} ripple on VDD			88		
		f = 10 kHz, 100 mV_{P-P} ripple on VDD			71		
E_N	Output noise(1)	A_V = 0 dB			8.0		μV_{RMS}
		A_V = -30 dB			2.0		
		A_V = -42 dB			2.0		
	Crosstalk between left and right channels	R_L = 16 Ω, f = 1 kHz, P_O = 5 mW			–56		dB
		R_L = 32 Ω, f = 1 kHz, P_O = 25 mW			–62		
R_{IN}	Amplifier input resistance				20		kΩ
V_{OOS}	Output offset voltage	A_V = 0 dB		–0.5		0.5	mV
$V_{OUT,Max}$	Max line output voltage	R_L = 10 kΩ			1		V_{RMS}
$f_{C,LPF}$	Input low-pass filter 3-dB cutoff frequency(2)	A_V = 0 dB			45.1		kHz
	Low-pass filter passband gain(2)	f = 10 Hz to 15 kHz, dc-coupled inputs with V_{CM} = 0 V			–0.4		dB
	Low-pass filter stopband gain(2)	f = 145 kHz			–16		dB
f_{CP}	Charge pump frequency				1.3		MHz
	Click and pop(1)	A_V = 0 dB, Volume Slewing Enabled, R_L = 32 Ω, peak voltage, 32 samples / second	Into shutdown		–83		dBV
			Out of shutdown		–69		
	Power consumption(3)	P_O = 0.5 mW, R_L = 32 Ω			6.2		mW
		P_O = 5 mW, R_L = 32 Ω, THRH = 1			13.3		
		P_O = 30 mW, R_L = 32 Ω, THRH = 0			56.9		
R_L	Minimum headphone load				32	7.8	Ω

(1) A-weighted
(2) Measured with respect to gain at 997 Hz
(3) Per output channel

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6.7 Electrical Characteristics, Mic Preamplifier and Bias

VDD = 1.8 V, MICVDD = 3.0 V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MICROPHONE BIAS							
V_{BIAS}	Microphone bias voltage	Programmed for high value, MICVDD ≥ 2.8 V		2.45	2.6	2.75	V
		Programmed for low value		1.88	2.0	2.12	
I_{OUT}	Max bias output current	Internal bias resistor bypassed (MICR = 011)			1.2		mA
R_{BIAS}	Bias output resistance	MICR = 000		2.09	2.2	2.31	kΩ
		MICR = 001		2.47	2.6	2.73	
		MICR = 010		2.85	3.0	3.15	
		MICR = 011			0.13		
E_N	Bias output noise(1)	Between SLEEVE and RING2, BW = 100 Hz to 7 kHz, 2.2 kΩ load between SLEEVE and RING2, MICR = 000, V_{BIAS} = 2.0 V			2.0		μV_{RMS}
PSRR	Power supply rejection ratio	Measured between SLEEVE and RING2, 2.2 kΩ load between SLEEVE and RING2, MICR = 000, V_{BIAS} = 2.6 V	f = dc, MICVDD = 2.8 V to 3.6 V		92		dB
			f = 2 kHz, 100 mV_{P-P} ripple, MICVDD = 3.0 V		73		
			f = 2 kHz, 100 mV_{P-P} ripple, MICVDD = 2.8 V		73		
MicZ	Microphone Capsule Impedance	Measured between Mic and GND before insertion		1500		20000	Ω
MICROPHONE PREAMPLIFIER							
A_V	Preamplifier gain	Programmed for high value, f = 997 Hz		23	24	25	dB
		Programmed for low value, f = 997 Hz		11	12	13	
E_N	Input referred noise(1)	f = 100 Hz to 7 kHz, A_V = 24 dB, Mic on SLEEVE, 2.2 kΩ load between SLEEVE and RING2, MICR = 000, V_{BIAS} = 2.0 V			3.4		μV_{RMS}
THD+N	Total harmonic distortion plus noise	V_{OUT} = 1 V_{RMS}			0.095 %		
PSRR	Power supply rejection ratio	Measured between MOUTP-MOUTN, 6.04 kΩ between SLEEVE and RING2, MICR = 010, V_{BIAS} = 2.0 V, f = dc, MICVDD = 2.4 V to 3.6 V		74			dB
		Measured between MOUTP-MOUTN, 2.2 kΩ between SLEEVE and RING2, MICR = 000, V_{BIAS} = 2.6 V	f = dc, MICVDD = 2.8 V to 3.6 V		109.5		
			f = 2 kHz, 100 mV_{P-P} ripple on MICVDD		78		
V_{CMO}	Output Common Mode	MICVDD = 2.4 V – 3.6V			0.4×MICVDD		V
$f_{C,LO}$	Lower -3 dB frequency of HPF(2)				20		Hz
$f_{C,HI}$	Upper -3 dB frequency of amplifier(2)				260		kHz

(1) A-weighted
(2) Measured with respect to gain at 997 Hz

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6.8 Timing Requirements

For I^2C interface signals and voltage power-up sequence, over recommended operating conditions (unless otherwise noted). Timing is specified by design.

			MIN	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states		400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		1.3		µs
t_{su1}	Setup time, SDA to SCL		100		ns
t_{h1}	Hold time, SCL to SDA		10		ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3		µs
t_{su2}	Setup time, SCL to start condition		0.6		µs
t_{h2}	Hold time, start condition to SCL		0.6		µs
t_{su3}	Setup time, SCL to stop condition		0.6		µs
t_{SP}	Pulse width of surpressed spike		0	50	ns

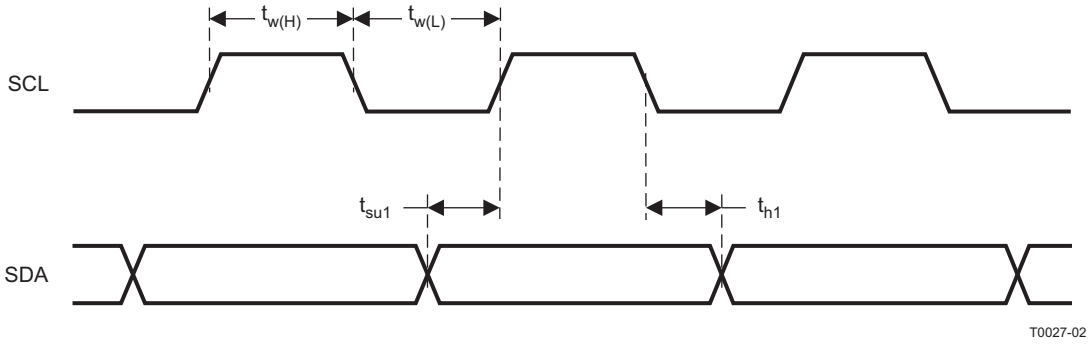


Figure 1. SCL and SDA Timing

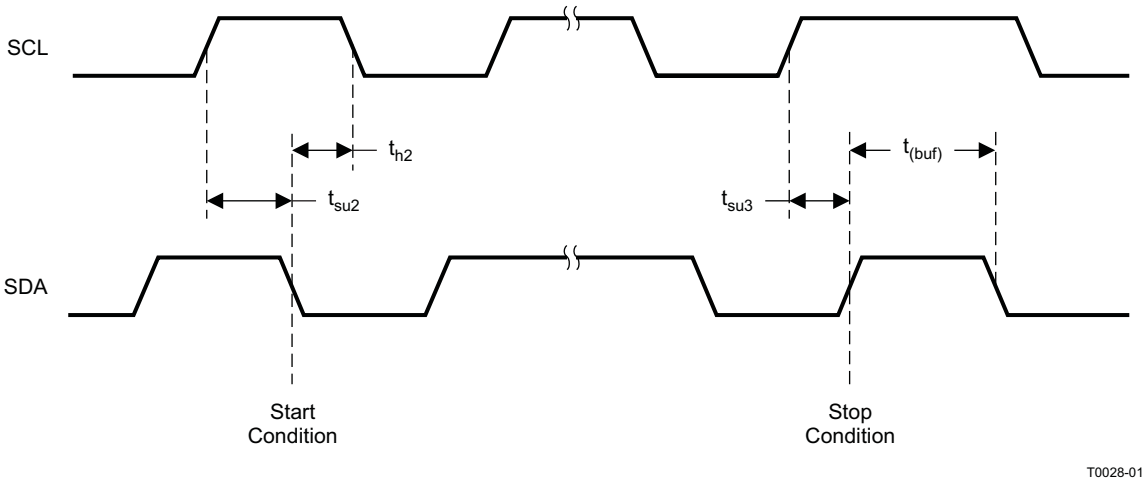
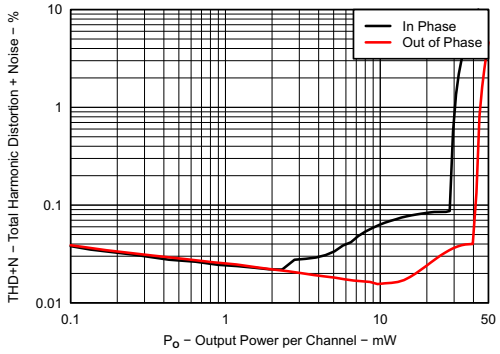


Figure 2. Start and Stop Conditions Timing

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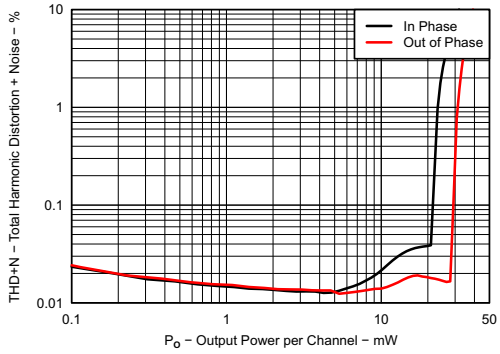
6.9 Typical Characteristics

VDD = 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_{HP} = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).



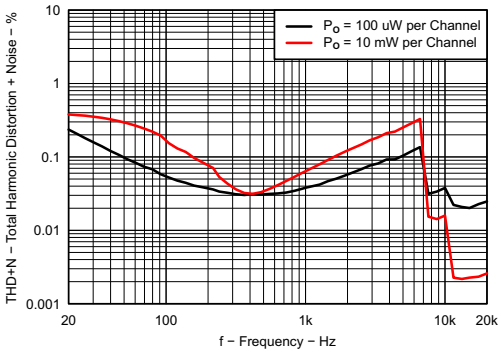
V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB
f - 1 kHz

Figure 3. Headphone Total Harmonic Distortion + Noise vs Output Power



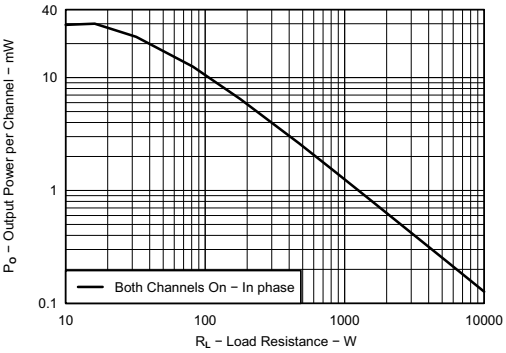
V_{DD} = 1.8 V R_L = 32 Ω Gain = 0 dB
f - 1 kHz

Figure 4. Headphone Total Harmonic Distortion + Noise vs Output Power



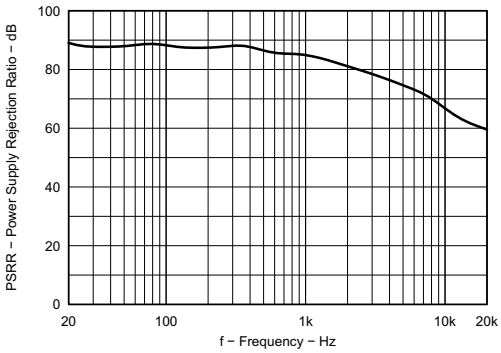
V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB

Figure 5. Headphone Total Harmonic Distortion + Noise vs Frequency



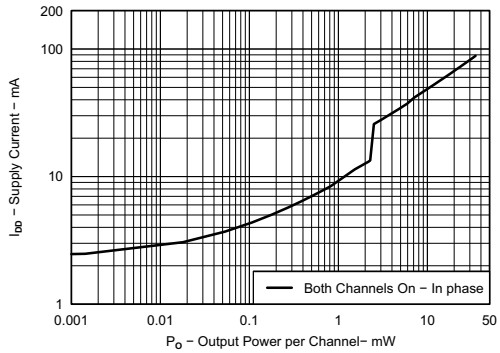
V_{DD} = 1.8 V f = 1 kHz Gain = 0 dB
THD+N = 1%

Figure 6. Headphone Output Power vs Load Resistance



V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB

Figure 7. Headphone Psrr vs Frequency



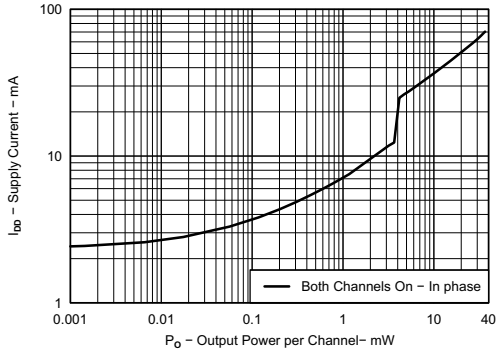
V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB
f = 1kHz THRH = 0

Figure 8. Headphone Supply Current vs Total Output Power

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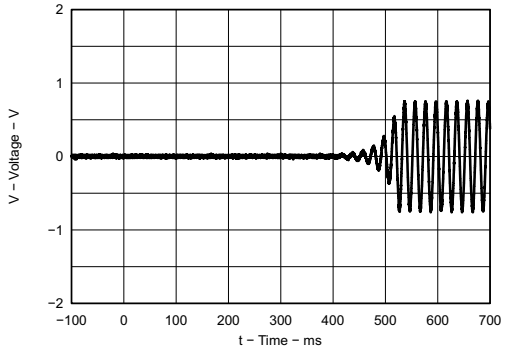
Typical Characteristics (continued)

VDD = 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_{HP} = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).



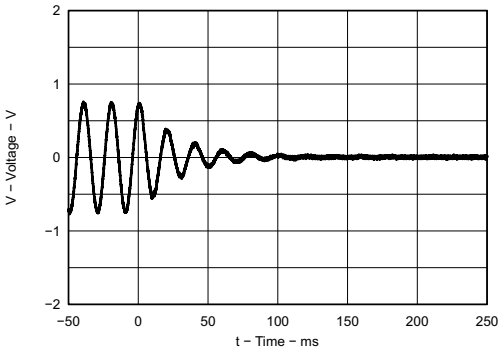
V_{DD} = 1.8 V R_L = 32 Ω Gain = 0 dB
f = 1kHz THRH = 0

Figure 9. Headphone Supply Current vs Total Output Power



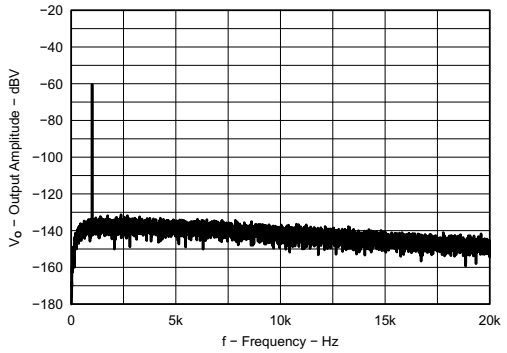
V_{IN} = 0.5 V_{RMS} R_L = 16 Ω
Volume slewing enabled
Device enabled at 0 ms

Figure 10. Headphone Start-up Waveforms vs Time



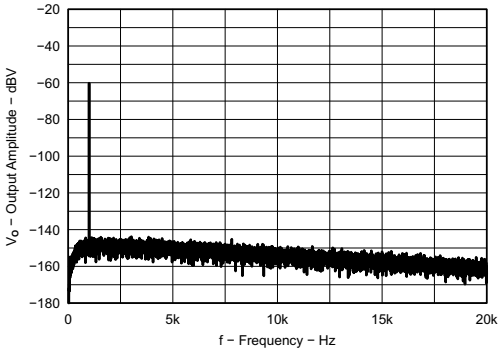
V_{IN} = 0.5 V_{RMS} R_L = 16 Ω
Volume slewing enabled
Device enabled at 0 ms

Figure 11. Headphone Shutdown Waveforms vs Time



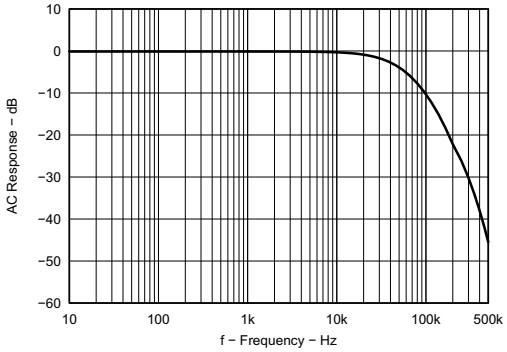
V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB
A weighted

Figure 12. Headphone Output Spectrum vs Frequency



V_{DD} = 1.8 V R_L = 16 Ω Gain = –30 dB
A weighted

Figure 13. Headphone Output Spectrum vs Frequency



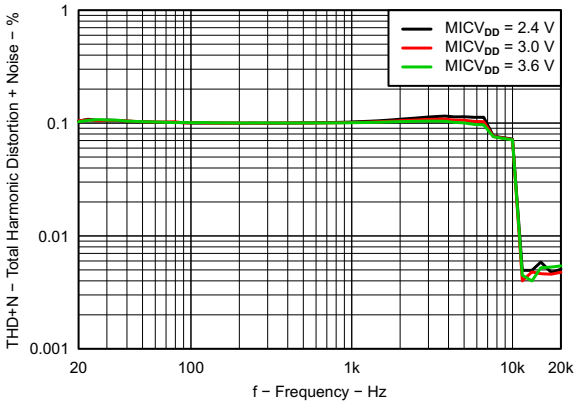
V_{DD} = 1.8 V R_L = 16 Ω Gain = 0 dB

Figure 14. Audio Filter Frequency Response

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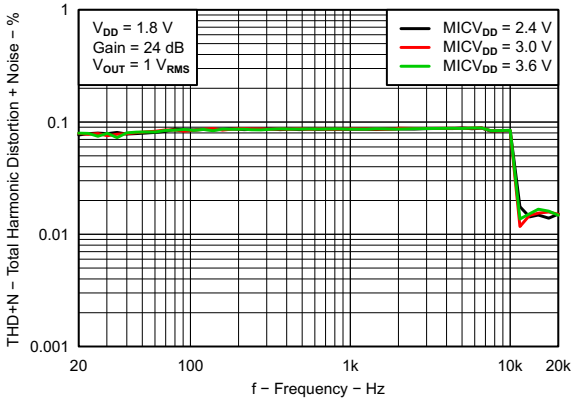
Typical Characteristics (continued)

VDD = 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_{HP} = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).



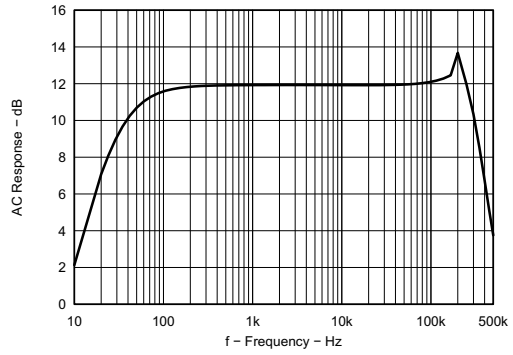
V_{DD} = 1.8 V V_{OUT} = 1 V_{RMS} Gain = 12 dB

Figure 15. Mic Preamplifier Total Harmonic Distortion + Noise vs Frequency



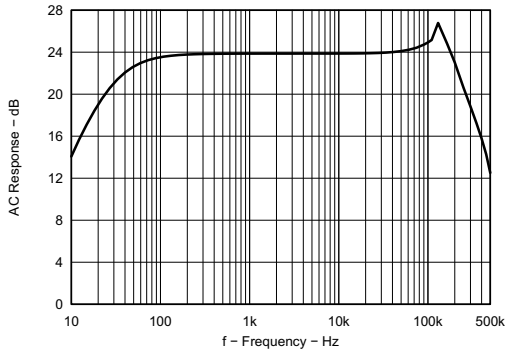
V_{DD} = 1.8 V V_{OUT} = 1 V_{RMS} Gain = 24 dB

Figure 16. Mic Preamplifier Total Harmonic Distortion + Noise vs Frequency



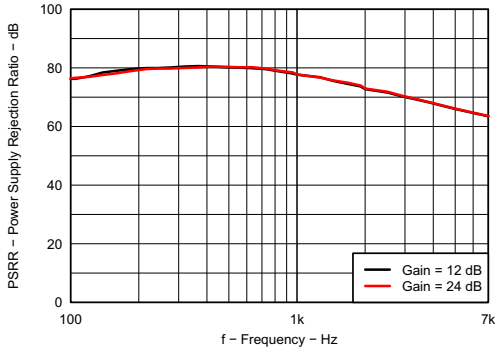
MIC V_{DD} = 3.0 V Gain = 12 dB

Figure 17. Mic Preamplifier Frequency Response



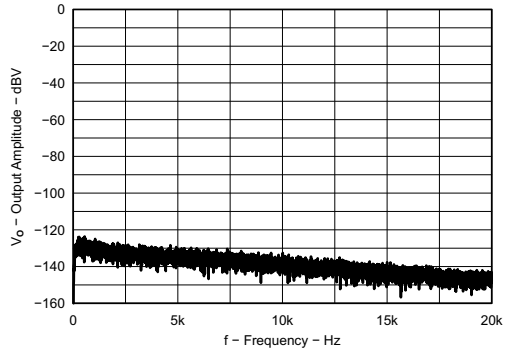
MIC V_{DD} = 3.0 V Gain = 24 dB

Figure 18. Mic Preamplifier Frequency Response



V_{DD} = 1.8 V MIC V_{DD} = 3.0 V

Figure 19. Mic Preamplifier + Micbias PSRR vs Frequency

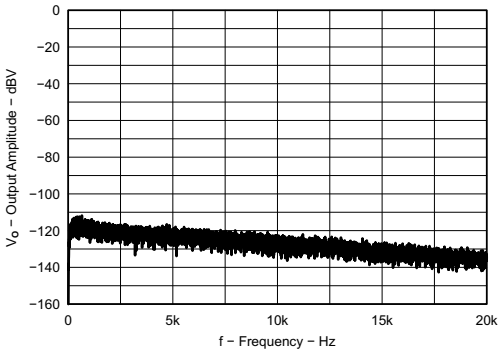


MIC V_{DD} = 3.0 V Gain = 12 dB No signal input

Figure 20. Mic Preamplifier + Micbias Output Frequency Spectrum

Typical Characteristics (continued)

VDD = 1.8 V, MICVDD = 3.0 V, A_V = 0 dB, C_{IN} = 0.47 µF, C_{FLY} = 1.0 µF, C_{CPVDD} = C_{CPVSS} = 1.0 µF, R_{HP} = 32 Ω, outputs in phase, T_A = 25°C (unless otherwise noted).



MIC V_{DD} = 3.0 V Gain = 24 dB No signal input

Figure 21. Mic Preamplifier + Micbias Output Frequency Spectrum

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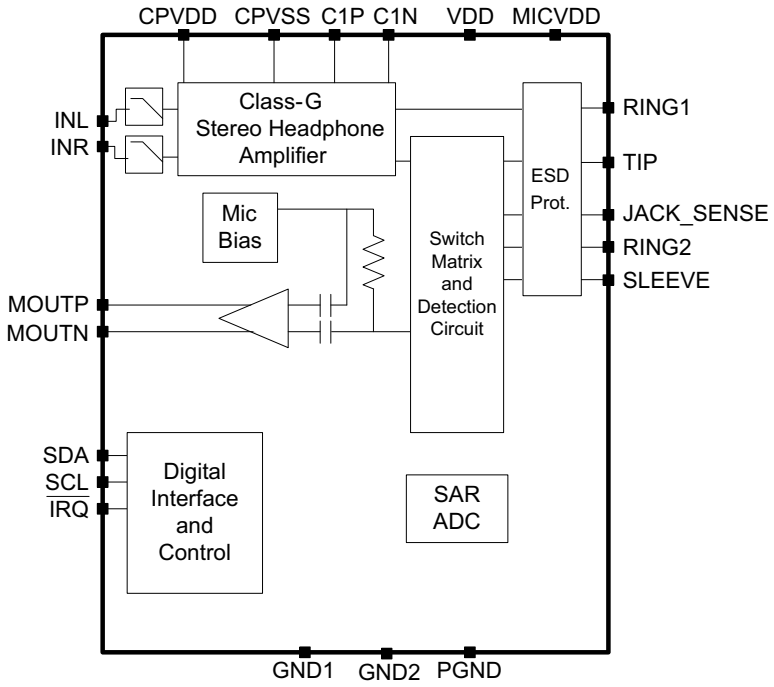
7 Detailed Description

7.1 Overview

The TPA6166A2 is a small device that serves a large number of complex functions in a portable audio device. It identifies an accessory plugged into the jack, and configures the internal subsystems to take full advantage of its capabilities.

- Headphone-jack accessory detection and identification
- Switch matrix
- Class-G ground-centered stereo headphone amplifier
- Mic preamplifier and bias
- SAR ADC for various analog sense functions
- ESD protection
- Convenient I^2C host interface

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 I^2C Interface

The TPA6166A2 I^2C address is 0x40 (7-bit).

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The most significant bit (MSB) is transferred first for the 8-bit address and data bytes. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

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Feature Description (continued)

Figure 22 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device, and then waits for an acknowledge condition. The TPA6166A2 holds SDA low during the acknowledge clock period to indicate acknowledgment. When acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pullup resistor must be used for the SDA and SCL signals to set the logic high level for the bus. When the bus level is 3.3 V, use pullup resistors between 1 kΩ and 2 kΩ.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 22.

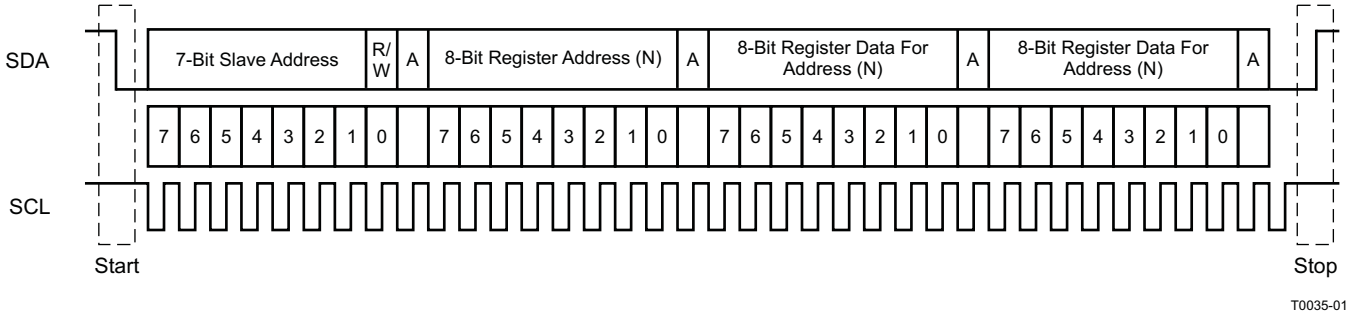


Figure 22. Typical I²C Sequence

7.3.1.1 Single and Multiple Byte Transfers

The serial control interface supports both single-byte and multiple byte read/write operations for all registers. During multiple-byte read operations, the TPA6166A2 responds with data, 1 byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledgments.

The TPA6166A2 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has occurred. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines the number of registers written.

7.3.1.2 Single-Byte Write

As Figure 23 shows, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA6166A2 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA6166A2 internal memory address being accessed. After receiving the register byte, the TPA6166A2 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the register byte, the TPA6166A2 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

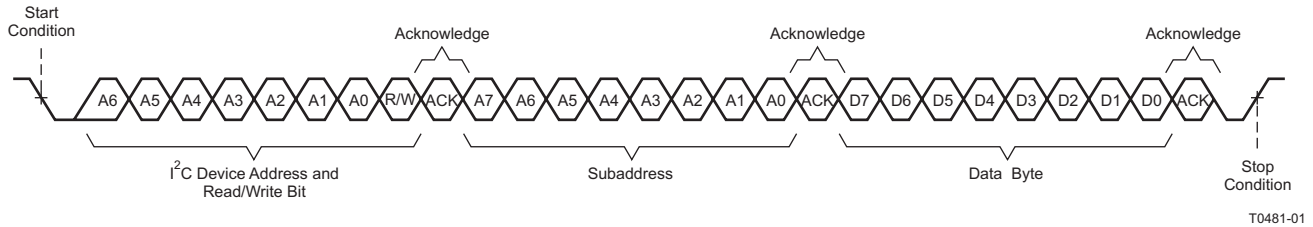


Figure 23. Single-Byte Write Transfer

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Feature Description (continued)

7.3.1.3 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA6166A2 as shown in Figure 24. After receiving each data byte, the TPA6166A2 responds with an acknowledge bit.

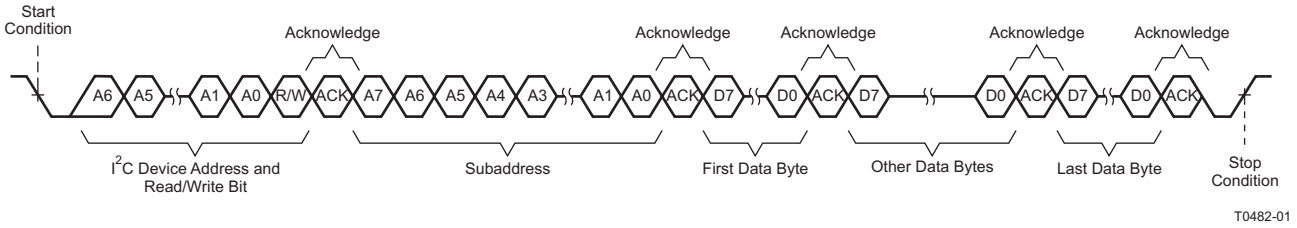


Figure 24. Multiple-Byte Write Transfer

7.3.1.4 Single-Byte Read

As Figure 25 shows, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually executed. Initially, a write is executed to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA6166A2 address and the read/write bit, the TPA6166A2 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA6166A2 issues an acknowledge bit. The master device transmits another start condition followed by the TPA6166A2 address and the read/write bit again. This time the read/write bit is set to 1, indicating a read transfer. Next, the TPA6166A2 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

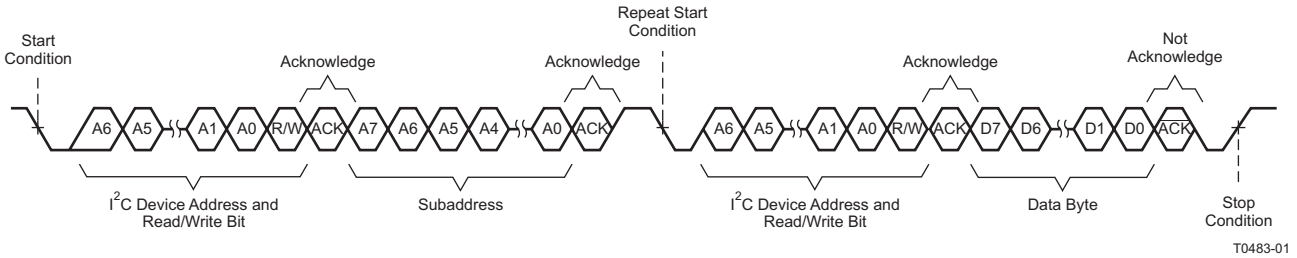


Figure 25. Single-Byte Read Transfer

7.3.1.5 Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA6166A2 to the master device as shown in Figure 26. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

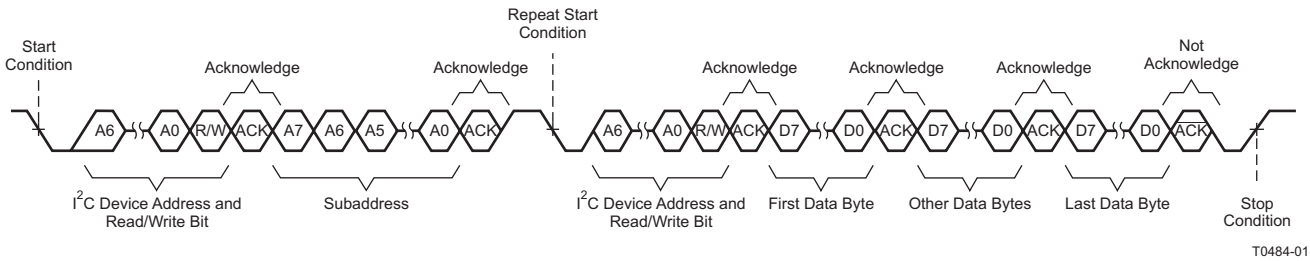


Figure 26. Multiple-Byte Read Transfer

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Feature Description (continued)

7.3.2 Accessory Detection

The TPA6166A2 has an advanced accessory jack detection circuitry which determines insertion, removal, as well as type detection of accessories with a 3.5-mm headset jack. The jack and its internal connections are shown in Figure 27.

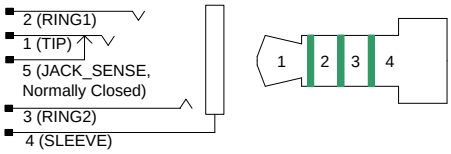


Figure 27. Connecting to a 3.5-mm Headset Jack

When the insertion of a jack is detected, the accessory type detection algorithm runs until two consecutive type detections produce the same result. In general, the type detection algorithm is not run again after this point of time. Hence, on-the-fly change of accessory type is not detected. The following accessories can be detected. Table 6 has specific detection details.

- Stereo Headset (HP with mic)
- Line Out Audio Cable
- Mono Headset
- Stereo Headphone
- Line Out Audio Cable

The limits of detection are shown in Table 1.

Table 1. Limits of Detection

PARAMETER	SYMBOL	MIN	MAX	UNIT
Cable Shield Capacitance	CCABLE	150	500	pF
Headphone Load Resistance	RHP	8	700/1500*	Ω
Audio Line Load Resistance	RLINE	10	50	kΩ
Microphone Load Resistance	RMIC	1.5	20	kΩ
Open/Float		200K || 70 pF	10 G || 5 pF	kΩ

As a result of accessory detection, appropriate blocks are automatically turned on ensuring lower possible power consumption. When accessory is removed, all blocks are turned off ensuring ultra low power. The TPA6166A2 achieves 22.7 µW when no accessory is inserted.

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7.3.3 Audio Playback Channel

The TPA6166A2 includes stereo audio channel with integrated low pass filter and class-G headphone amplifier. Figure 28 shows the block diagram for the Audio Channel. The channel includes volume control block. The volume level can be varied from +6 dB to –42 dB in 1-dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control, which can be achieved by setting Register 0x07, Bit 7 (L=R) to 1. Gain changes are implemented with a soft-stepping algorithm, which only changes the actual volume by one step in every 3.25 ms, either up or down, until the desired volume is reached.

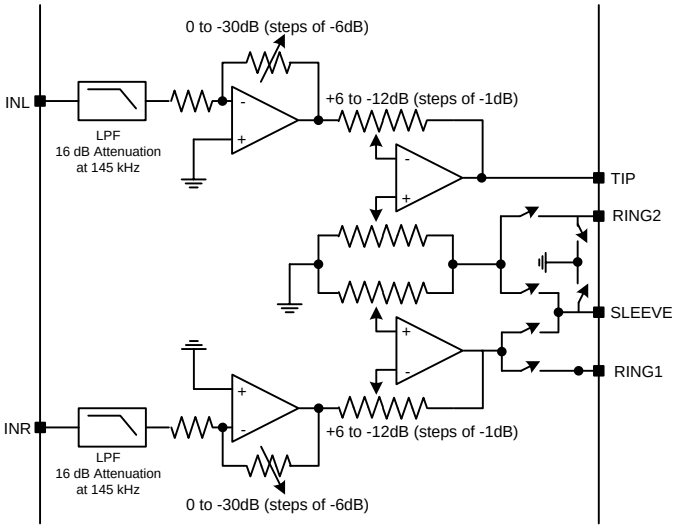


Figure 28. Audio Playback Channel

Because of soft-stepping, the system does not know when the audio channel has been actually muted. This may be important if the system wishes to mute the channel before making a significant change. To help with this situation, the device provides a flag back to the system through a read-only register bit that alerts the system when the part has completed the soft-stepping and the actual volume has reached the desired volume level. Soft-stepping feature can be disabled by setting Register 0x1E, Bit 5 ($\overline{\text{VSEN}}$) to 1.

The TPA6166A2 integrates switches on RING2 (terminal 3) and SLEEVE (terminal 4) to ground. Based on accessory detection result, either RING2 or SLEEVE is selected as accessory ground, and appropriate switch is turned on. As switches have finite resistance, it can give rise to crosstalk between left and right channel. The TPA6166A2 integrates ground loop rejection circuitry, which reduces crosstalk to a great extent.

The left channel audio output can be routed to TIP. For right channel, audio output is routed to RING1.

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7.3.3.1 Class-G Headphone Amplifier

Class-G is a linear amplifier using a modulating supply voltage. A high-efficiency step-down converter regulates the headphone amplifier supply voltage. The headphone amplifier supply voltage increases as the audio output voltage increases. This prevents signal clipping and distortion. The headphone amplifier supply voltage decreases during softer audio periods, reducing battery current and improving overall efficiency. The class-G amplifier has more than twice the efficiency of an equivalent class-AB amplifier. This increases battery life during audio playback.

Figure 29 shows the block diagram for the class-G headphone amplifier. The class-G control examines the amplifier output voltage and determines the optimum headphone supply voltage. CPVDD and CPVSS voltages increase fast enough to avoid any output clipping or distortion. The class-G control operates automatically and does not require programming.

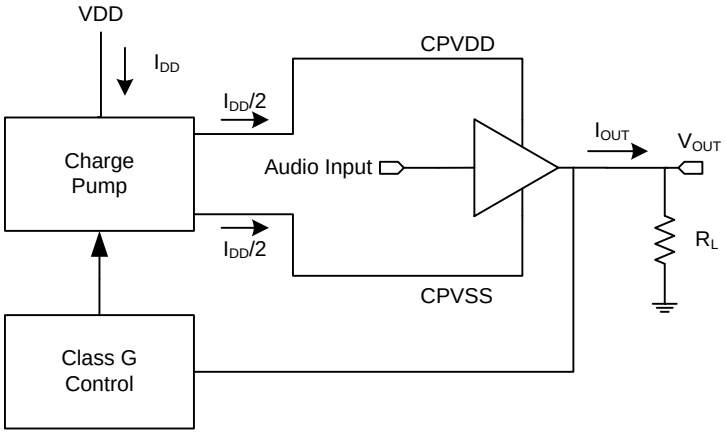


Figure 29. Class-G Headphone Block Diagram

7.3.3.1.1 Headphone Charge Pump

The TPA6166A2 includes a high-efficiency step-down charge pump and an inverting charge pump to generate power supplies for the headphone amplifier. These charge pumps use a common flying capacitor, thus minimizing components. The step-down charge pump regulates CPVDD; the inverting charge pump regulates CPVSS. These are designed to only drive the TPA6166A2 headphone amplifier. Do not use CPVDD or CPVSS as a voltage supply to drive an external device.

7.3.3.2 Out-of-Band and Input RF Noise Rejection

When using amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when the output out-of-band noise of the CODEC/DAC folds back into the audio frequency due to the limited gain bandwidth product of the audio amplifier. Single-ended RF noise can also fold back into the audio band thus degrading the audio signal even further.

The TPA6166A2 has a built-in low-pass filter to reduce CODEC/DAC out-of-band noise and RF noise, that could fold back into the audio frequency.

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7.3.4 Mic Channel

The TPA6166A2 includes microphone preamplifier with selectable gain of 12 dB and 24 dB. The device uses architecture, which removes requirement of external AC coupling capacitor by integrating it inside. The TPA6166A2 also includes Mic-bias with integrated bias resistor. A mic bias voltage can be programmed to 2.0 V or 2.6 V. Mic-bias resistor can be programmed to 2.2 kΩ, 2.6 kΩ, 3.0 kΩ or bypass. Based on accessory detection result, either RING2 (terminal 3 of jack) or SLEEVE (terminal 4 of jack) is selected as Mic input, and appropriate switch is turned on. Figure 30 shows the block diagram for the Mic Channel. Note that Bias resistor bypass mode, accessory detection, removal detection, and mic amp will not function.

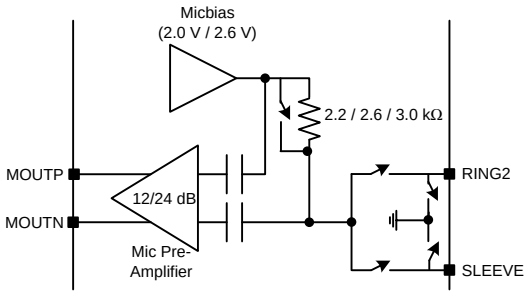


Figure 30. Mic Channel

7.3.5 Button Press Detection

The TPA6166A2 supports button press detection of different types:

- **Single button press/release**: When pressed, this typically creates an equivalent resistance of 1 Ω between RING2 and SLEEVE.
- **Passive button press/release**: When pressed, this creates an equivalent resistance between RING2 and SLEEVE. The TPA6166A2 reports press and release event along with resistance value (KEYDATA_DIV and KEYDATA in Register 0x17).

The impedance seen by the ADC is calculated using the following data

- Bias voltage
- Bias resistor
- Parallel impedance of the switch pressed and the microphone capsule impedance

The button press detection is done in a two-stage process. The device remains in a low power mode until a comparator is tripped. The comparator threshold is set to <1500Ω. Upon detection, the ADC is started to calculate the impedance pressed.

NOTE

The ADC will support impedances up to 375 Ω. Higher values are supported, but are much more susceptible to capacitance in the mic capsule, and could potentially provide erronious readings. At 375 Ω, Mic Capsule capacitances supported can be up to 50 nF.

For more details on configuring the device for Button Press Detection, see *Button Detection*.

7.4 Device Functional Modes

7.4.1 I²C Options

The TPA6166A2 I²C address is 0x40 (7-bit).

- *Single-Byte Write*
- *Multiple-Byte Write*
- *Incremental Multiple-Byte Write*
- *Single-Byte Read*
- *Multiple-Byte Read*

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Device Functional Modes (continued)

7.4.2 System in Shutdown Mode

Shutdown mode enables lowest power consumption from device. During this mode, accessory insertion, removal and type detection are not supported, but as soon as system comes out of shutdown, detection will work fine.

This mode can be programmed by programming /SHDN, register 0x1D (bit-7) to 0 For coming out of shutdown, /SHDN bit should be set to 1.

This will also rerun accessory detection algorithm.

7.4.3 System in Sleep Mode

This mode is enabled by programming SLEEP, register 0x1D (bit-6) to 1. During this mode, accessory insertion, removal, type and single-button press/release detection are supported.

7.4.3.1 Accessory Not Inserted

When the device is in AUTO mode (register 0x1E, bit 1-0 = 01), the device automatically configures itself in lowest possible power mode.

If accessory was previously inserted and is then removed, interrupt gets generated. Upon interrupt following sequence can be used to determine accessory removal and take appropriate action:

- Read control registers 0x00 to 0x02
- If JKIN, register 0x00, bit-7 = 0, then infer that accessory has been removed. Program SLEEP, register 0x1D, bit-6 = 1.

7.4.3.2 Accessory Inserted

When the device is in AUTO (register 0x1E, bit 1-0 = 01) and SLEEP (register 0x1D, bit-6 = 1) mode, the device automatically configures itself to minimize power consumption. For example: the mic preamplifier and headphone amplifiers are turned off, but removal and button-press detection continue to operate.

If the accessory was previously not inserted and is then inserted, interrupt gets generated. Upon interrupt following sequence can be used to determine accessory insertion and take appropriate action:

- Read control registers 0x00 to 0x02
- If JKIN, register 0x00, bit 7 = 1, then infer that accessory has been inserted.
- Read control register 0x19 to determine type of accessory

When the system wakes up and programs the device out of SLEEP mode, appropriate blocks will automatically turn on based on the type of accessory. System can also use accessory type to configure different routings (example: mix left and right channel for mono headset) and signal swing (depending on whether it is headphone or line-out load).

If the system was previously not in sleep mode and enters sleep mode, the following sequence should be followed to avoid pop noise on the headphone output:

- Enable interrupt due to volume slewing. This can be done by programming register 0x04, bit-5 (IVOL) = 1.
- If register 0x07, bit-7 (L=R) is 1, then program register 0x1E, bits 7-6 (left and right headphone control) = 00 and bits 1-0 (AUTO) = 00. Wait for interrupt due to volume slewing complete (VOL, register 0x00, bit-5).
- If register 0x07, bit-7 (L=R) is 0, then execute following steps:
  - If register 0x1E, bit-7=1, then program register 0x1E, bit-7 = 0 and bits 1-0 = 00. Wait for interrupt due to volume slewing complete (VOL, register 0x00, bit-5)
  - If register 0x1E, bit-6=1, then program register 0x1E, bit-6 = 0 and bits 1-0 = 00. Wait for interrupt due to volume slewing complete (VOL, register 0x00, bit-5).
- Program device in sleep mode (register 0x1D, bit-6, SLEEP = 1).
- Program device back in Auto mode (register 0x1E, bits 1-0, AUTO = 01.

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Device Functional Modes (continued)

7.4.3.3 Button Detection During Sleep Mode

During Sleep mode, single-button press/release detection is supported. Remaining buttons of passive multi-button headset (resistance of button higher than 0 Ω) are also detected as single button (resistance ≈ 0 Ω). For a button press, the system can use this event to wake up the system, and then program the device (details in *Button Detection*) to detect the second button press correctly.

Upon interrupt, the following sequence needs to be followed for button detection:

- Read control registers 0x00 to 0x02
- If MCSW, register 0x00, bit 1 = 1, then infer that button has been pressed/released. As long as button is pressed, MCSW continues to remain set.

7.4.4 System in Wake-Up Mode

This mode is enabled by programming SLEEP, register 0x1D (bit-6) to 0. During this mode, accessory insertion, removal, type, single button press/release and passive multi-button detection are supported.

7.4.4.1 Accessory Not Inserted

When the device is in AUTO mode (register 0x1E, bit 1-0 = 01), the device automatically configures itself in lowest possible power mode.

If accessory was previously inserted and is then removed, interrupt gets generated. Upon interrupt following sequence can be used to determine accessory removal and take appropriate action:

- Read control registers 0x00 to 0x02
- If JKIN, register 0x00, bit 7 = 0, then infer that accessory has been removed. Program SLEEP, register 0x1D, bit-6 = 1.

If a voice call is in progress, the system can use removal information to change from headset to handset mode. If audio is playing, the system can use the removal information to route audio to the speaker amplifier.

7.4.4.2 Accessory Inserted

When the device is in AUTO mode (register 0x1E, bit 1-0 = 01), the device automatically configures itself to turn on appropriate blocks. For example: for mono, only left headphone amp is turned on, whereas for stereo both left and right headphone amps are turned on).

If accessory was previously not inserted and is then inserted, an interrupt is generated. Upon an interrupt, the following sequence can be used to determine that an accessory insertion has occurred and take appropriate action:

- Read control registers 0x00 to 0x02
- If JKIN, register 0x00, bit-7 = 1, then infer that accessory has been inserted.
- Read control register 0x19 (bit 6-0, STATE) to determine type of accessory. Program SLEEP, register 0x1D, bit-6 = 0 (if audio is playing or in voice call).

If a voice call is in progress, the system can use the insertion information to change from handset to headset mode. If audio is playing on speaker, the system can use the insertion information to route audio to headset (accessory).

Accessory type detection can be used to configure different routings (example: for mono headset, mix left and right channel and route it on INL of the TPA6166A2) and signal swing (depending on headphone or line-out load).

7.4.4.3 Audio Not Playing or Not in Voice Call

During this mode, lowest power option is to program the device in SLEEP mode (register 0x1D, bit 6 = 1). This will power down mic preamplifier and headphone amplifiers. If audio starts playing or a voice call starts, SLEEP can be programmed to 0. To minimize pop and clock, headphone amplifiers go through power up sequencing where it first powers up in MUTE and then soft step volume to set gain with slew rate of 3.25 ms/dB. Volume slewing can be disabled by programming register 0x1E, bit-5 to 1.

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Device Functional Modes (continued)

7.4.4.4 High Impedance Line Out Load

The TPA6166A2 detects 50-kΩ max impedance as a line-level output. A value above 50 kΩ is treated as float and the corresponding amplifier is kept powered down. If higher value line-out load must be supported, the following sequence can be used, when accessory insertion is detected:

- Register 0x19 (bit 6-0, STATE) value is already available immediately after insertion detection (to determine type of accessory). Check if STATE have one of following values
  - 0x1B
  - 0x1C
  - 0x1F
- If value matches one of the above, the following register writes should be done
  - Register 0x19 (bits 7-0) = 0x1A
  - Register 0x19 (bits 7-0) = 0x9A

The preceding sequence will power up both left and right headphone amplifiers. After this step, the device will again go into automatic mode, where blocks will be powered up and down based on detection result.

7.4.4.5 Button Detection

If only single-button detection is required, following sequence can be used when interrupt is generated:

- Read control registers 0x00 to 0x02
- If MCSW, register 0x00, bit 1 = 1, then infer that button has been pressed (PRESS, register 0x01, bit-1 = 1) or released (PRESS, register 0x01, bit-1 = 0)

If both single-button and passive multi-button detection are required, the following sequence can be used:

- As soon as the device is in wake-up mode (SLEEP = 0), following register writes should be done
  - Register 0x1C (bit-7) = 1
  - Register 0x66 (bits 7-0) = 0xF1
  - Register 0x6F (bits 7-0) = 0x01
  - Register 0x66 (bits 7-0) = 0x00
- Upon interrupt, following sequence can be used:
  - Read control registers 0x00 to 0x02
  - If MCSW (register 0x00, bit-1) = 1, then infer that single-button has been pressed (PRESS, register 0x01, bit-1 = 1) or released (PRESS, register 0x01, bit-1 = 0).
  - If MCSW = 0 and KEY (register 0x01, bit-2) = 1, then infer that passive multi-button has been pressed (PRESS, register 0x01, bit-1 = 1) or released (PRESS, register 0x01, bit-1 = 0).
  - If passive multi-button press is detected, value of button resistance can be known by reading register 0x17 (KEYDATA_DIV and KEYDATA). Equation for resistance calculation is shown in description of control register 0x17
- When device needs to be taken to Sleep or Shutdown mode or accessory removal gets detected, the following additional registers should be programmed to minimize power consumption
  - Register 0x1C (bit-7) = 0
  - Register 0x66 (bits 7-0) = 0xF1
  - Register 0x6F (bits 7-0) = 0x00
  - Register 0x66 (bits 7-0) = 0x00

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7.5 Register Maps

7.5.1 Register Functional Overview

The TPA6166A2 when configured in fully automated mode (bits 1-0, register 0x1E set to 01) automatically enables and disables relevant blocks (headphone, mic preamplifier, mic bias, and so forth) based on result of accessory detection.

Table 2. Register Descriptions for Software Developers

Registers	Read/Write	Function
0x00, 0x01, 0x02	R	Configuration and device status registers. These registers are used to report the makeup of the inserted jack as well as report when a microphone switch has been pressed or the jack has been removed. The TPA6166A2 uses the status registers and IRQ to report the status of various device functions. The status registers bits are set when their respective event occurs and cleared upon reading the register. Device status can be determined either by polling the registers or configuring the IRQ to go low when specific events occur and then reading these registers on IRQ.
0x04, 0x05	R/W	Interrupt mask registers. These registers determine which bits in the status registers (0x00 – 0x02) will trigger IRQ to go low. Once IRQ goes low, it becomes high when status register responsible for IRQ generation gets read.
0x07, 0x08	R/W	Headphone volume setting registers. These registers independently control and report the gain of the left and right headphone amplifiers. There is an option to have right channel gain track left channel gain setting. This can be done by setting bit 7 in control register 0x07.
0x09	R/W	Microphone bias and preamplifier setting register. This register is used to program different settings related to microphone preamplifier and microphone bias.
0x0B	R	Revision ID register
0x15, 0x16	R/W	Passive multi-button debounce and delay settings. Debounce helps in filtering any unwanted noise/glitches in system which can cause wrong button detection. The delay register sets the time-out that the mic button press is masked from the system. At the end of the delay time, the TPA6166A2 checks to see if accessory is still present. If accessory is not present, then it does not generate interrupt corresponding to button press. This prevents accessory removal from being detected as a button press (due to RING2 and SLEEVE getting shorted during removal).
0x17	R	Passive multi-button data register. For resistance calculations, refer to control register description in data sheet
0x19	R/W	State Register. Indicates type of accessory (headset with/without mic, headphone, line-out, no accessory inserted, and so forth). If AUTO mode (default) is turned on, relevant blocks are automatically turned on/off based on type of accessory.
0x18, 0x1A	R/W	Accessory detection test hardware settings. Provides fine-tuning for accessory detection algorithm.
0x1C	R/W	Clock control for passive multi button. Needed to be configured along with few other registers for passive multi-button to work. Refer to control register description in data sheet for details.
0x1D, 0x1E	R/W	Enable settings register. This contains all of the bits that control the separate functional blocks. The system can either directly control these bits, or it can allow device to automatically configure itself and report which blocks are enabled. When the AUTO bits (B1-B0) are set to 01 or 10, this register is read only. The block enable bits do not need to be set to detect accessory insertion/removal.
0x03, 0x06, 0x0A, 0x0C, 0x0D – 0x14, 0x1B, 0x1F	R/W	Reserved. Always write recommended values to these registers.

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7.5.2 Initialization

7.5.2.1 Reserved Registers

Always program values based on Table 3 (registers in bold must be programmed).

Table 3. Initialization of Reserved Registers

Register Address	Value (Hex)	Comments
0x03	00	Same as default
0x06	00	Same as default
0x0A	00	Same as default
0x0C	1C	Same as default
0x0D	00	Same as default
0x0E	00	Same as default
0x0F	00	Same as default
0x10	00	Same as default
0x11	00	Same as default
0x12	01	Default is 00
0x13	45	Default is 00
0x14	00	Same as default
01B	00	Default is not defined
0x1F	00	Same as default

7.5.2.2 Fixed Registers

Values for these registers will likely remain same all the time. Table below have recommended settings for registers. Based on system requirement, it is possible that slightly different values need to be programmed.

Table 4. Typically Fixed Registers

Register Address	Value (Binary)	Comments
0x04	1100 0010	Same as default
0x05	0000 0100	Same as default
0x09	$B_7B_6B_5B_4B_3B_200$	Bits 1-0 must be programmed to 00. Bits 7-2 values based on system need (Example: 0100 01 for 24-dB mic preamplifier gain, 2.2-kΩ bias resistor and 2.6-V bias voltage)
0x15	1111 1111	Debounce time of ~64 ms. If this causes too much delay for button press detection, then lower value can be considered.
0x16	1111 1111	Debounce time of ~256 ms. If this causes too much delay for button press detection, then lower value can be considered.
0x18	1100 0000	Same as default
0x1A	1001 0101	Same as default

7.5.2.3 Other Registers

Values for these registers will likely be changed by system on-the-fly depending on mode of operation

Table 5. Commonly Used Registers

Register Address	Value (Binary)	Comments
0x1E	0001 10001	TI recommends programming this register first before anything else in this table
0x07	0000 0100	Bits 6-0 values based on system need (Example: 011 1001 for 0dB gain). These bits can be changed on-the-fly for controlling volume.
0x08	$1B_6B_5B_4B_3B_2B_1B_0$	Bits 6-0 are don't care if bit 7 of register 0x1E is set to 1
0x1C	0000 0000	Bit-7 will likely change based on mode, if passive multi-button needs to be supported.
0x1D	1100 0000	

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7.5.3 Typical Use Case Modes

After initialization, registers described in Section will need to be programmed during different modes. In addition, the following registers will be used for checking status, configuration and measurement data:

- 0x00
- 0x01
- 0x02
- 0x17
- 0x19

Upon interrupt, the system host should read registers 0x00, 0x01 and 0x02 to determine the interrupt source and respond appropriately.

- System In Shutdown Mode
- System In Sleep Mode
  - Accessory Not Inserted
  - Accessory Inserted
  - Button Detection During Sleep Mode
- System In Wake-Up Mode
  - Accessory Not Inserted
  - Accessory Inserted
  - Audio Not Playing Or Not In Voice Call
  - High Impedance Line-Out Load
  - Button Detection
- Accessory Insertion/Removal Detection Without Using Jack_sense
  - Scheme 1
  - Scheme 2
- Special Headset Detection

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7.5.4 Recommended Software Flow Chart

The flow chart in Figure 31 gives a conceptual view of how software can be organized for different modes.

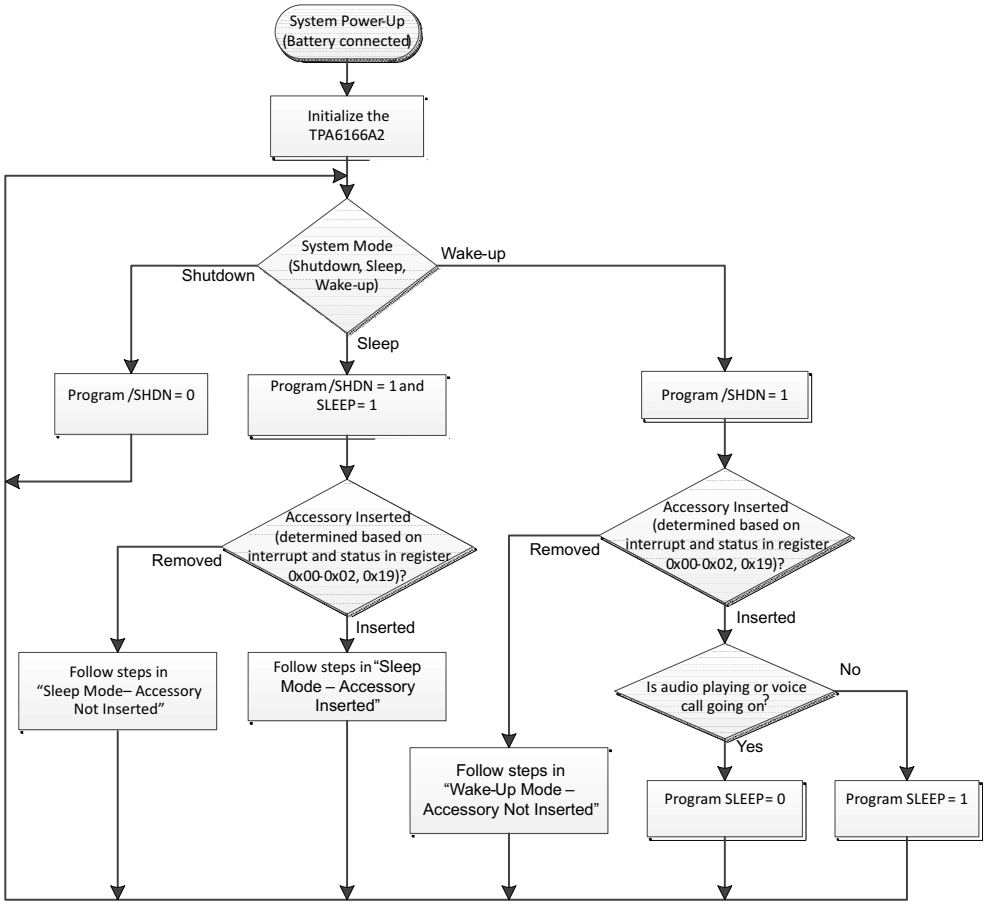


Figure 31. Recommended Software Flow Chart

7.5.5 Register Map Summary

The TPA6166A2 I²C address is 0x40 (7-bit). See *I²C Interface* for more details.

REGISTER		READ / WRITE	DEFAULT	FUNCTION
DEC	HEX			
0	0x00	R	0x00	Configuration and Device Status Register 1
1	0x01	R	0x00	Configuration and Device Status Register 2
2	0x02	R	0x00	Configuration and Device Status Register 3
3	0x03	R	0x00	Reserved. Always write 0x00
4	0x04	R/W	0x00	Interrupt Mask Register 1
5	0x05	R/W	0x00	Interrupt Mask Register 2
6	0x06	R/W	0x00	Reserved. Always write 0x00
7	0x07	R/W	0xC0	Headphone Volume Control Register 1
8	0x08	R/W	0x40	Headphone Volume Control Register 2
9	0x09	R/W	0x03	Microphone Bias Control Register
10	0x0A	R	0x00	Reserved
11	0x0B	R	0x30	Revision ID Register
12	0x0C	R/W	0x1C	Reserved.
13	0x0D	R/W	0x00	Reserved. Always write 0x00

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REGISTER		READ / WRITE	DEFAULT	FUNCTION
DEC	HEX			
14	0x0E	R/W	0x00	Reserved. Always write 0x00
15	0x0F	R/W	0x00	Reserved. Always write 0x00
16	0x10	R/W	0x00	Reserved. Always write 0x00
17	0x11	R/W	0x00	Reserved. Always write 0x00
18	0x12	R/W	0x00	Reserved. Always write 0x01
19	0x13	R/W	0x00	Reserved. Always write 0x45
20	0x14	R	0x00	Reserved.
21	0x15	R/W	0x00	Keyscan Debounce Register
22	0x16	R/W	0x00	Keyscan Delay Register
23	0x17	R	0x00	Passive Multi Button Keyscan Data Register
24	0x18	R/W	0x00	Jack Detect Test Hardware Settings
25	0x19	R/W	0x80	State Register
26	0x1A	R/W	0x15	Jack Detect Test Hardware Settings
27	0x1B	R		Reserved
28	0x1C	R/W	0x01	Clock control. Initiialize it to 0x00
29	0x1D	R/W	0x00	Enable Register 1
30	0x1E	R/W	0x01	Enable Register 2
31	0x1F	R	0x00	Reserved

Registers 0x00, 0x01, and 0x02 are used to report the makeup of the inserted jack as well as report when a microphone switch has been pressed or the jack has been removed. The TPA6166A2 uses the status registers and $\overline{IRQ}$ to report the status of various device functions. The status registers bits are set when their respective event occurs and cleared upon reading the register. Device status can be determined either by polling the registers or configuring the $\overline{IRQ}$ to go low when specific events occur. Registers 0x04 and 0x05 determine which bits in the status register will trigger $\overline{IRQ}$ to go low. Once $\overline{IRQ}$ goes low, it becomes high when status register responsible for $\overline{IRQ}$ generation gets read.

Use a minimum 2-ms wait time after TPA6166A2 power supplies are stable before reading or writing to any register.

7.5.6 Detailed Register Descriptions

7.5.6.1 Register 0x00: Config and Device Status Register 1

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	JKIN	R	0	Jack Detected. JKIN changes state when the jack detect circuit senses any valid accessory inserted. 0 = No valid accessory detected. 1 = Valid accessory detected. Set the IJKIN interrupt mask to alert the system when the JKIN value has changed. During shutdown mode ($\overline{SHDN}$ = 0), JKIN will report whether mechanical switch (JACK_SENSE) is open or closed. STATE value will continue to remain 0x00.
6	DDONE	R	0	Jack Configuration Detect Done. DDONE changes state when the jack detect algorithm is done running and the jack config is known and reported in the Config and Status1 registers. “RESET WHEN READ”. 0 = Jack detect algorithm is not complete. 1 = Jack detection algorithm is complete. When change in configuration happens, it is set again. Set the IDDONE interrupt mask to alert the system when the DDONE is set.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
5	VOL	R	0	Volume Slew Complete VOL goes high after the headphone volume has slewed to its final programmed value. VOL will set every time a gain change is complete whether the gain change is positive or negative. Ramp the volume down and wait for VOL to set to ensure clickless turnoff. It is also generated during power down/up and mute/unmute, where gain changes from/to present value to/from minimum value. RESET WHEN READ. 0 = No volume slewing sequences have completed since the status register was last read. 1 = Volume slewing complete.
4		R	0	Reserved. Write only default value.
3	MIC_IN	R	0	Microphone Connected/Disconnected MIC_IN reports when a microphone is connected or removed. Set the IMIC interrupt mask to alert the system when the mic load status has changed. 0 = Microphone is removed. 1 = Microphone is connected.
2	JACK_SENSE	R	0	JACK_SENSE (terminal 5) Status JACK_SENSE reports the mechanical jack switch status. For an operational mechanical jack switch, JACK_SENSE and JKIN will flag at the same time. If the switch is broken, or if the jack is not plugged in all the way, JACK_SENSE and JKIN will not report the same value. The JACK_SENSE bit also reports when a jack has been removed. Set the IJACK_SENSE interrupt mask bit to signal the system when the status of JACK_SENSE changes. 0 = Mechanical jack switch shows removed. 1 = Mechanical jack switch shows connected.
1	MCSW	R	0	Microphone Switch Status MCSW goes high when the microphone bias goes to low for the debounce period plus the delay period. This happens when a switch shorts across the microphone, pulling the micbias node down, indicating a keypress from a hook switch, ADC ≤ 9 LSB (Calculated assuming 2.6 kΩ bias resistor). Also during sleep mode, but without delay time. RESET WHEN READ. MCSW is also used when a button is pressed while in sleep mode. 0 = No change in mic bias, no switch press. 1 = Mic bias has been pulled to ground and debounced since the last status read. Debounce time set by KEY_DEB. Delay time set by KEY_DEL.
0		R	0	Reserved. Write only default value.

7.5.6.2 Register 0x01: Config and Device Status Register 2

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	LINE_L	R	0	Line-Level Audio on TIP Detected 0 = Line audio load on TIP not detected. 1 = Line audio load on TIP detected.
6	LINE_R	R	0	Line Level Audio on RING1 Detected 0 = Line audio load on RING1 not detected. 1 = Line audio load on RING1 detected.
5	HP_L	R	0	Headphone on TIP Detected 0 = Headphone load on TIP not detected. 1 = Headphone load on TIP detected.
4	HP_R	R	0	Headphone on RING1 Detected 0 = Headphone load on RING1 not detected. 1 = Headphone load on RING1 detected.
3		R	0	Reserved. Write only default value.
2	KEY	R	0	Passive Multi Button Headset KEY Status KEY reports when the passive multibutton or single button has been pressed. Data is available in KEYDATA. RESET WHEN READ. 0 = No button pressed. 1 = Button has been pressed/released. Debounce and delay times have occurred.

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BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
1	PRESS	R	0	Key Press/Release Event This bit reports whether the current interrupt caused by the KEY or MCSW status bits, is the result of a press or release. 1 = Current interrupt caused by a press. 0 = Current interrupt caused by a release. When interrupt is caused by release, there is a delay of 0.5 ms in resetting this bit from time interrupt is generated and KEY status bit is set. This bit is not set when device is in Sleep Mode.
0		R	0	Reserved. Write only default value.

7.5.6.3 Register 0x02: Config and Device Status Register 2

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-4		R	0000	Reserved. Write only default values.
3	RESET	R	0	Device Reset Status Reports whether TPA6166A2 got reset after last register read. It can be used to restore control register values, if device gets reset due to ESD strike. Interrupt is generated to alert the system when this situation occurs. Interrupt is cleared when this register bit is read. RESET WHEN READ. 0 = TPA6166A2 has not reset since last register read. 1 = TPA6166A2 has been reset since last register read.
2		R	0	Reserved. Write only default value.
1-0	GND	R	00	Jack Common Location Identifier The two GND bits tell the system whether the jack's common connection is at RING2 or SLEEVE. GND is also used to indicate when a jack has been removed. 00 = No common connection sensed, jack has been removed or nothing has been inserted yet. 01 = The common jack connection is RING2. 10 = The common jack connection is SLEEVE. 11 = Common on both RING2 and SLEEVE.

7.5.6.4 Register 0x03: Reserved Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved.

7.5.6.5 Register 0x04: Interrupt Mask Register 1

The interrupt mask registers control which status bits will flag a system interrupt. Setting an interrupt mask bit will cause IRQ to pull low whenever the target status bits set.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	IJKIN	R/W	0	Jack Detect Interrupt Enable 0 = Disabled 1 = Enabled
6	IDDONE	R/W	0	Jack Configuration Detect Done Interrupt Enable 0 = Disabled 1 = Enabled
5	IVOL	R/W	0	Volume Slew Interrupt Enable 0 = Disabled 1 = Enabled
4		R	0	Reserved. Write only default value.
3	IMIC	R/W	0	Microphone Interrupt Enable 0 = Disabled 1 = Enabled

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BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
2	IJACK_SENSE	R/W	0	JACK_SENSE Status Interrupt Enable 0 = Disabled 1 = Enabled
1	IMCSW	R/W	0	Mic Switch Interrupt Enable 0 = Disabled 1 = Enabled
0		R/W	0	Reserved. Always write 0.

7.5.6.6 Register 0x05: Interrupt Mask Register 2

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	ILINE_L	R/W	0	Line Level Audio Load TIP Interrupt Enable 0 = Disabled 1 = Enabled
6	ILINE_R	R/W	0	Line Level Audio Load RING1 Interrupt Enable 0 = Disabled 1 = Enabled
5	IHP_L	R/W	0	Headphone Audio Load TIP Interrupt Enable 0 = Disabled 1 = Enabled
4	IHP_R	R/W	0	Headphone Audio Load RING1 Interrupt Enable 0 = Disabled 1 = Enabled
3		R	0	Reserved. Write only default value.
2	IKEY	R/W	0	KEY Interrupt Enable 0 = Disabled 1 = Enabled
1		R/W	0	Reserved. Write only default value.
0		R/W	0	Reserved. Always write 0.

7.5.6.7 Register 0x06: Reserved Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved.

7.5.6.8 Register 0x07: Headphone Volume Register 1

The headphone volume registers independently control and report the gain of the left and right headphone amplifiers. Set Bit 7 in register 0x07 to have the right channel gain track the left.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	L=R	R/W	1	Left/Right Tracking 0 = The right channel volume control is independent of the left. 1 = The left and right volume controls track each other allowing for only one register to be written to change both channel volumes. Control both volume controls by writing to LVOL.
6	MUTEL	R/W	1	Left Headphone Mute 0 = Disable. 1 = Enable, output is muted.

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BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
5-0	LVOL	R/W	00 0000	Left Headphone Volume Control 00 xxxx = –42 dB 01 0000 = –41 dB 01 0001 = –40 dB 01 0010 = –39 dB ... 11 1001 = 0 dB ... 11 1111 = +6 dB

7.5.6.9 Register 0x08: Headphone Volume Control Register 2

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	LO_EXT_STAB	R/W	0	Extended Line-Out Stability 0 = Audio Channel does not support gain less than 0 dB for line-out load with large capacitive load (>100 pF). 1 = Audio Channel supports all gains for line-out load with max capacitive load of 470 pF.
6	MUTER	R/W	1	Right Headphone Mute 0 = Disable. 1 = Enable, output is muted.
5-0	RVOL	R/W	00 0000	Right Headphone Volume Control 00 xxxx = –42 dB 01 0000 = –41 dB 01 0001 = –40 dB 01 0010 = –39 dB ... 11 1001 = 0 dB ... 11 1111 = +6 dB

7.5.6.10 Register 0x09: Microphone Bias Control Register

The microphone bias register controls which microphone bias voltage and bias resistors are used, as well as the debounce time when a key press is detected.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	DIS_MIC_MUTE	R/W	0	Mic preamplifier Mute Control during button press Enable/Disable of Mic preamplifier Mute, when button (active/passive multi-button headset) is pressed. 0 – Mic Preamplifier is muted during button press. (Default) 1 – Mic Preamplifier is not muted during button press.
6	GAIN	R/W	0	Microphone Preamplifier Gain Select 0 = 12dB 1 = 24dB
5-3	MICR	R/W	000	Microphone Bias Resistor Select 000 = 2.2 kΩ 001 = 2.6 kΩ 010 = 3.0 kΩ 011 = Bypassed 1xx = Invalid
2	BIAS	R/W	0	Microphone Bias Voltage Select 0 = 2.0 V 1 = 2.6 V
1-0		R/W	11	Reserved. Always write 00. Needs to be initialized to 00 after device power up.

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7.5.6.11 Register 0x0a: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R	0000 0000	Reserved.

7.5.6.12 Register 0x0b: Revision ID Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-4	REV	R	0011	Revision ID
3-0		R		Reserved.

7.5.6.13 Register 0x0c: Reserved Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0001 1100	Reserved.

7.5.6.14 Registers 0x0d to 0x10: Reserved Registers

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved.

7.5.6.15 Register 0x11: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved. Always write 0 to this register.

7.5.6.16 Register 0x12: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved. Always write 0x01.

7.5.6.17 Register 0x13: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved. Always write 0x45.

7.5.6.18 Register 0x14: Reserved Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R	0000 0000	Reserved.

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7.5.6.19 Register 0x15: Keyscan Debounce Register

The keyscan debounce register controls the debounce time when a keypress is detected.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0	KEY_DEB	R/W	0000 0000	Keyscan Debounce Register Debounce time set from 0.25 ms to 63.75 ms in 0.25 ms increments. The programmed code plus 0.25 represents the debounce time directly, i.e. code 0x4F represents 20 ms of debounce.

7.5.6.20 Register 0x16: Keyscan Delay Register

The keyscan delay register sets the timeout that the mic button press is masked from the system. At the end of the delay time, the TPA6166A2 checks to see if a microphone is still present. If the mic is present, the system is alerted by setting the MCSW bit in the status register, flagging an interrupt if IMCSW is set. If the mic is not present after the delay time, then the system is flagged with an interrupt by setting MIC_IN, which signifies the mic has been removed and no keypress was made. This prevents accessory removal from being detected as a button press (due to RING2 and SLEEVE getting shorted during removal).

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0	KEY_DEL	R/W	0000 0000	Keyscan Delay Register Delay time set from 1 ms to 256 ms in 1-ms increments. The programmed code plus one multiplied by 1 ms represents the delay time, that is, code 0xC7 represents 200 ms of delay.

7.5.6.21 Register 0x17: Passive Multi Button Keyscan Data Register

The keyscan data register contains the data read from a keypress after the 10-bit ADC encodes the input voltage level. The read keypress could come from a single switch or a passive multi-button device.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	KEYDATA_DIV	R	0	Keyscan Data Divider Keyscan data should be inferred based on Equation 1. When the 10-bit ADC output is less than 128 (that is, 3 MSBs will be equal to 0), KEYDATA_DIV is set to 0 and 7 LSBs are reported in KEYDATA. When 10-bit ADC output is more than or equal to 128, KEYDATA_DIV is set to 1 and 9 LSBs of ADC Data divided by 4 (and rounded off) are reported in KEYDATA. This loses resolution for high value of Rswitch||Rmic, which is acceptable.
6-0	KEYDATA	R	000 0000	Keyscan Data B6-B0 are read only bits that contain the data read from a passive keypress that shorts the microphone to ground.

$$R_{SWITCH} \,||\, R_{MIC} = \left(\frac{R_{BIAS}}{\frac{3072}{KEYDATA} - 1} \right) \text{ (If KEYDATA_DIV} = 0\text{)}$$

$$R_{SWITCH} \,||\, R_{MIC} = \left(\frac{R_{BIAS}}{\frac{768}{KEYDATA} - 1} \right) \text{ (If KEYDATA_DIV} = 1\text{)} \quad (1)$$

7.5.6.22 Register 0x18: Jack Detect Test Hardware Settings

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	SHORT_Z	R/W	0	Maximum Impedance During Short Defines maximum impedance below which terminal is considered short. This information is used while detecting whether RING1 (terminal 2) is ground. 0 = 4 Ω 1 = 7 Ω
6	HP_LO_TH	R/W	0	Threshold Impedance to Distinguish Between Headphone and line-out Load Defines impedance below which load is Headphone and above is line-out. 0 = 700 Ω 1 = 1.5 kΩ
5-0		R	00 0000	Reserved.

7.5.6.23 Register 0x19:State Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	$\overline{\text{FORCE}}$	R/W	1	Load State Force Enable 0 = Force configuration of the load into the state programmed by B6-B0. 1 = State forcing disabled. B6-B0 reports the configuration reported by the jack configuration algorithm. When $\overline{\text{FORCE}}$ bit is changed from 0 to 1, the TPA6166A2 will not re-un accessory detection algorithm and configuration will continue to set to value already written in STATE bits. System will need to reset and then set $\overline{\text{SHDN}}$ to rerun accessory detection algorithm.
6-0	STATE	R/W	000 0000	Accessory State Bits B6-B0 represents accessory type Refer to Table 6 for the state table.

Table 6. State Lookup for Register 0x19, Bits 6-0

B6-B0		COMMENTS	TIP	RING1	RING2	SLEEVE	JACK_SENSE
HEX	BIN						
0x00	000 0000	Nothing	Float	Float	Float	Float	Short
0x01	000 0001	Stereo Headset (HP with mic)	HPL	HPR	Ground	Mic	Open
0x02	000 0010		HPL	HPR	Mic	Ground	Open
0x0A	000 1010	Mono Headset	HPL	Ground	Ground	Mic	Open
0x0B	000 1011		HPL	Ground	Mic	Ground	Open
0x0C	000 1100		HPL	HPL	Ground	Mic	Open
0x0D	000 1101		HPL	HPL	Mic	Ground	Open
0x0E	000 1110		HPL	Float	Ground	Mic	Open
0x0F	000 1111		HPL	Float	Mic	Ground	Open
0x10	001 0000	Stereo Headphone	HPL	HPR	Ground	Ground	Open
0x11	001 0001		HPL	Float	Ground	Ground	Open
0x12	001 0010		Float	HPR	Ground	Ground	Open
0x1A	001 1010	Stereo Line Out Audio Cable	LOL	LOR	Ground	Ground	Open
0x1B	001 1011		Cap / Float	LOR	Ground	Ground	Open
0x1C	001 1100		LOL	Cap / Float	Ground	Ground	Open
0x1F	001 1111	Unsupported	Cap / Float	Cap / Float	Ground	Ground	Open

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7.5.6.24 Register 0x1a: Jack Detect Test Hardware Settings

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	JACK_DEB	R/W	0	Debounce Time during Jack Insertion/Removal Detection Controls debounce time on comparators output during Jack Insertion / Removal Detection 0 = 3 ms (insertion and Sleep mode button press); 12 ms (removal detection) 1 = 20 ms (insertion and Sleep mode button press); 80 ms (removal detection)
6		R	0	Reserved.
5-4	AC_REPEAT	R/W	01	Pulse Test Repeat Control the number of times the pulse test is repeated. The more times the test is repeated, the more accurate the results will be. The final result is the average of all the tests. 00 = Test runs once 01 = Test runs 2 times 10 = Test runs 4 times 11 = Test runs 8 times
3-2	PULSE_WIDTH	R/W	01	Pulse Width Control 00 = 50 µs 01 = 25 µs 10 = 100 µs 11 = 200 µs
1-0	PULSE_AMP	R/W	01	Pulse Amplitude Control 00 = VDD / 36 (50 mV) 01 = VDD / 72 (25 mV) 10 = VDD / 18 (100 mV) 11 = VDD / 9 (200 mV)

7.5.6.25 Registers 0x1b: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R/W	0000 0000	Reserved.

7.5.6.26 Register 0x1c: Clock Control

Write 0x00 to this register at power-up. This ensures best performance from the TPA6166A2.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	CLOCK_CONTROL	R/W	0	Clock control for passive multi-button headset 0 = Clock is not turned on. 1 = Clock is turned on. Write this bit when passive multi-button functionality is required with headset inserted and device is not in Sleep/Shutdown mode. Along-with this bit, also write following sequence: Register: 0x66, Value: 0xF1 Register: 0x6F, Value: 0x01 Register: 0x66, Value: 0x00 When CLOCK_CONTROL is set to 0 (due to device going into Sleep/Shutdown mode), write following sequence: Register: 0x66, Value: 0xF1 Register: 0x6F, Value: 0x00 Register: 0x66, Value: 0x00
7-0		R/W	000 0001	Reserved. Always write 000 0000

7.5.6.27 Register 0x1d: Enable Register 1

The Enable registers contain all of the bits that control the separate functional blocks for the TPA6166A2. The system can either directly control these bits, or it can allow TPA6166A2 to automatically configure itself and report in the Enable register which blocks are enabled. When the AUTO bits (B1-B0) are set to 01 or 10, the Enable Registers are read only. The block enable bits do not need to be set to sense a jack removal. The jack removal circuitry is active as soon as an inserted jack is detected.

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BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	$\overline{\text{SHDN}}$	R/W	0	Full Device Shutdown Control $\overline{\text{SHDN}}$ turns TPA6166A2 on and off. When $\overline{\text{SHDN}}$ is low, the device is in low power mode and the jack insertion detect circuitry is active. Pull $\overline{\text{SHDN}}$ high to turn on the device and run the jack configuration detect algorithm. Typically $\overline{\text{SHDN}}$ will be held low until the system gets an interrupt from the indicating that a jack has been inserted. The system will then pull $\overline{\text{SHDN}}$ high. 0 = TPA6166A2 in lowest power shutdown mode. During this mode, accessory insertion/removal detection works only if jack switch not broken. If switch is broken, status will be reported as if accessory is inserted (even if accessory is not inserted or it is removed). SLEEP setting is ignored during this mode. 1 = TPA6166A2 is active. The jack configuration algorithm runs immediately after $\overline{\text{SHDN}}$ is pulled high.
6	SLEEP	R/W	0	Sleep Mode Enable Pull SLEEP high to enable the circuitry that looks for accessory insertion/removal and button press (for headset with Mic) when TPA6166A2 is shutdown. When a button press (for headset with Mic) is sensed, the MCSW bit in the status register is set, generating an interrupt if IMCSW is set. 0 = TPA6166A2 is in normal mode as long as $\overline{\text{SHDN}}$ is set. 1 = TPA6166A2 is in sleep mode. During this mode, accessory insertion and removal detection works even for broken Jack switch. For Headset with Mic cases, button press will generate an interrupt, which can be used for system wakeup. When device is programmed in Sleep mode (SLEEP=1), following sequence must to used to ensure best performance: Disable Auto mode and headphone amplifiers by programming register 0x1E, bits D1D0 to 00 and bits D7D6 to 00 Enable Auto mode by programming register 0x1E, bit D1D0 to 01
5		R	0	Reserved.
4	MIC_BIAS	R/W	0	Microphone Bias Enable/Status Set MIC_BIAS to enable the mic bias block. This bit is read only when AUTO (B1-B0) is set to 01 or 10. 0 = Microphone bias is disabled. 1 = Microphone bias is active.
3	MIC_AMP	R/W	0	Microphone Amplifier Enable/Status Set MIC_AMP to enable the mic amp. This bit is read only when AUTO (B1-B0) is set to 01 or 10. 0 = Microphone amp is disabled. 1 = Microphone amp is active.
2	KS	R	0	Keyscan Enable/Status KS enables the circuitry that decodes passive multi-button keypad or simple microphone switch. 0 = Keyscan ADC is disabled. 1 = Keyscan ADC is enabled. This bit is always **Read Only** (regardless of AUTO bits setting).
1		R	0	Reserved.
0		R	0	Reserved.

7.5.6.28 Register 0x1e: Enable Register 2

Set Register 0x1E, Bit 4 to 1 to ensure the best performance from the TPA6166A2.

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7	LFTEN	R/W	0	Left Headphone Enable/Status Set LFTEN to enable the left channel of the DirectDrive headphone amplifier. This bit is read only when AUTO (B1-B0) is set to 01 or 10. 0 = Headphone amp left channel disabled 1 = Headphone amp left channel enabled
6	RGHEN	R/W	0	Right Headphone Enable/Status Set RGHEN to enable the right channel of the DirectDrive headphone amplifier. This bit is read only when AUTO (B1-B0) is set to 01 or 10. 0 = Headphone amp right channel disabled 1 = Headphone amp right channel enabled

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BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
5	$\overline{\text{VSEN}}$	R/W	0	Volume Adjustment Slewing Volume changes are smoothed by stepping through intermediate steps. $\overline{\text{VSEN}}$ also ensures that the volume automatically ramps from the minimum setting to the programmed value at turnon and back to the minimum value at turnoff. 0 = Enabled 1 = Disabled
4		R/W	0	Reserved. Always write 1.
3	FAST	R/W	0	Jack Insertion Polling Speed A fast polling speed tests for a jack insertion 3 times per second while a slow polling speed tests for jack insertion every 2 seconds. This setting is valid only when mechanical TERMINAL5 switch is not operational. When mechanical TERMINAL5 switch is operational, detection is instantaneous (excluding debounce time and detection time). 0 = Slow polling mode, 2-sec delay between polls 1 = Fast polling mode, 333-ms delay between polls
2	THRH	R/W	0	Class-G Threshold Select THRH selects the threshold at which the power supplies switch from ±0.9 V to ±1.8 V. A higher threshold allows the TPA6166A2 output stage to be powered from ±0.9 V for a higher percentage of the audio waveform, decreasing power dissipation at the expense of dynamic distortion. 0 = Low Threshold 1 = High Threshold
1-0	AUTO	R/W	01	Automatic Mode Select Set AUTO to allow the TPA6166A2 to enable functional blocks depending on the load. In auto mode the system merely reads the status of registers 0x1D and 0x1E to find out what blocks are enabled. Setting AUTO makes bits register 0x1D and 0x01E read only. Clear AUTO to give the system control of what functional blocks are active. The system would need to allow the jack configuration detect algorithm to complete before enabling functional blocks. 00 = System controls which functional blocks are on. Registers 0x1D and 0x1E are R/W. $\overline{\text{SHDN}}$ and SLEEP settings are ignored. 01 = TPA6166A2 enables functional blocks automatically depending on the results of the jack configuration detect algorithm provided that SLEEP is set to 0 ($\overline{\text{SHDN}}$ must be set to 1, otherwise device will go into low power state). 10 = TPA6166A2 enables functional blocks automatically depending on the results of the jack configuration detect algorithm regardless of settings of $\overline{\text{SHDN}}$ and SLEEP. 11 = Invalid.

7.5.6.29 Register 0x1F: Reserved

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0		R	0000 0000	Reserved.

7.5.6.30 Register 0x66: Clock Flex Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0	CLOCK_FLEX	R/W	0000 0000	Reserved. Write 0xF1 to use Register 0x6F, then set back to zero.

7.5.6.31 Register 0x6F: Clock Set Register

BIT	NAME	READ / WRITE	DEFAULT	DESCRIPTION
7-0	CLOCK_SET	R/W	0000 0000	Write 0x01 when passive button detection is needed in Active mode. (accessory is inserted, and device is not in Sleep/Shutdown mode). Reset to 0x00 when the device is going to sleep to save power.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section describes a typical application of TPA6166A2 with a standard audio jack with battery voltage level supply. The circuit detects what kind of device is plugged into the jack and delivers excellent audio quality.

8.2 Typical Application

Figure 32 shows a typical application circuit for the TPA6166A2 with a 5-terminal audio jack. *Accessory Detection* describes all the accessory jack configurations the TPA6166A2 automatically detects.

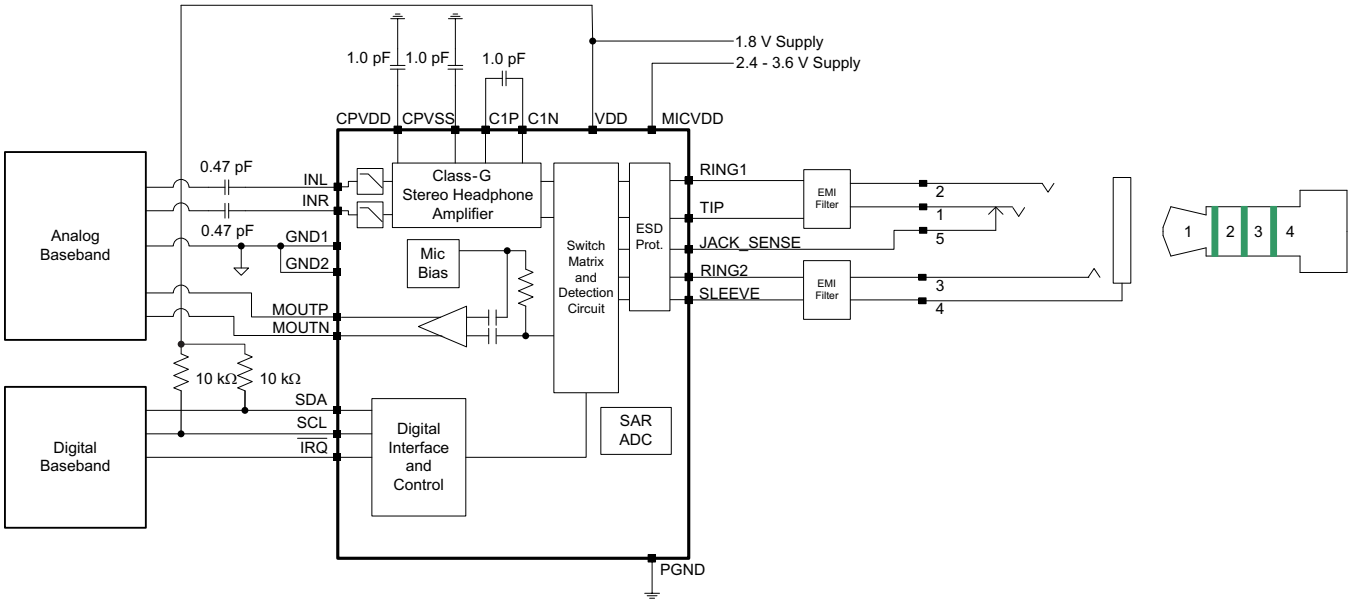


Figure 32. Typical Application Circuit

8.2.1 Design Requirements

Table 7. Design Parameters

DESIGN PARAMETERS	VALUE
VDD Supply voltage	1.7 V to 1.9 V
MICVDD Microphone supply voltage	2.4 V to 3.6 V

8.2.2 Detailed Design Procedure

8.2.2.1 Charge Pump Capacitors

The CPVDD and CPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low ESR (example: < 20 mΩ at 1.3 MHz) ceramic capacitors to maximize charge pump efficiency. X5R-type capacitors or better are required for best performance. Typical values are 1 µF to 2.2 µF for the charge pump capacitors.

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Charge pump capacitors should be able to handle up to 2 V during normal operation. During IEC ESD strike on jack terminals, voltage on these capacitors can go as high as 12 V for 30 to 40 ns. Capacitors rated for 6.3 V or higher can typically handle such voltages for short durations without getting damaged.

8.2.2.2 Audio Input ac Coupling Capacitors

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6166A2 turnon pop to an inaudible level. The input capacitors are in series with TPA6166A2 internal input resistors, creating a high-pass filter. Equation 2 calculates the high-pass filter corner frequency. The TPA6166A2 typical input impedance, R_{IN}, is 20 kΩ.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \tag{2}$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \tag{3}$$

Example: Select input coupling capacitor values to achieve a 20 Hz high-pass corner frequency. Equation 3 shows the input coupling capacitors must be at least 0.4 µF. Choose a 0.47-µF standard value capacitor for each TPA6166A2 input. Use X5R-type or better capacitors for best performance.

8.2.2.3 Suggested Output EMI Filter

To prevent noise getting radiated from headphone, EMI filters are often included on terminals connected to the Jack. Figure 33 illustrates typical connection diagram of EMI filter implemented using 'pi' configuration.

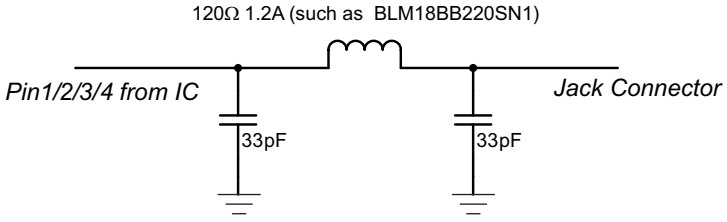


Figure 33. EMI Filter

High-frequency impedance of RF beads in range of 100 MHz can impact IEC ESD performance on TPA6166A2 jack outputs (LOUT, PIN2_ROUT, PIN3, and PIN4). Higher impedances change the waveform during IEC strike to make it wider, which subjects internal circuit to stress for longer duration. Use RF beads which are equal to or less than 22-Ω impedance at 100 MHz.

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8.2.3 Application Curve

The high quality and low distortion of the TPA6166A2 mic preamplifier is shown in Figure 34.

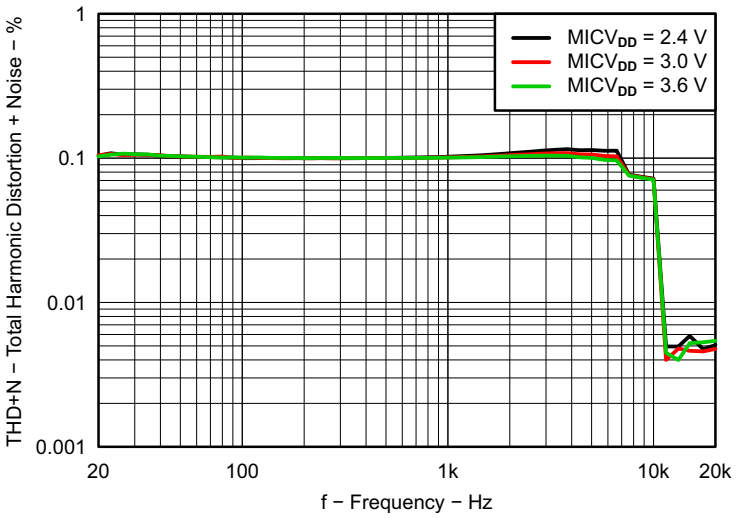


Figure 34. Mic Preamplifier Total Harmonic Distortion + Noise vs Frequency

9 Power Supply Recommendations

The TPA6166A2 has two power-supply domains, VDD and MICVDD. The TPA6166A2 allows VDD and MICVDD supplies to come up in any order. The Internal circuit of the TPA6166A2 has diodes between VDD and MICVDD supply domain, which are reversed bias during normal operation. If MICVDD voltage is less than VDD, these diodes can get forward bias and drive MICVDD. If the application requires that the MICVDD terminal not be driven in such a condition, an external switch on MICVDD can be used. I^2C read/write and the accessory-detection algorithm is disabled until both VDD and MICVDD supplies are up. During operation, if the MICVDD supply goes below its normal operating voltage, the control-register contents are still preserved. Once the supply comes up again, the accessory detection algorithm runs again to ensure the correct state. If the MICVDD supply is not powered up, the SDA line can be clamped by TPA6166A2. This is due to the internal ESD protection structure on SDA being biased based on MICVDD.

9.1 Decoupling Capacitors

The TPA6166A2 requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use quality low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 1-µF capacitor within 5 mm of the VDD and MICVDD terminal. Reducing the distance between the decoupling capacitor and VDD/MICVDD minimizes parasitic inductance and resistance, improving TPA6166A2 supply rejection performance. Use 0402 or smaller size capacitors if possible. Ensure that the ground connection of each of the capacitors has a minimum-length return path to the device. Failure to properly decouple the TPA6166A2 may degrade audio or EMC performance.

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10 Layout

10.1 Layout Guidelines

The ground terminal must be connected to the ground plane as close as possible to the TPA6166A2, to minimize any inductance in the path. Place the decoupling capacitor as close as possible to the supply terminal, minimizing trace length (and thus the inductance) on the decoupling capacitor connection to ground.

Because INL and INR are single-ended inputs, take care to minimize noise on INL and INR with respect to TPA6166A2 ground. This is best achieved by using then same ground plane for the signal source and the TPA6166A2 with a minimum inductance between them.

The accessory-detection algorithm requires trace capacitance to be minimized between TPA6166A2 and the jack. Depending upon headphone impedance, trace resistance between TPA6166A2 and the jack impacts power delivered to load. If trace resistance is much smaller than headphone impedance, power loss is given by Equation 4. Trace resistance should be minimized based on acceptable power loss.

$$\text{Power Loss} = \frac{\text{Trace Resistance}}{\text{Headphone Resistance}} \tag{4}$$

To minimize crosstalk, trace resistance on RING2 (terminal 3) and SLEEVE (terminal 4) should be minimized. This can be achieved by placing TPA6166A2 close to the jack. For cases where trace resistance is not small, crosstalk is given by Equation 5. In such scenarios, best balance can be achieved by increasing trace width of SLEEVE. RING2 has no constraint on maximum capacitance, and its trace width can be maximized to achieve desired crosstalk performance.

$$\text{Crosstalk (dB)} = 20\log_{10}\left(\frac{\text{Trace Resistance}}{\text{Headphone Resistance} + \text{Trace Resistance}}\right) \tag{5}$$

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10.2 Layout Example

10.2.1 Pad Sizing

When determining the pad size for the WCSP terminals, use nonsolder mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 35 and Table 8 show the appropriate diameters for a WCSP layout.

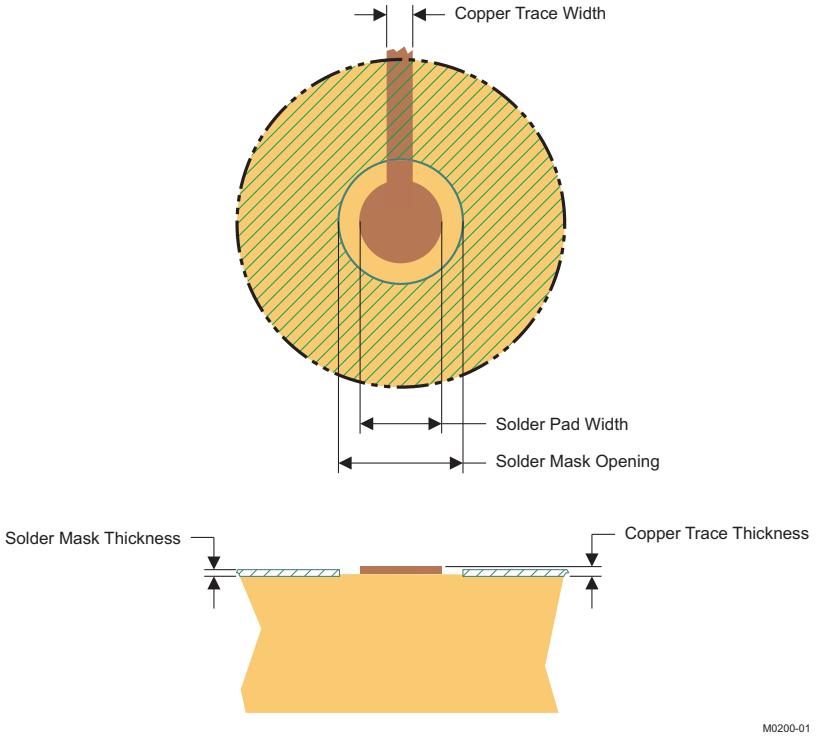


Figure 35. Land Pattern Dimensions

Table 8. Land Pattern Dimensions (1)(2)(3)(4)

SOLDER PAD DEFINITION	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) (7) OPENING	STENCIL THICKNESS
Nonsolder mask defined (NSMD)	230 µm	310 µm	1 oz. max. (32 µm)	275 µm × 275 µm sq. (rounded corners)	100 µm thick

(1) Circuit traces from NSMD-defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device standoff and impact reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating range of the intended application.
(3) Recommended solder paste is type 3 or type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0.5 mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) Best solder stencil performance is achieved using laser-cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
(7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

Table 9. Package Dimensions

D	E
Max. = 2470 µm	Max. = 2470 µm
Typ. = 2440 µm	Typ. = 2440 µm
Min. = 2410 µm	Min. = 2410 µm

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11 Device and Documentation Support

11.1 Development Support

See *TPA6166A2EVM User's Guide*, SLOU381.

11.2 Trademarks

DirectPath is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6166A2YFFR	ACTIVE	DSBGA	YFF	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SMB	Samples
TPA6166A2YFFT	ACTIVE	DSBGA	YFF	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	SMB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

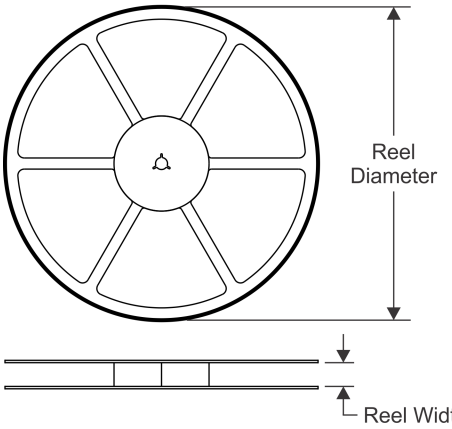
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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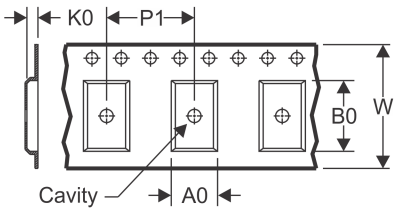
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

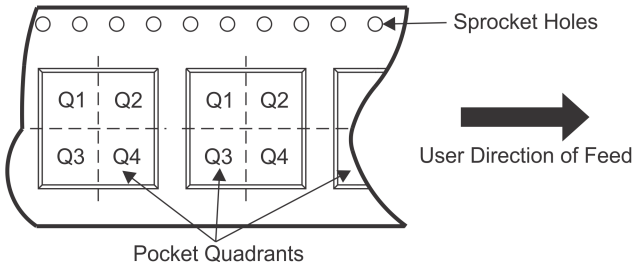


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

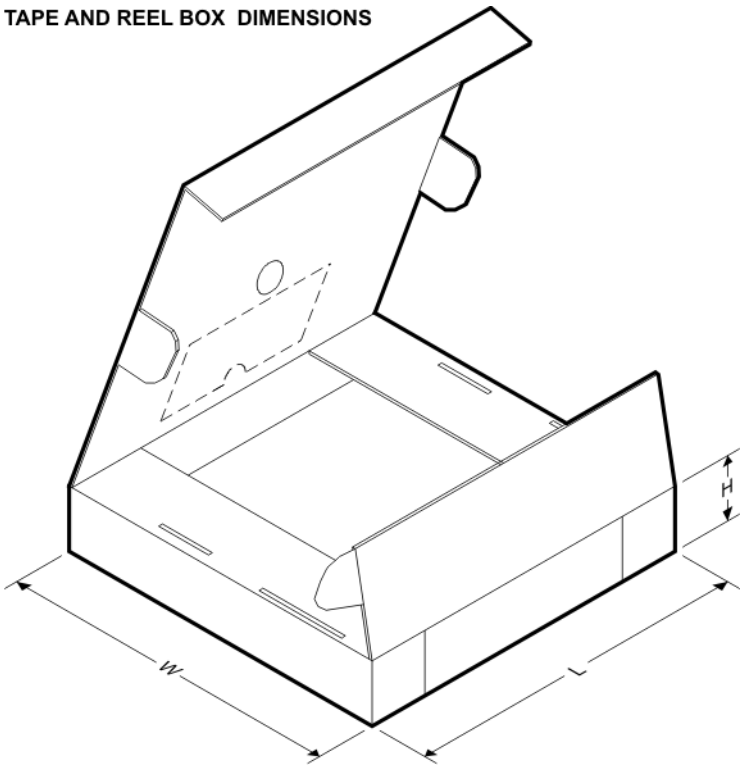
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6166A2YFFR	DSBGA	YFF	25	3000	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1
TPA6166A2YFFT	DSBGA	YFF	25	250	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1

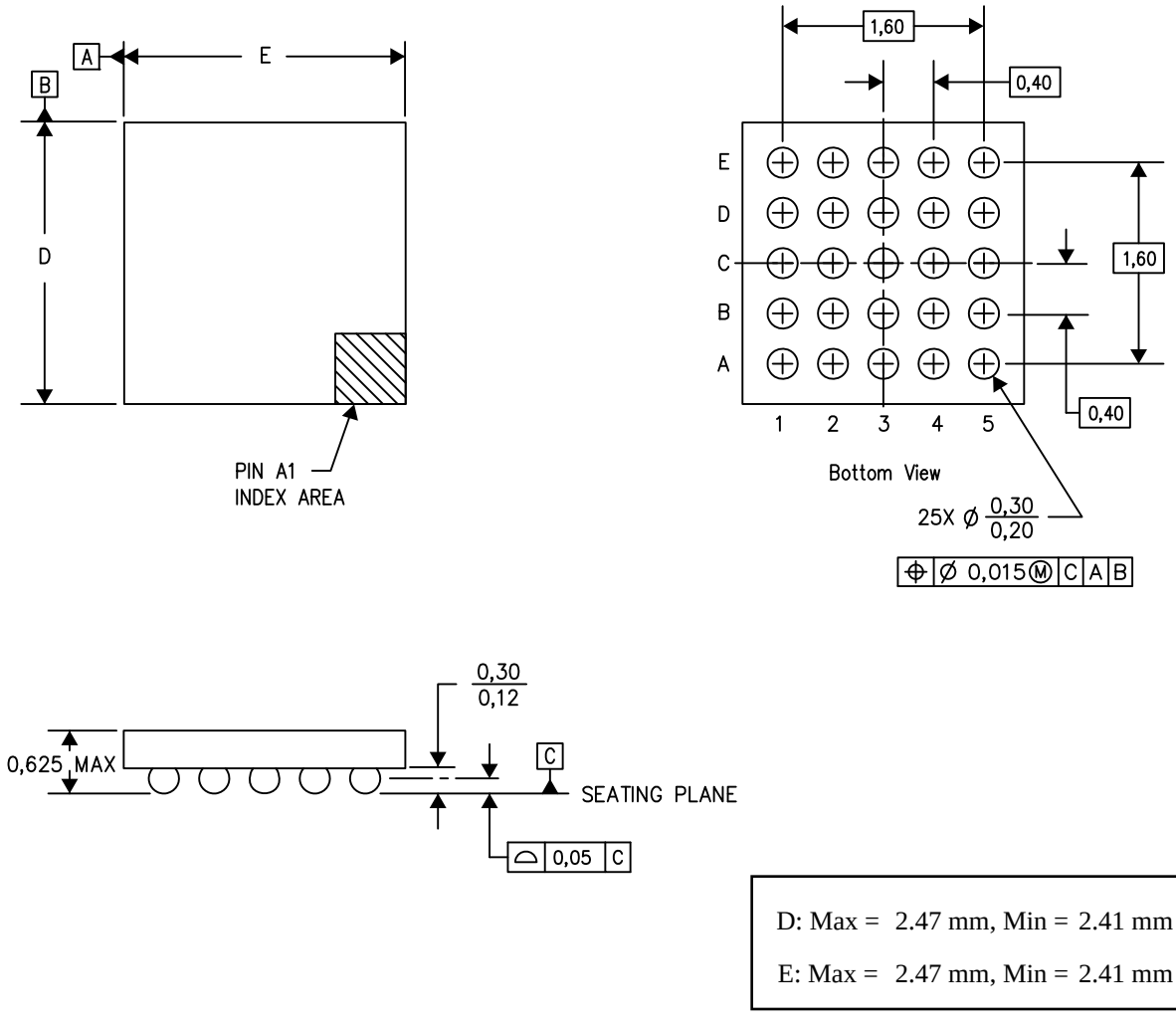
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6166A2YFFR	DSBGA	YFF	25	3000	182.0	182.0	20.0
TPA6166A2YFFT	DSBGA	YFF	25	250	182.0	182.0	20.0

YFF (S–XBGA–N25) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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