TMUXHS4212 Two-Channel Differential 2:1 Mux / 1:2 Demux

1 Features

- Provides bidirectional 2:1 MUX / 1:2 DEMUX
- Supports USB 3.2 up to 10 Gbps (Gen 2.0) and PCI Express up to 16 Gbps (Gen 4.0)
- Also supports SATA, SAS, MIPI DSI/CSI, FPD-Link III, LVDS, SFI and Ethernet interfaces
- –3-dB differential BW of 13 GHz
- Dynamic characteristics
  - Insertion loss = –1.3 / -1.8 dB at 5 / 8 GHz
  - Return loss = –13 / -12 dB at 5 / 8 GHz
  - Off isolation = –22 / -20 dB at 5 / 8 GHz
- Low intra/inter-pair skew of 8 / 20 ps max
- Adaptive common mode voltage tracking
- Supports common mode voltage up to 0 to 1.8 V
- Single supply voltage V_{CC} of 3.3 V
- Ultra low active (180 μA) and standby power consumption (<2 μA)
- Industrial temperature option with –40° to 105°C
- Available in 2.5 mm x 4.5 mm QFN package

2 Applications

- PC and notebooks
- Smartphone, Tablets, and TV
- Gaming and Home theater & entertainment
- Data center and enterprise computing
- Medical applications
- Test and measurements
- Factory automation and control
- Aerospace and defense
- Electronic point of sale (EPOS)
- Wireless infrastructure

3 Description

The TMUXHS4212 is a high-speed bidirectional passive switch in mux or demux configurations. It is suited for many applications including USB Type-C® and PCI Express. The TMUXHS4212 is a generic analog differential passive mux or demux that works for many high-speed differential interfaces with data rates up to 16 Gbps. The device can be used for higher data rates where electrical channel has signal integrity margins. The TMUXHS4212 supports differential signaling with common mode voltage range (CMV) of 0 to 1.8 V and with differential amplitude up to 1800 mVpp. Adaptive CMV tracking ensures the channel through the device remains unchanged for the entire common mode voltage range.

The dynamic characteristics of the TMUXHS4212 allows high-speed switching, minimum attenuation to the signal eye diagram, and with very little added jitter. The device's silicon design is optimized for excellent frequency response at higher frequency spectrum of the signals. Its silicon signal traces and switch network are matched for best intra-pair skew performance.

The TMUXHS4212 has an extended industrial temperature range that suits many rugged applications including industrial and high reliability use cases.

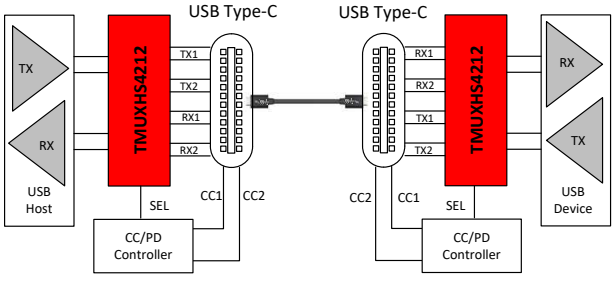
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUXHS4212	VQFN (20)	2.50 mm × 4.50 mm × 0.5-mm pitch
TMUXHS4212I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

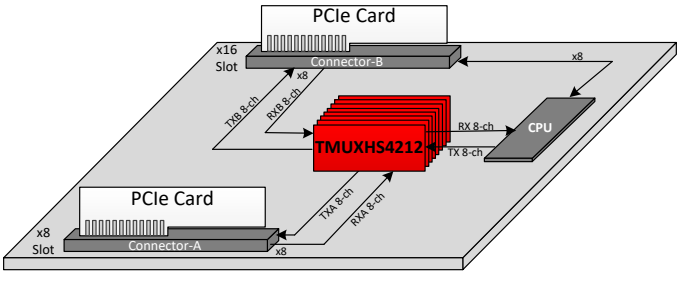
ADVANCE INFORMATION

Application Use Cases



USB-C DFP Port with USB 3.2

USB-C UFP Port with USB 3.2



PCIe 3.0/4.0 Lane Switching

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 High-Speed Performance Parameters ... 5
6.7 Switching Characteristics ... 6
6.8 Typical Characteristics ... 7
7 Parameter Measurement Information ... 7
8 Detailed Description ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 10
9 Application and Implementation ... 11
9.1 Application Information ... 11
9.2 Typical Applications ... 13
9.3 Systems Examples ... 17
10 Power Supply Recommendations ... 19
11 Layout ... 19
11.1 Layout Guidelines ... 19
11.2 Layout Example ... 19
12 Device and Documentation Support ... 20
12.1 Receiving Notification of Documentation Updates 20
12.2 Support Resources ... 20
12.3 Trademarks ... 20
12.4 Electrostatic Discharge Caution ... 20
12.5 Glossary ... 20
13 Mechanical, Packaging, and Orderable Information ... 20

ADVANCE INFORMATION

4 Revision History

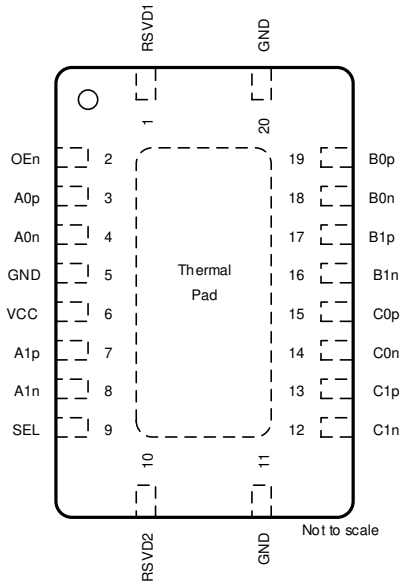
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2020	*	Initial release

Copyright © 2020, Texas Instruments Incorporated

5 Pin Configuration and Functions

RKS Package
20-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0n	4	I/O	Port A, channel 0, high-speed negative signal
A0p	3	I/O	Port A, channel 0, high-speed positive signal
A1n	8	I/O	Port A, channel 1, high-speed negative signal
A1p	7	I/O	Port A, channel 1, high-speed positive signal
B0n	18	I/O	Port B, channel 0, high-speed negative signal (connector side)
B0p	19	I/O	Port B, channel 0, high-speed positive signal (connector side)
B1n	16	I/O	Port B, channel 1, high-speed negative signal
B1p	17	I/O	Port B, channel 1, high-speed positive signal
C0n	14	I/O	Port C, channel 0, high-speed negative signal
C0p	15	I/O	Port C, channel 0, high-speed positive signal
C1n	12	I/O	Port C, channel 1, high-speed negative signal
C1p	13	I/O	Port C, channel 1, high-speed positive signal
GND	5, 11, 20	G	Ground
OEn	2	I	Active-low chip enable. The pin can be connected to GND if always on functional behaviour is desired. L: Normal operation, H: Shutdown. If always ON behavior of the device is desired the pin can be permanently connected to GND.
RSVD1	1	NA	Reserved pins. Connect both pins to V_{CC} or leave both of them open (no connect).
RSVD2	10	NA	
SEL	9	I	Port select pin. L: Port A to Port B, H: Port A to Port C
V_{CC}	6	P	3.3 V power

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC-ABSMAX}$	Supply voltage		–0.5	4	V
$V_{HS-ABSMAX}$	Voltage	Differential I/O	–0.5	2.4	V
$V_{CTR-ABSMAX}$	Voltage	Control pins	–0.5	V_{CC}+0.4	V
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3.0	3.3	3.6	V
$V_{CC-RAMP}$	Supply voltage ramp time		0.1		100	ms
V_{IH}	Input high voltage	SEL, OEn pins	$0.75V_{CC}$			V
V_{IL}	Input low voltage	SEL, OEn pins			$0.25V_{CC}$	V
V_{DIFF}	High-speed signal pins differential voltage		0		1.8	V_{pp}
V_{CM}	High speed signal pins common mode voltage		0		1.8	V
T_A	Operating free-air/ambient temperature	TMUXHS4212	0		70	°C
		TMUXHS4212I	-40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUXHS4212 RKS (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	53.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.1	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package ThermalMetrics application report.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	OEn = 0; 0 V ≤ V_{CM} ≤ 1.8		180	250	µA
I_{STDN}	Device shutdown current	OEn = V_{CC}		2	5	µA
C_{ON}	Output ON capacitance to GND	OEn = 0		0.4		pF
C_{OFF}	Output OFF capacitance to GND	OEn = V_{CC}		0.6		pF
R_{ON}	Output ON resistance	0 V ≤ V_{CM} ≤ 1.8 V; I_O = –8 mA		5	9	Ω
ΔR_{ON}	On-resistance match between pairs for the same channel at same V_{CM}, V_{CC} and T_A				0.5	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX) – R_{ON}(MIN) over V_{CM} range for the same channel at same V_{CC} and T_A				0.75	Ω
$I_{IH,CTRL}$	Input high current, control pins (SEL, OEn)	V_{IN} = 3.6 V			2	µA
$I_{IL,CTRL}$	Input low current, control pins (SEL, OEn)	V_{IN} = 0 V			1	µA
$R_{CM,HS}$	Common mode resistance to ground on Ax pins	Each pin to GND		1.0	1.6	MΩ
$I_{IH,HS,SEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8 V for selected port, A and B with SEL = 0, and A and C with SEL = V_{CC}			5	µA
$I_{IH,HS,NSEL}$	Input high current, high-speed pins [Ax/Bx/Cx][p/n]	V_{IN} = 1.8 V for non-selected port, C with SEL = 0, and B with SEL = V_{CC} (1)			150	µA
$I_{HIZ,HS}$	Leakage current through turned off switch between Ax[p/n] and [B/C]x[p/n]	OEn = VCC; Ax[p/n] = 1.8 V, [B/C]x[p/n] = 0 V and Ax[p/n] = 0 V, [B/C]x[p/n] = 1.8 V			2	µA
$R_{A,p2n}$	DC Impedance between p and n for Ax pins	OEn = 0 and VCC		20		KΩ

(1) There is a 20-kΩ pull-down in non-selected port.

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	f = 10 MHz		-0.4		dB
		f = 2.5 GHz		-0.8		
		f = 4 GHz		-1.1		
		f = 5 GHz		-1.3		
		f = 8 GHz		-1.8		
		f = 10 GHz		-2.1		
BW	–3-dB bandwidth			13		GHz
R_L	Differential return loss	f = 10 MHz		-28		dB
		f = 2.5 GHz		-16		
		f = 4 GHz		-13		
		f = 5 GHz		-13		
		f = 8 GHz		-12		
		f = 10 GHz		-12		
O_{IRR}	Differential OFF isolation	f = 10 MHz		-60		dB
		f = 2.5 GHz		-27		
		f = 4 GHz		-23		
		f = 5 GHz		-22		
		f = 8 GHz		-20		
		f = 10 GHz		-18		
X_{TALK}	Differential crosstalk	f = 10 MHz		-65		dB
		f = 2.5 GHz		-40		
		f = 4 GHz		-35		
		f = 5 GHz		-32		
		f = 8 GHz		-29		
		f = 10 GHz		-26		

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

6.7 Switching Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	f = 1 Ghz			70	ps
t_{SW_ON}	Switching time SEL-to-Switch ON	Biased from Bx/Cx side with CMV difference is <100mV, Bx/Cx pins at 90% of final value,		300	500	ns
t_{SW_OFF}	Switching time SEL-to-Switch OFF	Biased from Bx/Cx side with CMV difference is <100mV, Bx/Cx pins at 90% of final value,		300	500	ns
t_{SK_INTRA}	Intra-pair output skew between P and N pins for same channel	f = 1 Ghz		2	8	ps
t_{SK_INTER}	Inter-pair output skew between channels	f = 1 Ghz		5	20	ps

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

6.8 Typical Characteristics

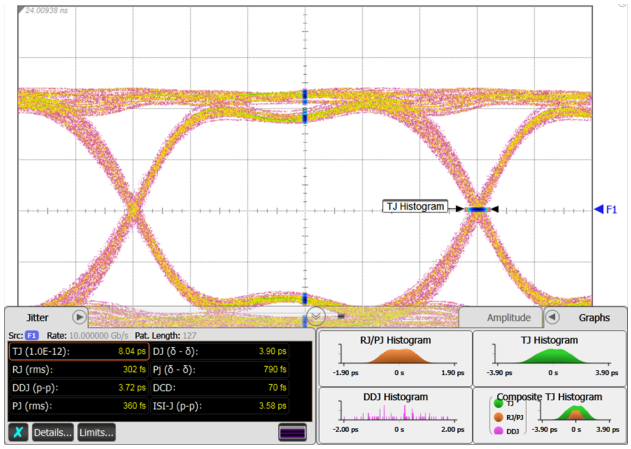


Figure 1. Jitter Decomposition of 10Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

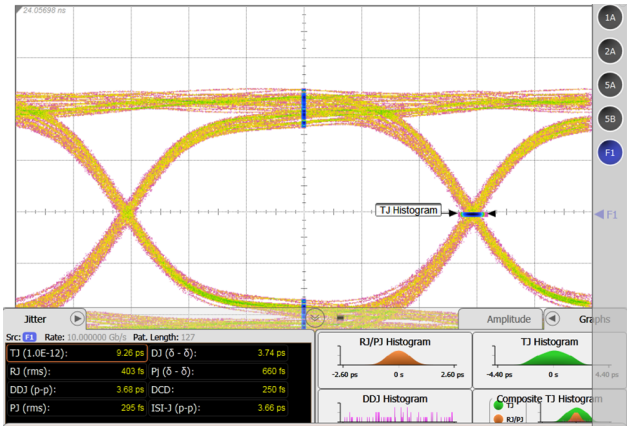


Figure 2. Jitter Decomposition of 10Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

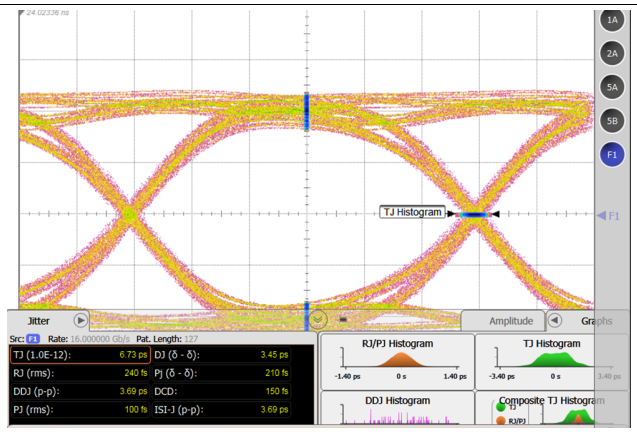


Figure 3. Jitter Decomposition of 16Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

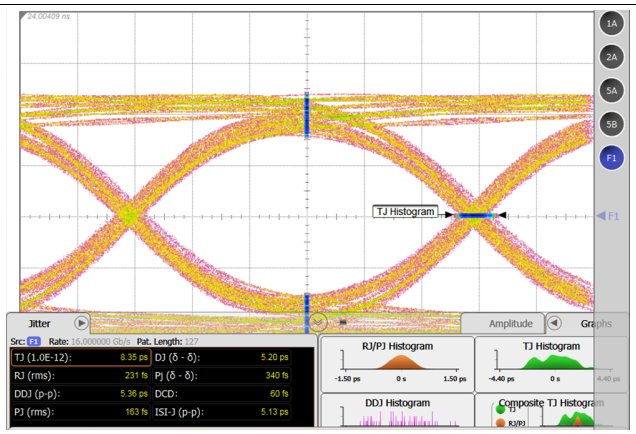


Figure 4. Jitter Decomposition of 16Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

ADVANCE INFORMATION

7 Parameter Measurement Information

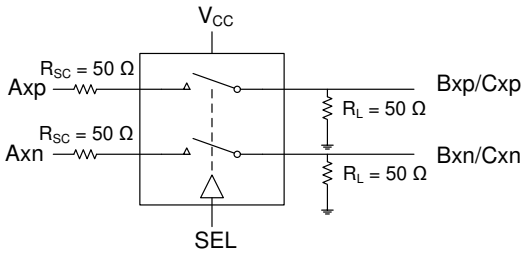


Figure 5. Test Setup

Parameter Measurement Information (continued)

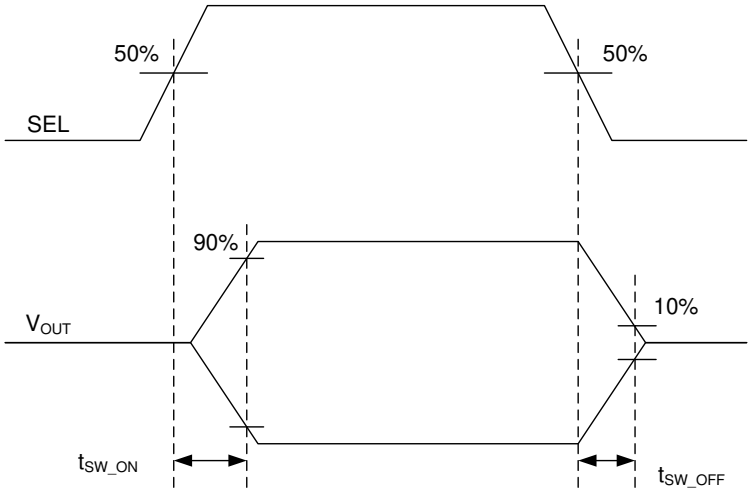


Figure 6. Switch On and Off Timing Diagram

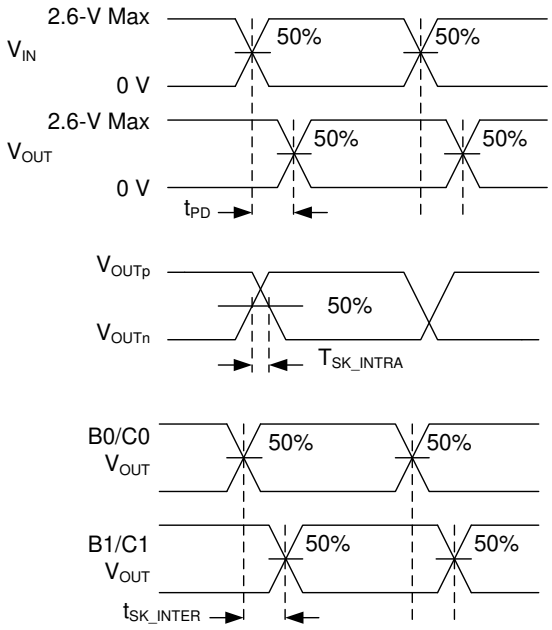


Figure 7. Timing Diagrams and Test Setup

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

8 Detailed Description

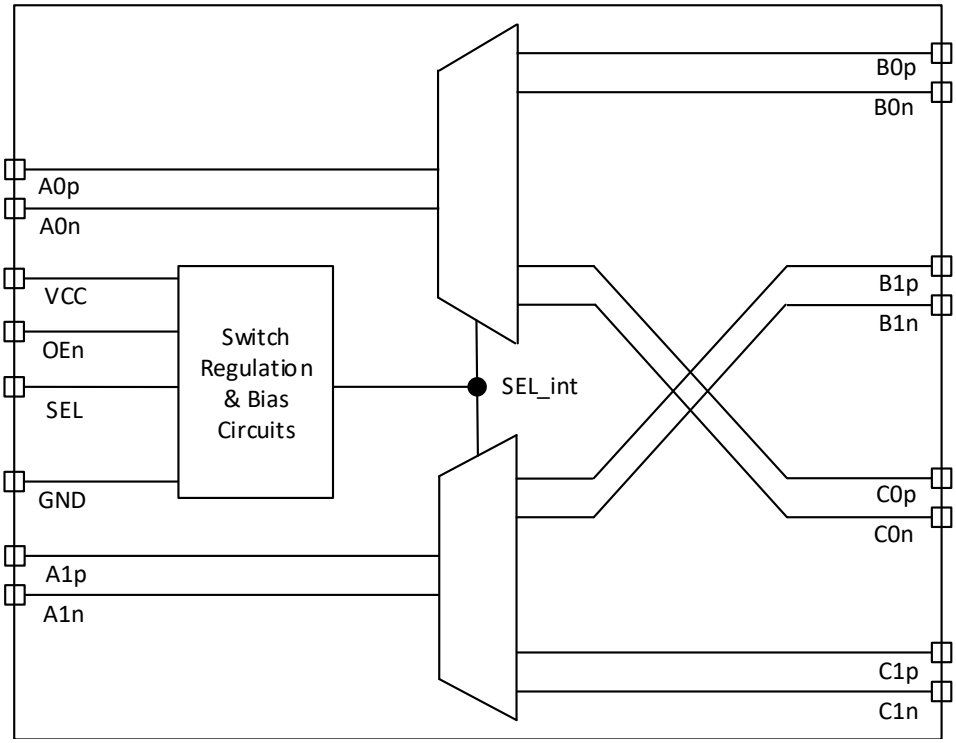
8.1 Overview

The TMUXHS4212 is a generic analog differential passive mux/demux that can work for any high-speed interface applications requiring a common mode voltage (CMV) range of 0 to 1.8 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive input voltage tracking that ensures the channel remains unchanged for the entire common mode voltage range. Two channels of the device can be used for electrical signals that have different CMV between them. Two channels can also be used such a way that the device switches two different interface signals with different data and electrical characteristics.

Excellent dynamic characteristics of the device allow high speed switching with minimum attenuation to the signal eye diagram with very little added jitter. While the device is recommended for the interfaces up to 16 Gbps, actual data rate where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained the device can potentially be used for higher data rates.

The TMUXHS4212 is only recommended for differential signaling. However certain low voltage single ended signaling such as Mipi DPHY LP signaling can pass through the device. It is recommended to analyze the data line biasing of the device for such single ended use cases.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Output Enable and Power Savings

The TMUXHS4212 has two power modes, active/normal operating mode and standby/shutdown mode. During standby mode, the device consumes very-little current to achieve ultra low power in systems where power saving is critical. To enter standby mode, the OEn control pin is pulled high through a resistor and must remain high. For active/normal operation, the OEn control pin should be pulled low to GND or dynamically controlled to switch between H or L.

The TMUXHS4212 consumes 180 μA of power when operational and has a shutdown mode exercisable by the OEn pin resulting < 2 μA.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

Feature Description (continued)

8.3.2 Data Line Biasing

The TMUXHS4212 has a weak pull-down of 1MΩ from A[0/1][p/n] pins to GND. While these resistors biases the device data channels to common mode voltage (CMV) of 0 V with very weak strength, it is recommended that the device is biased by a stronger impedance from either side of the device to a valid value in the range of 0 - 1.8 V. To avoid double biasing appropriate AC coupling capacitors should be ensured on either side of the device.

In certain use cases if both side of the TMUXHS4212 is ac coupled, it is recommended that appropriate CMV biasing is used for the device. 10 kΩ to GND or any other bias voltage in the range of 0 - 1.8 V for each A[0/1][p/n] pin will suffice for most use cases.

The high-speed data ports incorporate 20 kΩ pull-down resistors that are switched in when a port is not selected and switched out when the port is selected. For example when SEL = L, the C[0/1][p/n] pins have 20 kΩ resistors to GND. The feature ensures that unselected port is always biased to a known voltage for long term reliability of the device and the electrical channel.

The positive and negative terminals of data pins A[0/1] have a weak (20 kΩ) differential resistor for device switch regulation operation. This does not impact signal integrity or functionality of high speed differential signaling that typically has much stronger differential impedance (such as 100 Ω).

8.4 Device Functional Modes

Table 1. Port Select Control Logic(1)

PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

(1) The TMUXHS4212 can tolerate polarity inversions for all differential signals on Ports A, B, and C. In such flexible implementation one must ensure that the same polarity is maintained on Port A versus Ports B/C.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUXHS4212 is a generic 2-channel high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The TMUXHS4212 supports many high-speed data protocols provided the signals' differential amplitude is within <1800 mVpp and a common mode voltage is <1.8 V. The TMUXHS4212 can be used for many high speed interfaces including:

- Universal Serial Bus (USB) 3.2 Gen 1.0, 2.0
- USB Type-C
- Peripheral Component Interconnect Express (PCIe) Gen 1.0, 2.0, 3.0, 4.0
- Serial ATA (SATA/eSATA)
- Serial Attached SCSI (SAS)
- Display Port (DP) 1.4, 2.0
- Thunderbolt (TBT) 3.0
- Mipi Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- Low Voltage Differential Signalling (LVDS)
- Serdes Framer Interface (SFI)
- Ethenet Interfaces

The device's mux/demux selection pin SEL can easily be controlled by an available GPIO pin of a controller or hard tie to voltage level H or L as an application requires.

The TMUXHS4212 with adaptive voltage tracking technology can support applications where the common mode is different between the RX and TX pair. The switch paths of the TMUXHS4212 have internal weak pull-down resistors of 1 MΩ on the A port pins. While these resistors biases the device data channels to common mode voltage (CMV) of 0 V with a weak strength, it is recommended that the device is biased from either side of the device to a valid value in the range of 0 - 1.8 V. It is expected that the system/host controller and Device/End point common mode bias impedances are much stronger (smaller) than the TMUXHS4212 internal pull-down resistors; therefore, they are not impacted.

Many interfaces require AC coupling between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option to provide AC coupling. Avoid the 0603, 0805 size capacitors and C-packs. When placing AC coupling capacitors, symmetric placement is best. The capacitor value must be chosen according to the specific interface the device is being used. The value of the capacitor should match for the positive and negative signal pair. For many interfaces such as USB 3.2 and PCIe, the designer should place them along the TX pairs on the system board, which are usually routed on the top layer of the board. Depending upon the application and interface specifications, use the appropriate value for AC coupling capacitors.

The AC coupling capacitors have several placement options. Typical use cases warrant that the capacitors are placed on one side of the TMUXHS4212. In certain use cases, if both side of the TMUXHS4212 is ac coupled, it is recommended that appropriate CMV biasing is used for the device. 10 kΩ to GND or any other bias voltage in the range of 0 - 1.8 V for each A[0/1][p/n] pin suffice for most use cases.Figure 8 shows a few placement options. Some interfaces such as USB SS and PCIe recommends AC coupling capacitors on the TX signals before it goes to a connector. Option (a) features TX AC coupling capacitors on the connector side of the TMUXHS4212. Option (b) illustrates the capacitors on the host of the TMUXHS4212. Option (c) showcases where the TMUXHS4212 is ac coupled on both sides. Range for V_{BIAS} is 0 to 1.8 V.

ADVANCE INFORMATION

Application Information (continued)

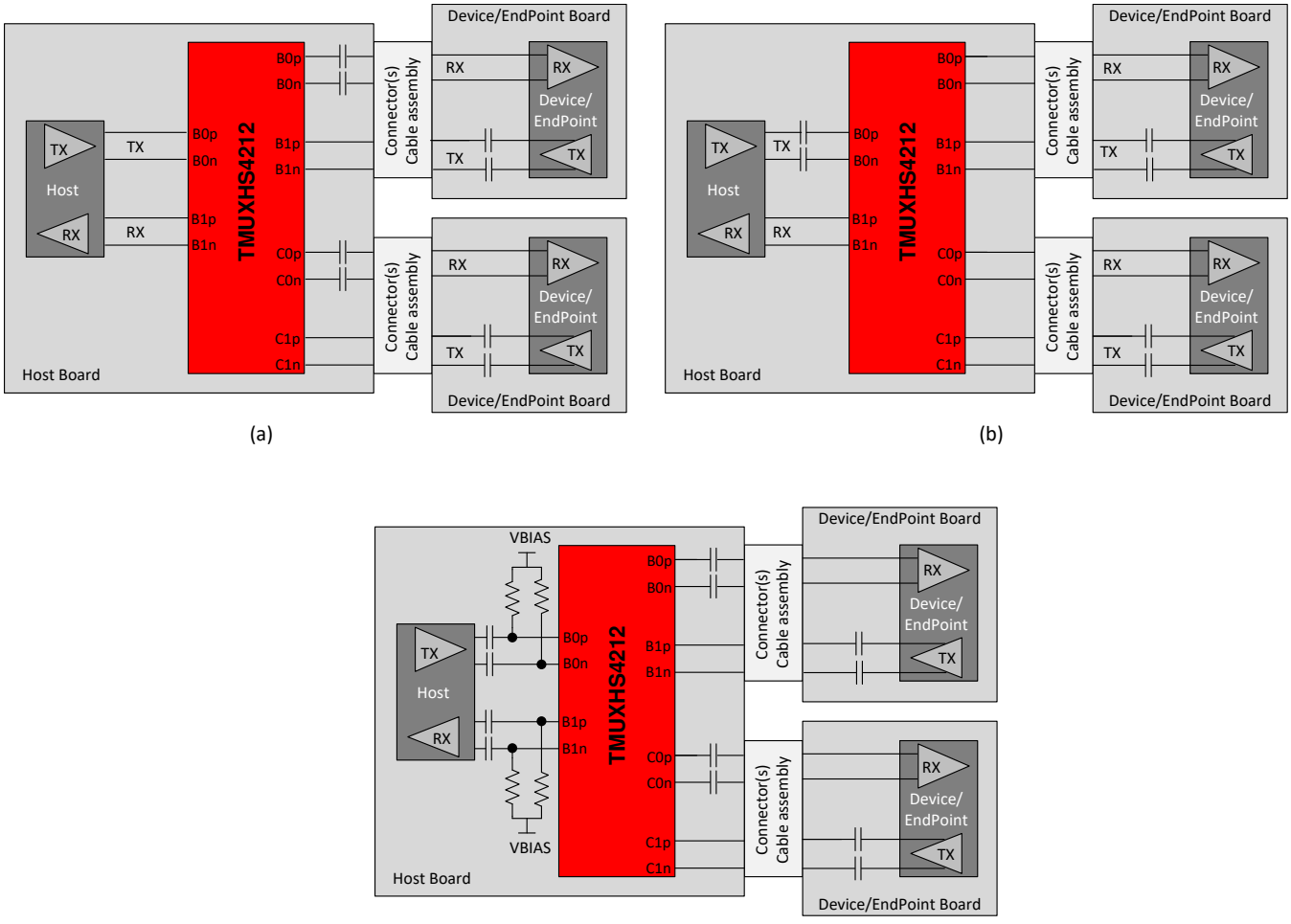


Figure 8. AC Coupling Capacitors Placement Options between Host and Device / Endpoint through TMUXHS4212

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

9.2 Typical Applications

9.2.1 USB3.2 implementation for USB Type-C

The TMUXHS4212 can be used in USB Type-C implementation to mux USB 3.2 superspeed signals (TX1, RX1 pairs versus TX2, RX2 pairs) to accommodate plug flips. In typical use cases, the mux selection is done by a USB Type-C Channel Configuration (CC) or Power Delivery (PD) controller. The device can used on a USB Type-C DFP, UFP or DRP port. The two USB Type-C connector applications show both a host and device side. The cable between the two connectors swivels the pairs to properly route the signals to the correct pin. The other applications are more generic because different connectors can be used.

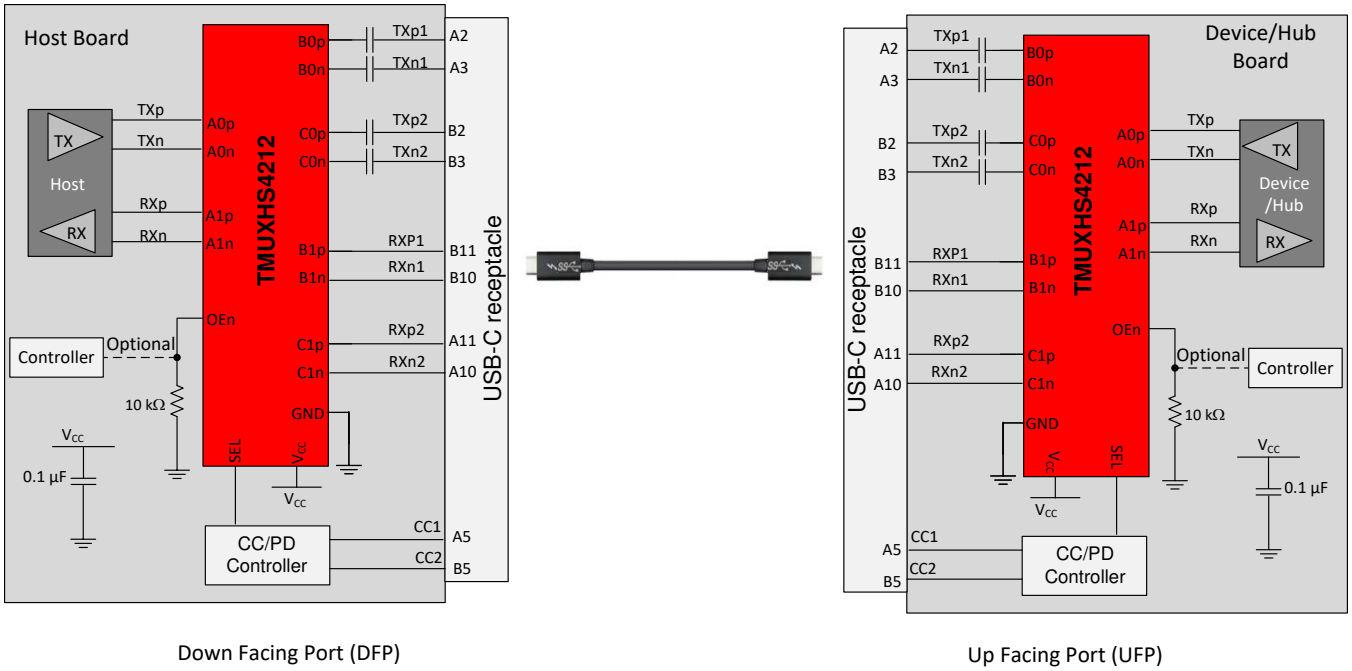


Figure 9. USB 3.2 Implementation for USB Type-C™ Connector

9.2.1.1 Design Requirements

The TMUXHS4212 can be designed into many different applications. All the applications have certain requirements for the system to work properly. The TMUXHS4212 requires 3.3 V ±10% V_{CC} rail. The OEn pin must be low for device to work; otherwise, it disables the outputs. This pin can be driven by a processor. The expectation is that one side of the device has AC coupling capacitors. Table 2 provides information on expected values to perform properly.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
AXp/n, BXp/n, CXp/n CM input voltage	0 V to 1.8 V
Control/OEn pin max voltage for low	0.5 V
Control/OEn pin min voltage for high	1.42 V
AC coupling capacitor	75 nF to 265 nF
R_{BIAS} (Figure 9) when needed	1 kΩ to 100 kΩ

ADVANCE INFORMATION

9.2.1.2 Detailed Design Procedure

The TMUXHS4212 is a high-speed passive switch device that can behave as a mux or demux. Because this is a passive switch, signal integrity is important because the device provides no signal conditioning capability. The device can support 2 to 3 inches of board trace and a connector on either end.

To design in the TMUXHS4212, the designer needs to understand the following.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and OEn pins.
- The thermal pad must be connected to ground.
- See the application schematics on recommended decouple capacitors from V_{CC} pins to ground

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

9.2.1.3 Application Curves

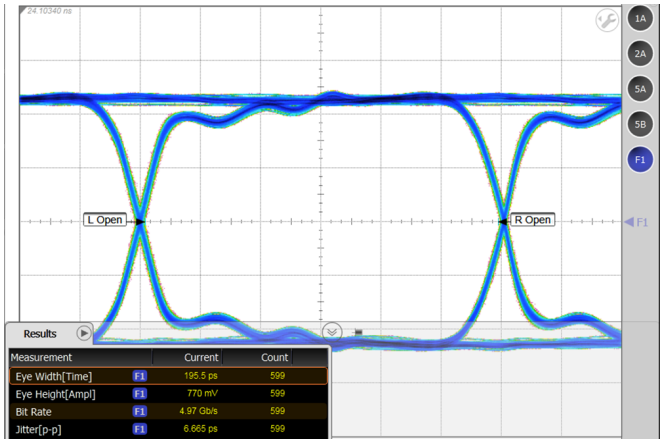


Figure 10. 5 Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

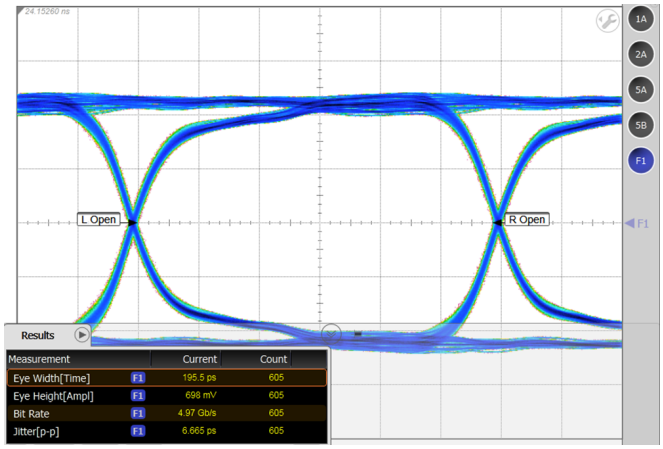


Figure 11. 5 Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

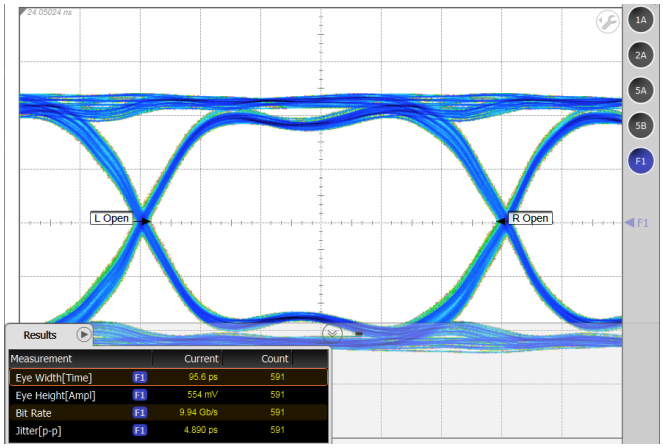


Figure 12. 10 Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

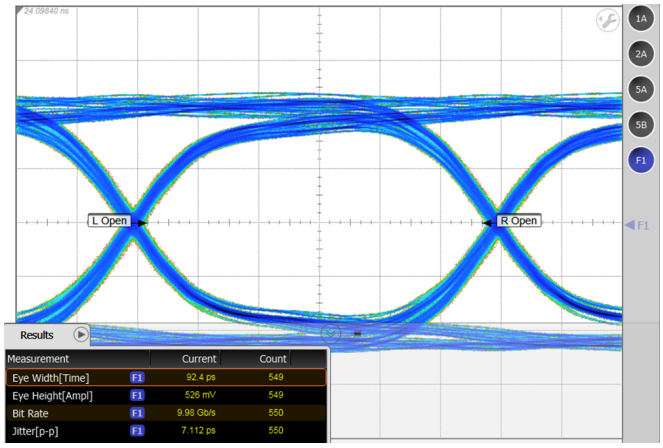


Figure 13. 10Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

ADVANCE INFORMATION

9.2.2 PCIe Lane Muxing

The TMUXHS4212 can be used to switch PCIe lanes between two slots. In many PC and server motherboards, the CPU does not have enough PCIe lanes to provide desired system flexibility for end customers. In such applications, the TMUXHS4212 can be used to switch PCIe TX and RX lanes between two slots. Figure 14 provides a schematic where eight TMUXHS4212 are used to switch eight PCIe TX and eight RX lanes. Note the common mode voltage (CMV) bias for the TMUXHS4212 must be within the range of 0 to 1.8 V. In implementations where receiver CMV bias of a PCIe root complex or an end point can not be ensured within the CMV range, additional DC blocking capacitors and appropriate CMV biasing must be implemented.

Copyright © 2020, Texas Instruments Incorporated

ADVANCE INFORMATION

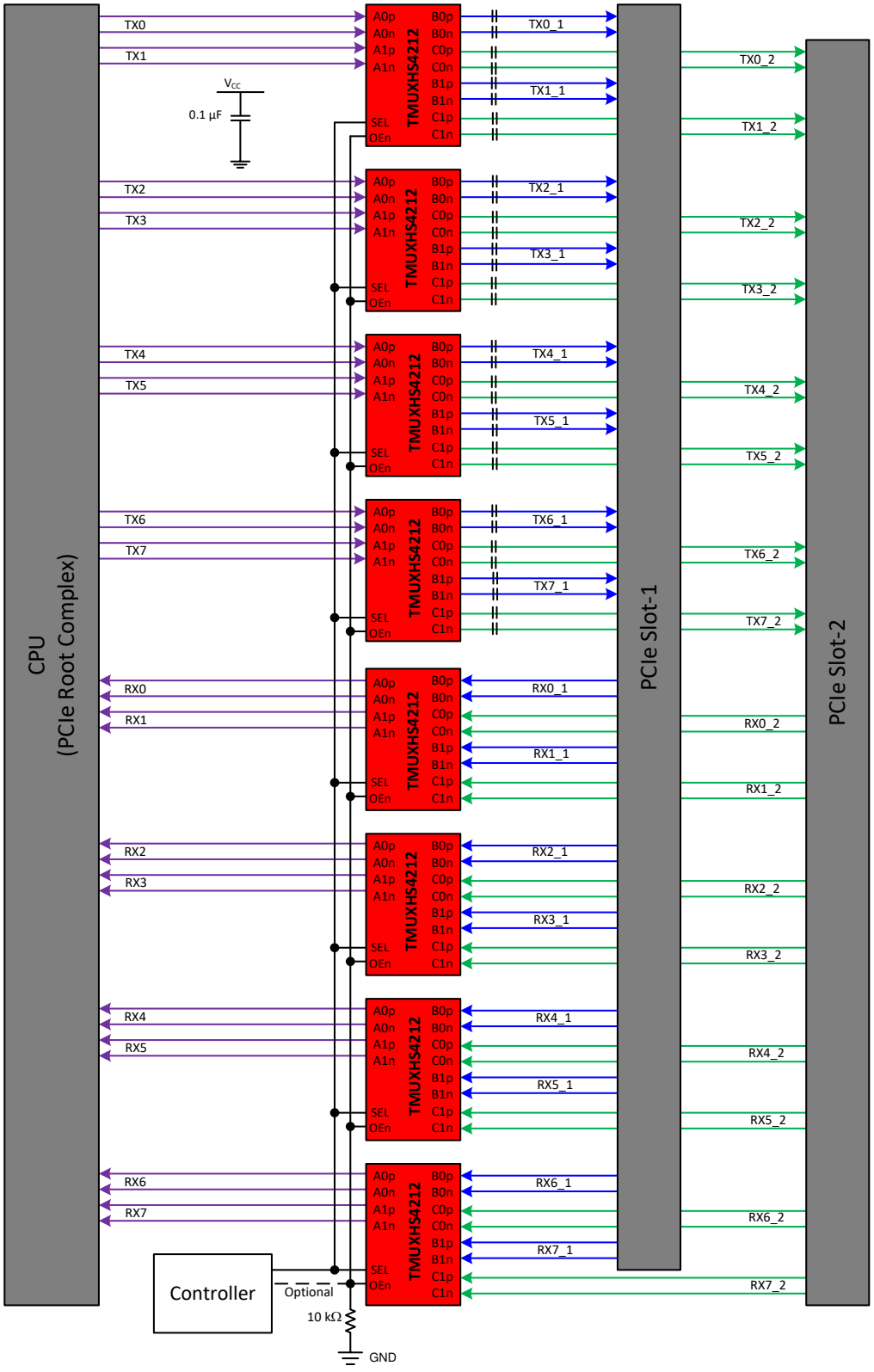


Figure 14. PCIe Lane Muxing

Copyright © 2020, Texas Instruments Incorporated

9.2.2.1 Application Curves

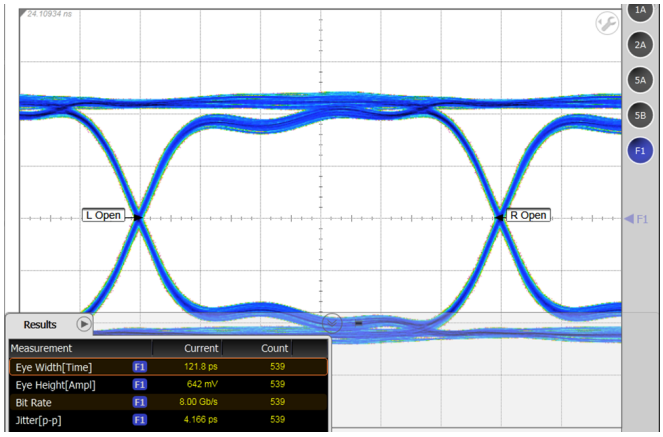


Figure 15. 8 Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

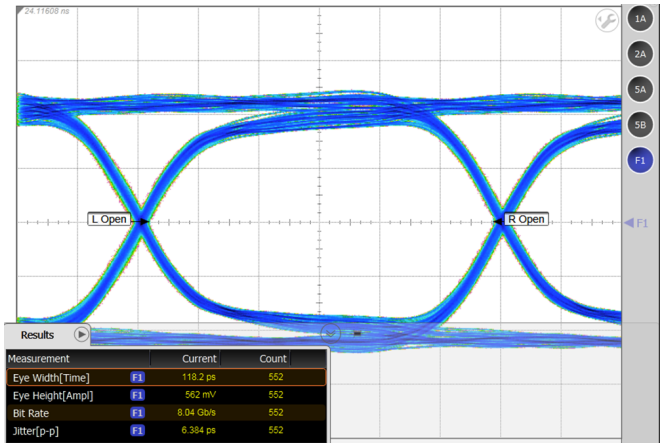


Figure 16. 8 Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

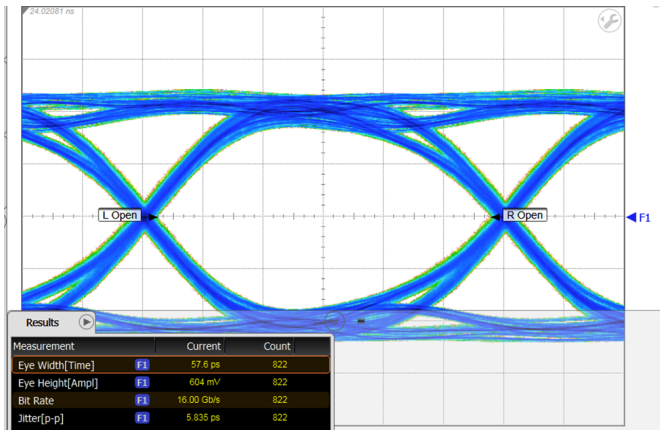


Figure 17. 16Gbps PRBS-7 signals through Calibration Traces in TI Evaluation Board

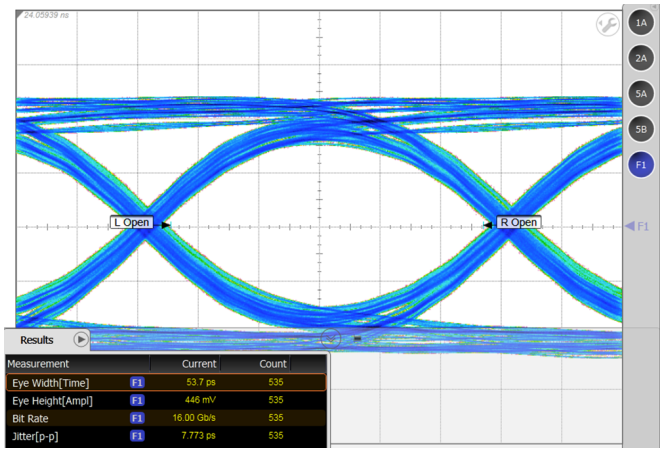


Figure 18. 16Gbps PRBS-7 signals through a Typical TMUXHS4212 channel in TI Evaluation Board

ADVANCE INFORMATION

9.3 Systems Examples

9.3.1 USB/eSATA

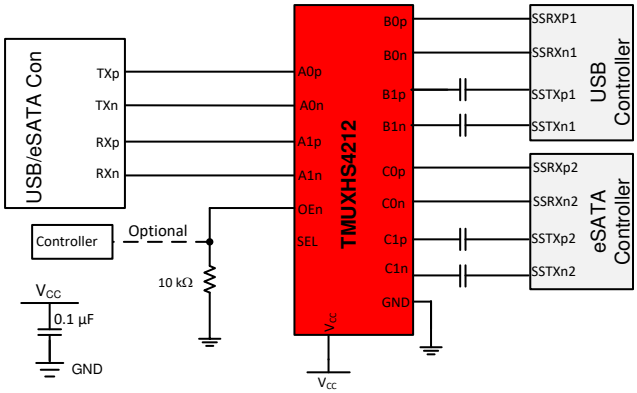


Figure 19. eSATA and USB 3.2 Combo Connector

Systems Examples (continued)

9.3.2 MIPI Camera Serial Interface

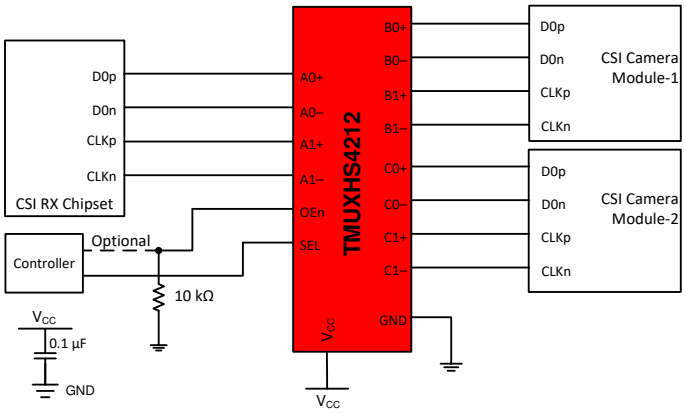


Figure 20. CSI Camera Selection

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

10 Power Supply Recommendations

The TMUXHS4212 does not require a power supply sequence. However, TI recommends that OEn is asserted low after device supply V_{CC} is stable and in specification. TI also recommends to place ample decoupling capacitors at the device V_{CC} near the pin.

11 Layout

11.1 Layout Guidelines

On a high-K board, TI always recommends to solder the Power-pad™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the Power-pad package. On a high-K board, the TMUXHS4212 can operate over the full temperature range by soldering the Power-pad onto the thermal land without vias.

For high speed layout guidelines refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*, SLLA414.

On a low-K board, for the device to operate across the temperature range, the designer must use a 1-oz Cu trace connecting the GND pins to the thermal land. A general PCB design guide for Power-pad packages is provided in *Power-pad Thermally-Enhanced Package*, SLMA002.

11.2 Layout Example

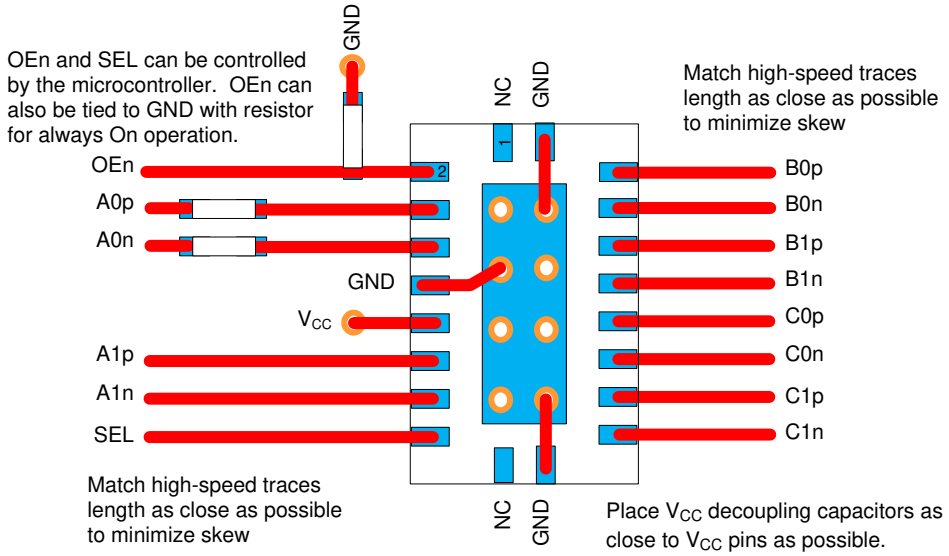


Figure 21. TMUXHS4212 Basic Layout Example for Application Shown in *USB3.2 implementation for USB Type-C*

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

USB Type-C, Power-pad, E2E are trademarks of Texas Instruments.
USB Type-C is a registered trademark of USB Implementation Forum.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

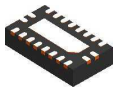
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

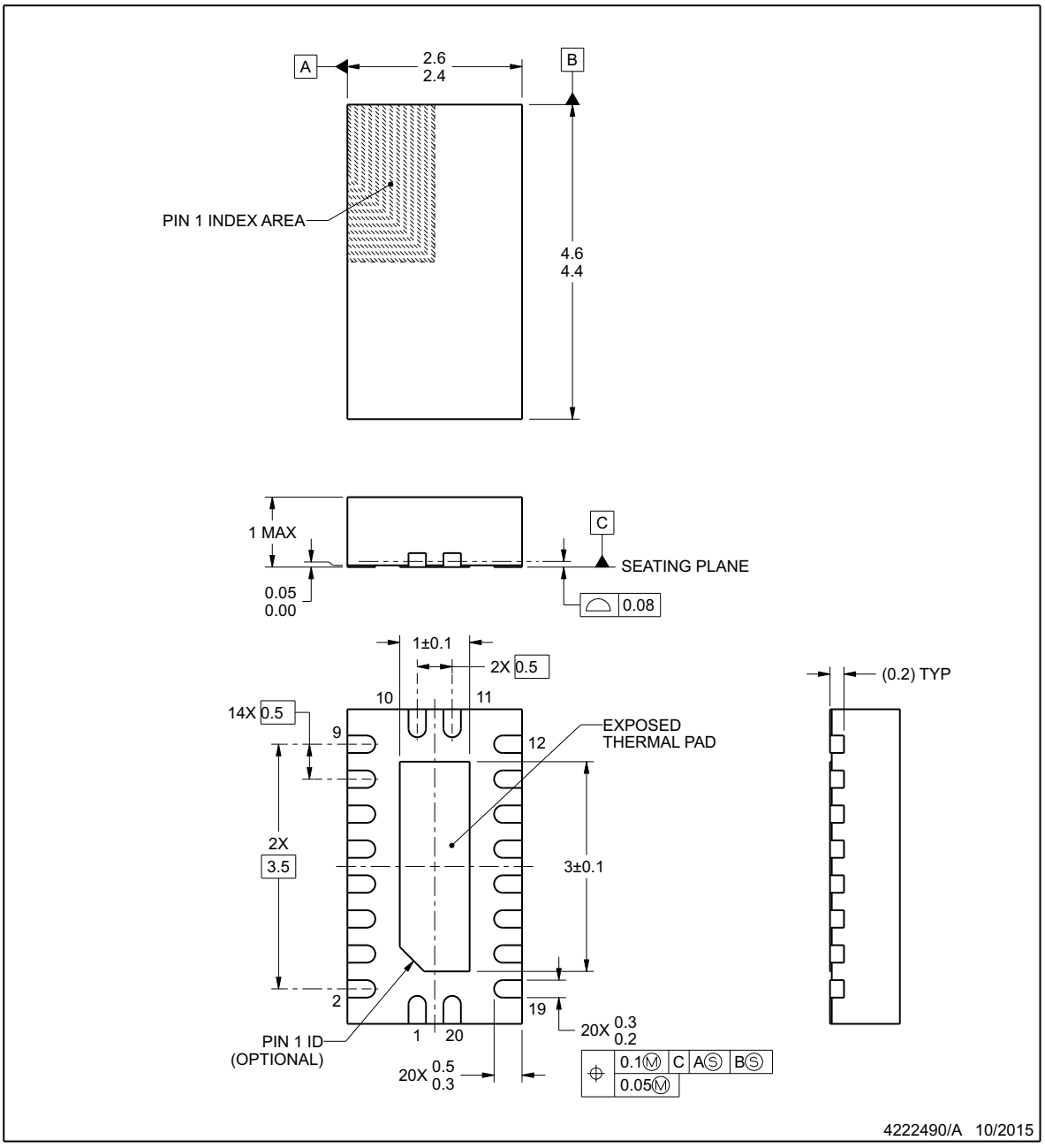
PACKAGE OUTLINE

RKS0020A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

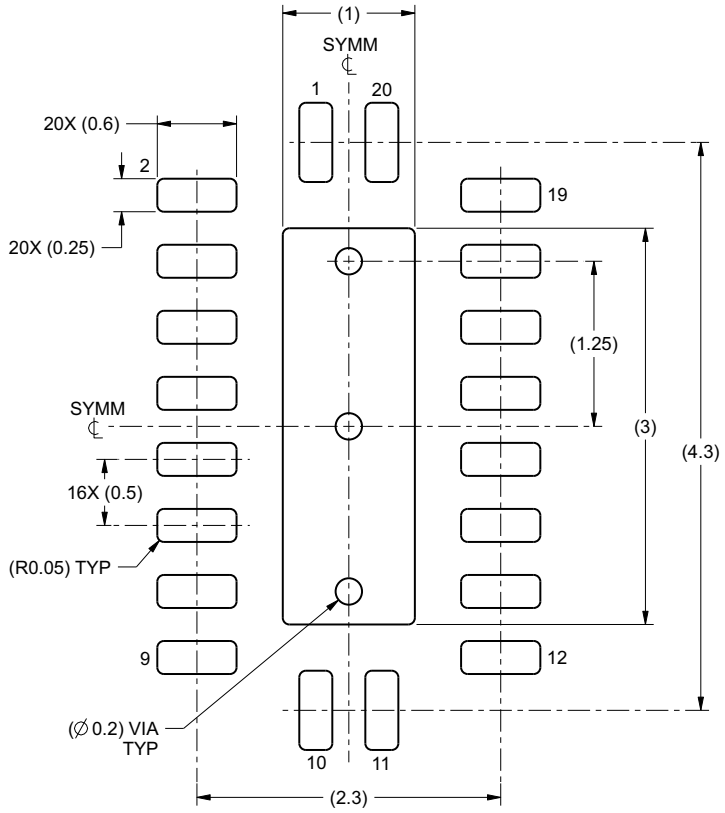
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

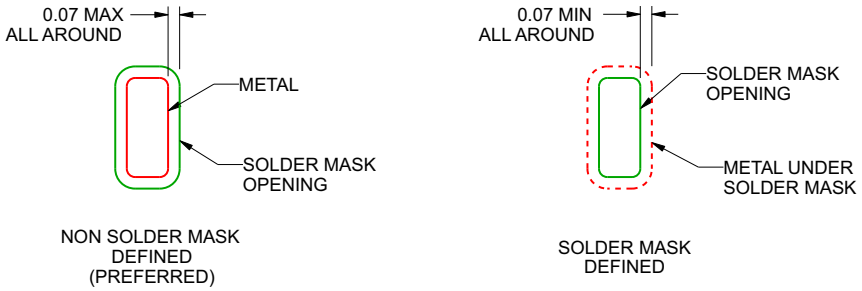
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/A 10/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

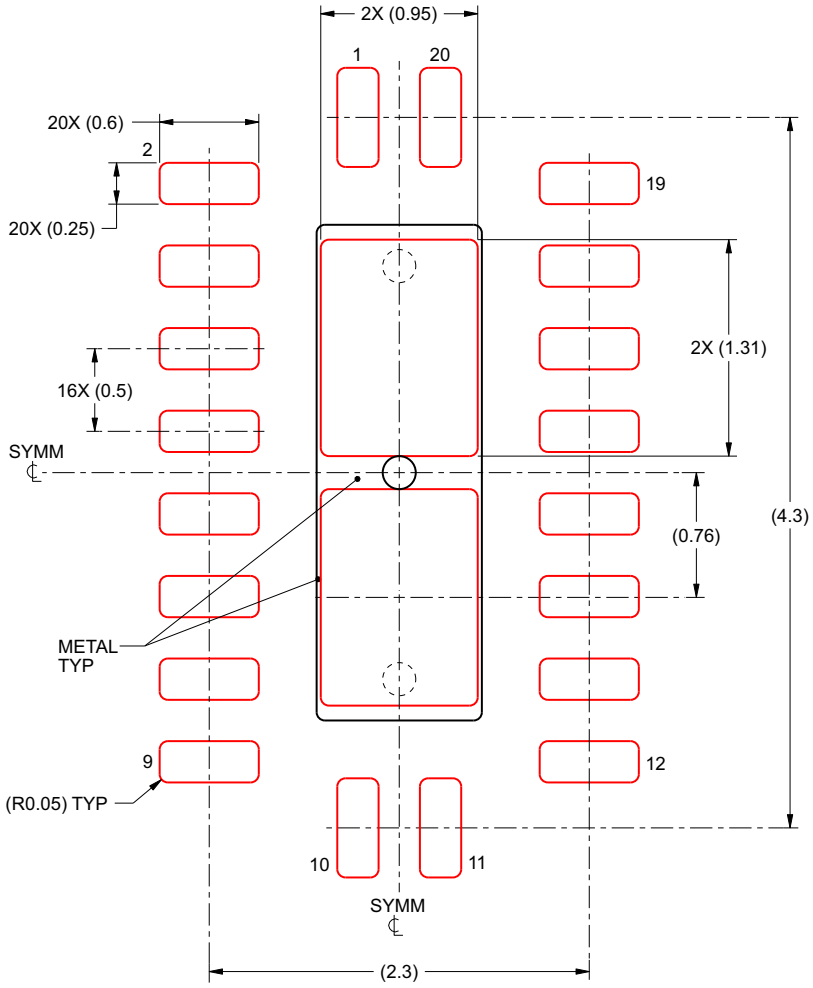
Copyright © 2020, Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/A 10/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

Copyright © 2020, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTMUXHS4212RKSR	ACTIVE	VQFN	RKS	20	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

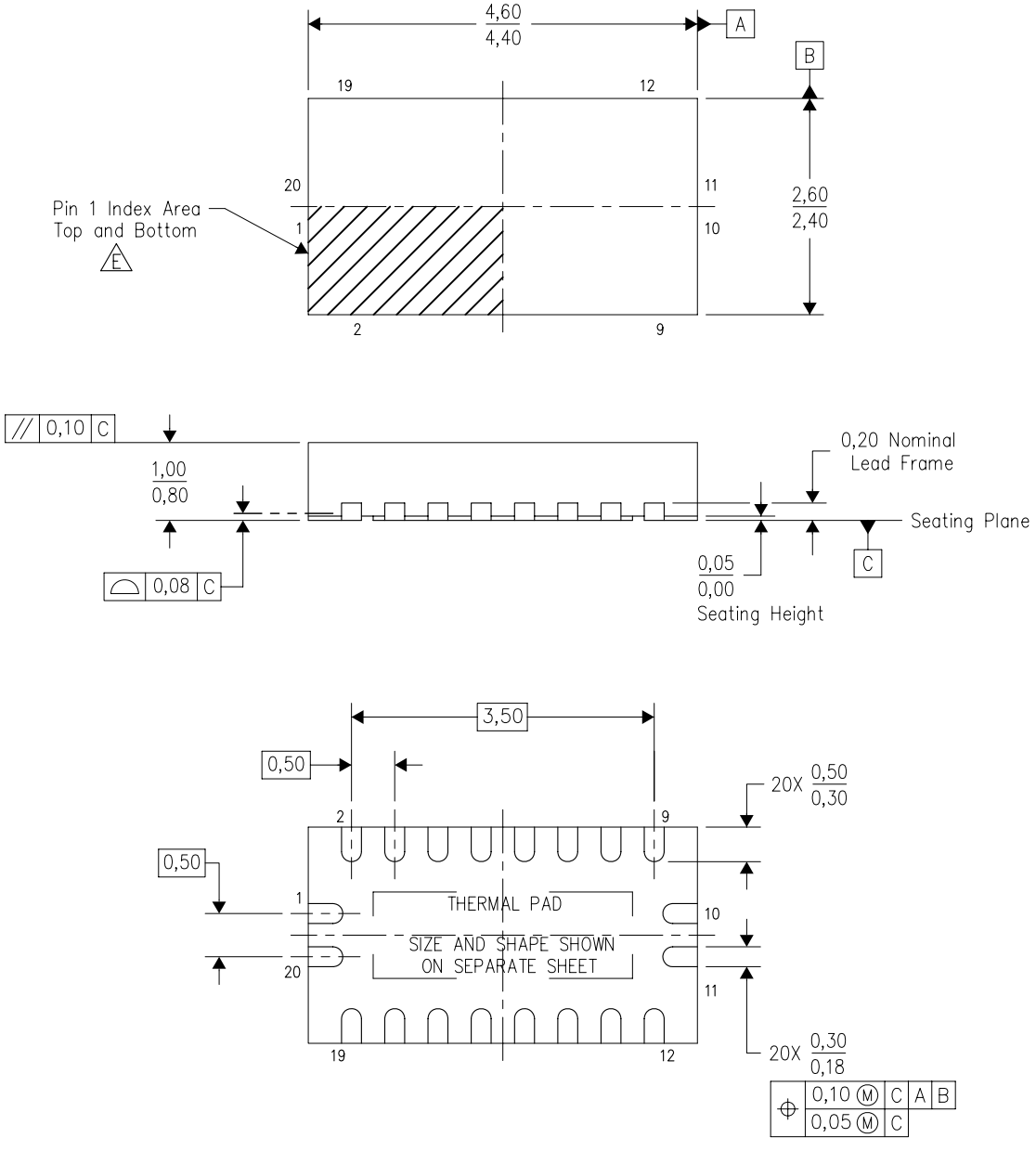
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RKS (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4211377/B 01/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated