Dual Mode DisplayPort™ to DVI/HDMI™ Electrical Bridge (Level Shifter)

Features

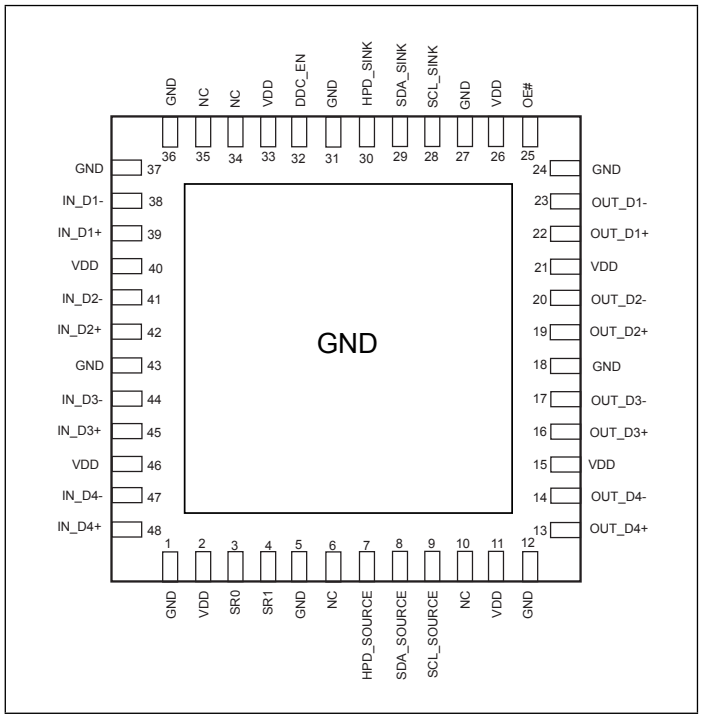
- Converts low-swing AC coupled differential input to HDMI™ rev 1.3 compliant open-drain current steering Rx terminated differential output
- HDMI Level shifting operation up to 2.5Gbps per lane (250MHz pixel clock)
- Integrated 50-ohm termination resistors for AC-coupled differential inputs.
- Enable/Disable feature to turn off TMDS outputs to enter low-power state.
- Output slew rate control on TMDS outputs to minimize EMI
- Integrated Passive DDC level shifters (3.3V source to 5V sink)
- Transparent operation: no re-timing or configuration required
- Level shifter for HPD signal from HDMI/DVI connector
- Integrated pull-down on HPD_sink input guarantees "input low" when no display is plugged in
- 3.3V Power supply required
- TMDS output enable control
- ESD protection on all I/O pins
  - 4kV HBM
  - ±8kV contact ESD protection on the following pins
    - → OUT_Dx±
    - → SDA_SINK, SCL_SINK
    - → HPD_SINK
- Packaging (Pb-free & Green available):
  - 48 TQFN, 7mm × 7mm (ZBE)

Description

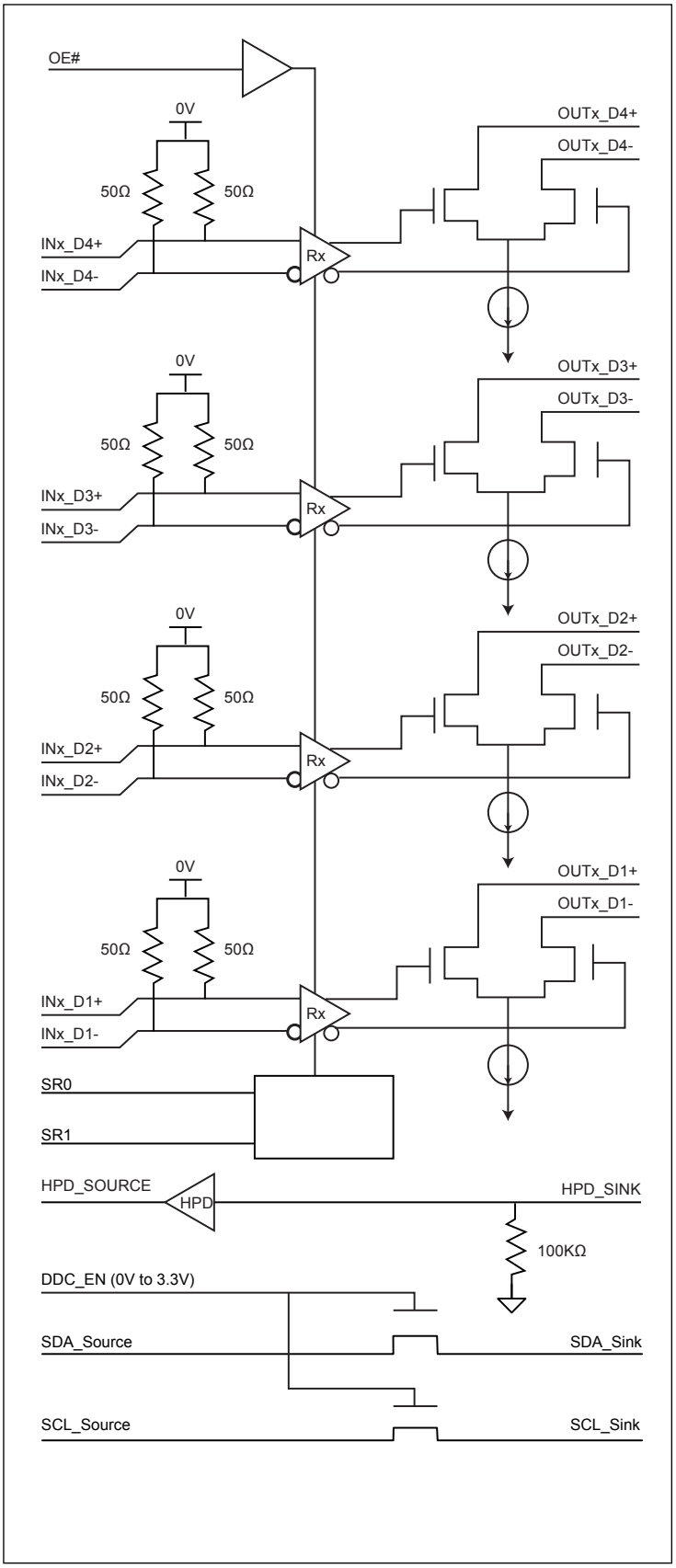
Pericom Semiconductor's PI3VDP411LSR provides the ability to use a Dual-mode DisplayPort™ transmitter in HDMI™ mode. This flexibility provides the user a choice of how to connect to their favorite display. All signal paths accept AC coupled video signals. The PI3VDP411LSR converts this AC coupled signal into an HDMI rev 1.3 compliant signal with proper signal swing. This conversion is automatic and transparent to the user.

The PI3VDP411LSR supports up to 2.5Gbps, which provides 12-bits of color depth per channel, as indicated in HDMI rev 1.3.

Pin Configuration (48-Pin TQFN)



Block Diagram



Pin	Name	I/O Type	Descriptions
1, 5, 12, 18, 24, 27, 31, 36, 37, 43	GND	POWER	GROUND
2, 11, 15, 21, 26, 33, 40, 46	V_{DD}	POWER	POWER, 3.3V ±10%
3	SR0	I	Slew Rate Control. Acceptable connections to SR0 pin are: resistor to 3.3V or short to GND. (internal 200KΩ pull-LOW)
4	SR1	I	Slew Rate Control. Acceptable connections to SR1 pin are: resistor to 3.3V or short to GND. (internal 200KΩ pull-LOW)
6, 10, 34, 35	NC	O	No Connect
7	HPD_SOURCE	O	HPD_SOURCE: 0V to 3.3V (nominal) output signal. HPD_Sink input can be as high as 5V and then HPD_Source will output no higher than 3.3V.
8	SDA_SOURCE	I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage limiting integrated NMOS passgate.
9	SCL_SOURCE	I/O	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting integrated NMOS passgate
13	OUT_D4+	O	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-.
14	OUT_D4-	O	HDMI 1.3 compliant TMDS output. OUT_D4- makes a differential output signal with OUT_D4+
16	OUT_D3+	O	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-.
17	OUT_D3-	O	HDMI 1.3 compliant TMDS output. OUT_D3- makes a differential output signal with OUT_D3+
19	OUT_D2+	O	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-.
20	OUT_D2-	O	HDMI 1.3 compliant TMDS output. OUT_D2- makes a differential output signal with OUT_D2+
22	OUT_D1+	O	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-.
23	OUT_D1-	O	HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+
25	OE#	I	Enable for IN_Dx to OUT_Dx level shifter path. OE# / IN_D Termination / OUT_D Outputs 1 / > 100KΩ / High-Z 0 / 50Ω / Active
28	SCL_SINK	I/O	5V DDC Clock I/O. Pulled up by external termination to 5V. Connected to SCL_SOURCE through voltage limiting integrated NMOS passgate.

Pin	Name	I/O Type	Descriptions
29	SDA_SINK	I/O	5V DDC Data I/O. Pulled up by external termination to 5V. Connected to SDA_SOURCE through voltage limiting integrated NMOS passgate.
30	HPD_SINK	I	Low Frequency, 0V to 5V (nominal) input signal. This signal comes from the TMDS connector. Voltage High indicates "plugged" state; voltage low indicated "unplugged". HPD_SINK is pulled down by an integrated 100K ohm pull-down resistor.
32	DDC_EN	I	Enables bias voltage to the DDC passgate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass gates themselves.) DDC_EN: Passgate 0V: Disable 3.3V: Enable
38	IN_D1-	I	Low-swing diff input from DP Tx outputs. IN_D1- makes a differential pair with IN_D1+.
39	IN_D1+	I	Low-swing diff input from DP Tx outputs. IN_D1+ makes a differential pair with IN_D1-.
41	IN_D2-	I	Low-swing diff input from DP Tx outputs. IN_D2- makes a differential pair with IN_D2+.
42	IN_D2+	I	Low-swing diff input from DP Tx outputs. IN_D2+ makes a differential pair with IN_D2-.
44	IN_D3-	I	Low-swing diff input from DP Tx outputs. IN_D3- makes a differential pair with IN_D3+.
45	IN_D3+	I	Low-swing diff input from DP Tx outputs. IN_D3+ makes a differential pair with IN_D3-.
47	IN_D4-	I	Low-swing diff input from DP Tx outputs. IN_D4- makes a differential pair with IN_D4+.
48	IN_D4+	I	Low-swing diff input from DP Tx outputs. IN_D4+ makes a differential pair with IN_D4-.

Absolute Maximum Ratings (Over operating free-air temperature range)

Item	Rating
Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V_{DD}+0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

Table: Power Supplies and Temperature Range

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{DD}	3.3V Power supply	3.0	3.3	3.6	V	
I_{CC}	Max Current			100	mA	
I_{CCQ}	Standby Current			2	mA	OE# = HIGH
T_{CASE}	Case temperature range for operation with spec.	-40		85	Celsius (°)	

Table: Differential Input Characteristics for IN_Dx signals

Symbol	Parameter	Min	Typ	Max	Units	Comments
T_{bit}	Unit Interval	360			ps	T_{bit} is determined by the display mode. Nominal bit rate ranges from 250Mbps to 2.5Gbps per lane. Nominal Tbit at 2.5 Gbps = 400 ps. 360ps = 400ps-10%
V_{RX_DIFF}	Input Differential Voltage level	0.175		1.200	V	See note 1 below
T_{RX_EYE}	Minimum Eye Width at IN_D input pair	0.8			T_{bit}	The level shifter may add a maximum of 0.02UI jitter (400 * 0.02) = 8ps
$V_{CM-ACp-p}$	AC Peak Common Mode Input Voltage			100	mV	See note 2 below
Z_{RX_DC}		40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50 ±20% tolerance).
$Z_{RX-Bias}$		0		2.0	V	Intended to limit power-up stress on chipset's PCIE output buffers.
Z_{RX_HIGH-Z}		100			k Ω	Differential inputs must be in a high impedance state when OE# is HIGH.

1. $V_{RX-DIFF} = 2x|V_{RX-D-} - V_{RX-D-}|$ Applies to IN_Dx signals

2. $V_{CM-AC-p-p} = |V_{RX-D-} - V_{RX-D-}|/2 - V_{RX-CM-DC}$

$V_{RX-CM-DC}$ = DC(avg) of $|V_{RX-D+} + V_{RX-D-}|/2$

$V_{CM-AC-p-p}$ includes all frequencies above 30 kHz.

TMDS Outputs

The level shifter's TMDS outputs are required to meet HDMI 1.3 specifications.

The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Truth Table (Slew Rate control function)

SR1	SR0	Rise/Fall Time (Typ)
1	1	140ps
1	0	130ps
0	1	120ps
0	0	110ps

Test Setup Condition

V_{DD} = 3.3V, Ambient temperture 25°C

Rise/Fall time is from 20% to 80% on Rising/Falling edge

Date rate: 620 Mbps

Input: 1V differential peak-to-peak clock pattern

Equalization : 3dB

Table 1: OE Pin Description

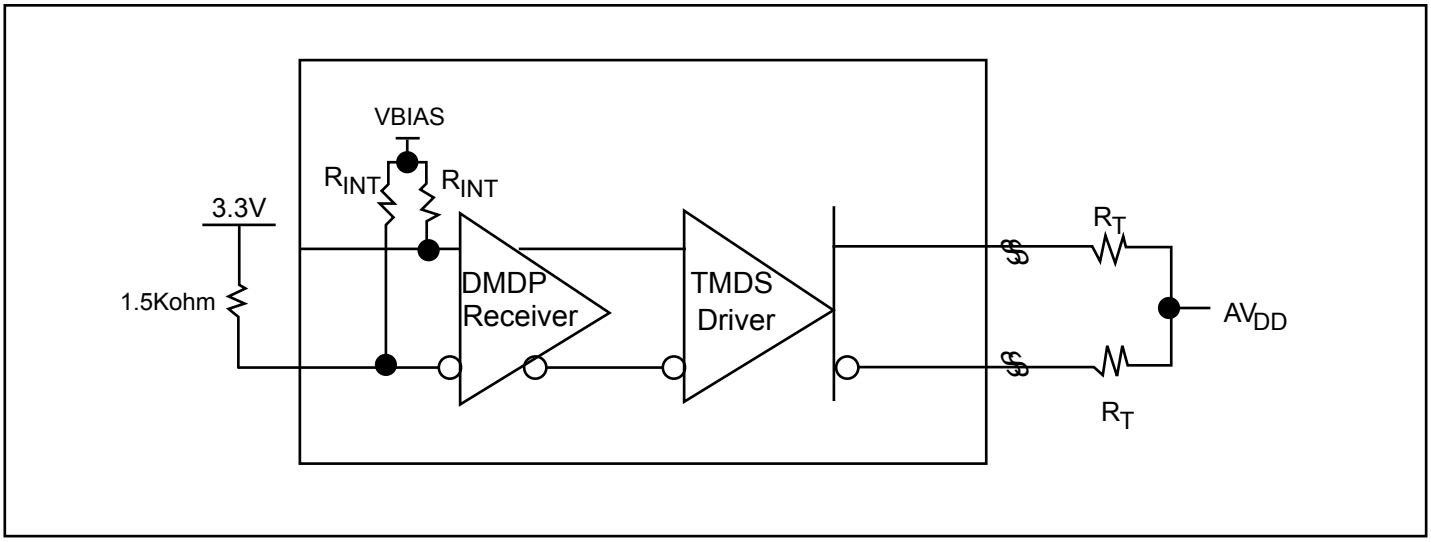
OE#	Device State	Comments
Asserted (low voltage)	Differential input buffers and output buffers enabled. Input impedance = 50Ω	Normal functioning state for IN_D to OUT_D level shifting function.
Unasserted (high voltage)	Low-power state. ▫ Differential input buffers and termination are disabled. ▫ Differential inputs are in a high impedance state. ▫ OUT_D level-shifting outputs are disabled. ▫ OUT_D level-shifting outputs are in high impedance state. ▫ Internal bias currents are turned off.	Intended for lowest power condition when: ▫ No display is plugged in or ▫ The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE# SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE#

Table 2: Differential Output Characteristics for TMDS_OUT signals

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_H	Single-ended high level output voltage	V_{DD}-10mV	V_{DD}	V_{DD}+10mV	V	V_{DD} is the DC termination voltage in the HDMI or DVI Sink. V_{DD} is nominally 3.3V
V_L	Single-ended low level output voltage	V_{DD}-600mV	V_{DD}-500mV	V_{DD}-400mV	V	The open-drain output pulls down from V_{DD}.
V_{SWING}	Single ended output swing voltage	425	500	600	mV	Swing down from TMDS termination voltage (3.3V ±10%)
I_{OFF}	Single-ended current in high-Z state			50	µA	Measured with TMDS outputs pulled up to V_{DD} Max _(3.6V) through 50Ω resistors.
$T_{SKEW-INTRA}$	Intra-pair differential skew			30	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins. HDMI revision 1.3 source allowable intrapair skew is 0.15 T_{bit}.
$T_{SKEW-INTER}$	Inter-pair lane-to-lane output skew			100	ps	This lane-to-lane skew budget is in addition to skew between differential input pairs
T_{JIT}	Jitter added to TMDS signals			25	ps	Jitter budget for TMDS signals as they pass through the level shifter. 25ps = 0.056 T_{bit} at 2.25 Gb/s

TMDS output oscillation elimination

The inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. Pericom recommends to add a 1.5Kohm pull-up to the CLK- input.



TMDS Input Fail-Safe Recommendation

Table 3: HPD Characteristics

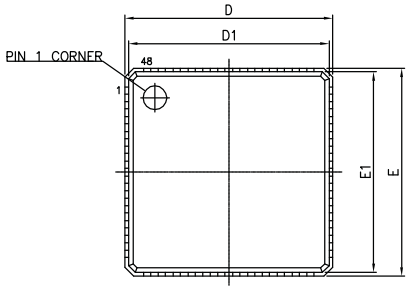
Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{IH-HPD}	Input High Level	2.0	5.0	5.3	V	Low-speed input changes state on cable plug/ unplug
V_{IL-HPD}	HPD_sink Input Low Level	0		0.8	V	
I_{IN-HPD}	HPD_sink Input Leakage Current			70	µA	Measured with HPD_sink at V_{IH-HPD} max and V_{IL-HPD} min
V_{OH-HPD}	HPD_source Output High-Level	2.5		V_{DD}	V	V_{DD} = 3.3V ±10% I_{OH} = -4mA(MIN) / -8mA(MAX)
V_{OL-HPD}	HPD_source Output Low-Level	0		0.4	V	I_{OL} = 4mA(MIN) / 8mA(MAX)
T_{HPD}	HPD_sink to HPD_source propagation delay			200	ns	Time from HPD_sink changing state to HPD_source changing state. Includes HPD_ source rise/fall time
$T_{RF-HPDB}$	HPD_source rise/ fall time	1		20	ns	Time required to transition from $V_{OH-HPDB}$ to $V_{OL-HPDB}$ or from $V_{OL-HPDB}$ to $V_{OH-HPDB}$

Table 4: OE# Input, DDC_EN

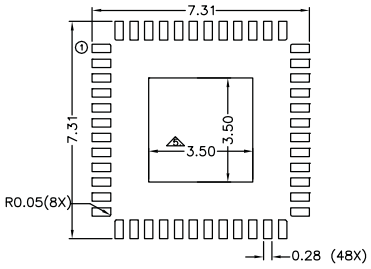
Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{IH}	Input High Level	2.0		V_{DD}	V	TMDS enable input changes state on cable plug/unplug
V_{IL}	Input Low Level	0		0.8	V	
I_{IN}	Input Leakage Current			10	µA	Measured with input at V_{IH-EN} max and V_{IL-EN} min

Table 5: Termination Resistor

Symbol	Parameter	Min	Typ	Max	Units	Comments
R_{HPD}	HPD_sink input pull-down resistor.	100K			Ω	Guarantees HPD_sink is LOW when no display is plugged in.



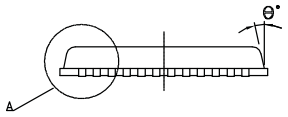
TOP VIEW

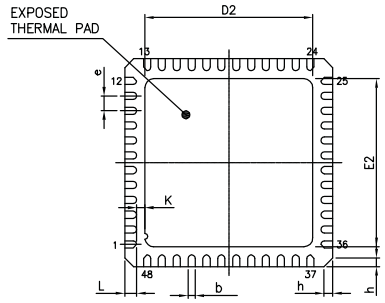


RECOMMENDED LAND PATTERN (TOP VIEW)

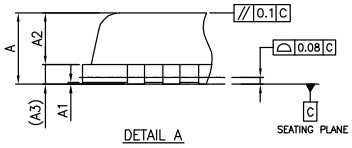
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
h	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	—	—
L	0.30	0.40	0.50
θ°	0.00	—	12.00

UNIT : mm





BOTTOM VIEW



DETAIL A

	D2			E2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
157X157MIL	3.40	3.60	3.80	3.40	3.60	3.80
213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40
208X208MIL	4.90	5.10	5.30	4.90	5.10	5.30

UNIT: mm

Notes:
1. All dimensions are in millimeters, angles are in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area

PERICOM Semiconductor Corporation

DATE: 02/11/09

DESCRIPTION: 48-Pin, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZB48

DOCUMENT CONTROL #: PD-2080 **REVISION: A**

09-0091

Note:
- **For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php**

Ordering Information

Ordering Code	Package Code	Package Type
PI3VDP411LSRZBE	ZB	Pb-free & Green, 48-pin TQFN

1. **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
2. **E = Pb-free and Green**
3. **Adding an X suffix = Tape/Reel**

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