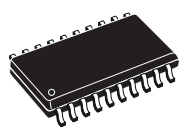
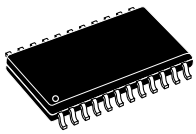
L7203

SMOOTH DRIVE SPINDLE MOTOR FOR OPTICAL DRIVE APPLICATION WITH POWER INTEGRATED

- SMOOTH DRIVE™ SYSTEM
- 1.8A DRIVE PEAK CAPABILITY
- SLEW RATE CONTROL
- INDUCTIVE SENSE START-UP ROUTINE
- THERMAL SHUTDOWN
- SUITABLE FOR 5V AND 12V APPLICATION
- ONLY ONE HALL SENSOR IS REQUIRED



SO20



SSO24

ORDERING NUMBERS: L7203 (SO20)
L7203S (SSO24)

DESCRIPTION

The L7203 SPINDLE MOTOR IC includes a three phase brushless spindle motor controller and the power stage in switching mode. The device is designed for both 5V and 12V OPTICAL DRIVE application requiring up to 1.8A peak of current.

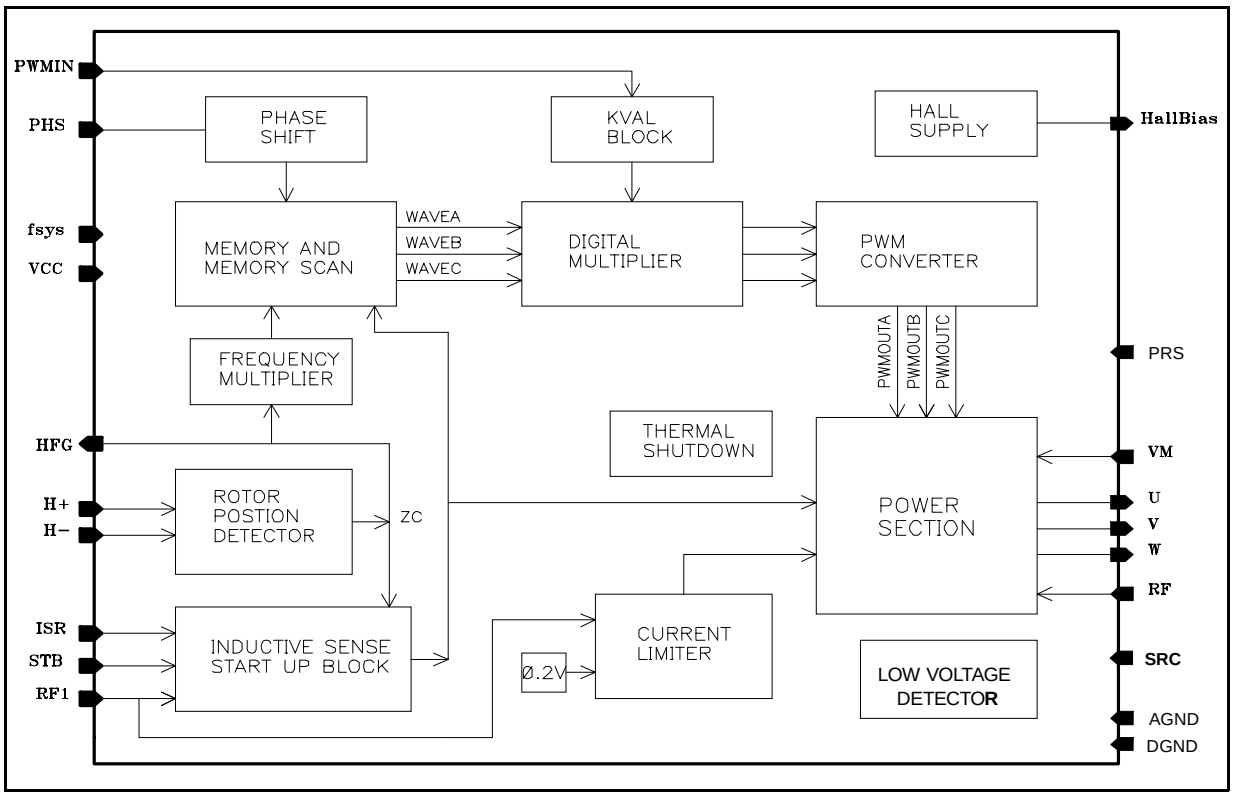
The device is realized in BCD5, a 0.7 µm Mixed technology.

The spindle motor position detection is carried out by means of a single comparator with hysteresis. In the start-up phase the "inductive sense start up method" is used to detect the rotor position, determining the direction of starting rotation. This procedure is implemented by a logic circuit on chip.

The device applies three sinusoidal voltages to the motor coils.

This is obtained through the application of the

BLOCK DIAGRAM



DESCRIPTION (continued)

SMOOTH DRIVING concept.

It is based on the idea of driving the motor winding through 3 sinusoidal voltages dephased of 120 degrees. The motor is controlled in voltage mode, so no current control compensation network is required.

Each profile is digitally described by 36 bytes stored in a ROM memory.

These sinusoidal signals are modulated by multiplying each sample by a value stored in the KVAL register. Using this kind of profiles it is possible to obtain great advantages such as torque ripple and acoustic noise reduction and lower EMI. An easier track following is ensured, since vibration are reduced.

The clock signal on the chip can be synchronized to the external application clock signal.

An internal circuit can limit the current. The threshold is fixed with a internal 0.2 V reference.

The device generates:

- a current generator to define output voltage slew rate
- a 3.3 V reference to bias hall sensor.
- the HFG open drain output signal for speed regulation.

The device includes :

- a circuit for thermal shutdown with hysteresis.
- a low voltage detector

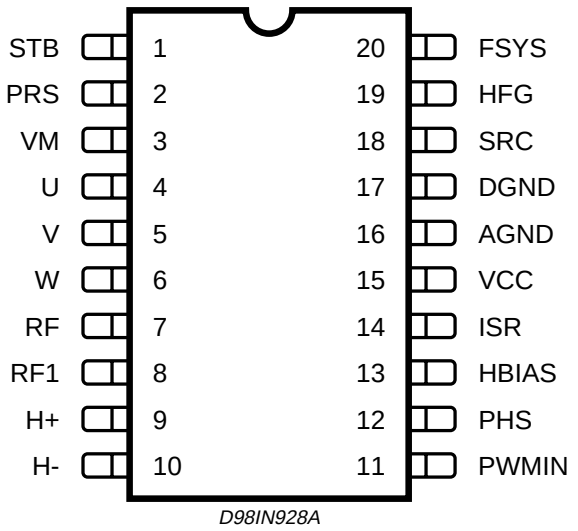
In the STANDBY state the main functions of the device are turned off, in order to minimize the power consumption.

The STANDBY state of the device is imposed by:

- Thermal shutdown
- stand by signal from µP

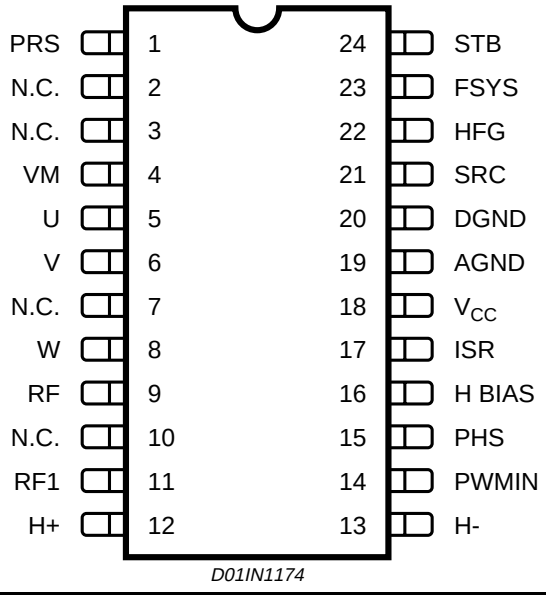
PIN CONNECTIONS

SO20



D98IN928A

SSO24



D01IN1174

PIN DESCRIPTION

PIN	DESCRIPTION	TYPE
POWER AND GROUND		
VM	Supply voltage for power stages +12/5V	P12
VCC	Supply for 5V core	P5
DGND	Logic ground	G
AGND	Analog ground	G
DIGITAL PIN		
PWMIN	PWM input signal to calculate kval	IC5
Fsys	System frequency	IC5
PHS	Phase Shift Pin	IC5
PRS	Prescaler Pin	IC5
STB	Start and Stop signal	ZD5
HFG	Open Drain F-Generator signal from Spindle Motor	OD5
HALL SENSOR		
BIAS	3.3V reference to bias Hall sensor	OA5
H+, H-	Hall sensor differential input	IA5
INDUCTIVE SENSE REFERENCE		
ISR	Inductive sense reference	IA5
MOTOR CONTROL		
OUTV	Winding output U	OA12
OUTV	Winding output V	OA12
OUTW	Winding output W	OA12
RF	Current sense resistor (force)	OA12
RF1	Current sense resistor (sense)	IA5
SLEW RATE CONTROL		
SRC	Slew Rate Control	OA5

INPUT DEFINITION

IC5 Input CMOS, 3.3-5V capability with hysteresis
ZD5 Bidirectional, open drain, 3.3-5V capability
OD5 Output, open drain, 3.3-5V capability

IA5 Input, Analog, 5V
OA5 Output, Analog, 5V

OA12 Output, Analog, 12V

P12 Power 12V / 5V
P5 Power 5V
G Ground

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction to Pins	Max.	16	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	Max.	90	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{amb}	Ambient Temperature	-20 to 80	°C
T_{op}	Operating Temperature	0 to 150	°C
T_{smin}	Minimum Thermal Circuit Threshold	140	°C
V_M		-0.3 to 15	Vdc
V_{CC}		-0.3 to 7	Vdc
	U, V, W, (low side drive =off)	-0.3 to 17	Vdc
	PWMIN, PHS, FSYS, TEST, STB, HFG, BIAS, H+, H-, RF1, RF, ISR, PORPin	-0.3 to V_{CC}+0.3	Vdc
P_{D1}	Power dissipation at sustained operation with a package $R_{thj\text{-}amb}$ at 90°C	1	W
ESD	Susceptibility	2000	Vac
T_{STG}	Storage Temperature	-55 to 150	°C
I_{OLHFG}	HFG open drain current	10	mA
I_{Peak}	Motor Peak Current	1.8	A

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V; V_M = 12V; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply 5V operating range		4.25		5.75	V
V_M	Supply 12V operating range	(note 1)	10.2		13.8	V
V_M	Supply 5V operating range		4.25		5.75	V
I_{Vcc}	V_{CC} Supply Current	V_{CC} = 5.75; f_{sys} = 20MHz STB = 0 (bias pin open) STB =1			1.3 20	mA mA
V_{VM}	V_M Supply Current	V_M = 13.8 STB = 0 STB =1			1 7	mA mA
PWMIN, PHS, PRS, Fsys						
V_{iL}	Input Low Voltage				1	V
V_{iH}	Input High Voltage		2.2			V
V_{iHYS}	Input Hysteresis			100		mV
I_z	Leakage Current	V_{CC} = 5.75	-10		+10	µA
STB						
V_{iL}	Input Low Voltage				1	V
V_{iH}	Input High Voltage		2.2			V
V_{OL}	Open Drain Output	IOL = 2mA V_{CC} = 4.25V			0.4	V
V_{iHYS}	Input Hysteresis			100		mV
I_z	Leakage Current	V_{CC} = 5.75, Therm off	-10		+10	µA
HFG						
V_{OL}	Open Drain Output	IOL = 2mA V_{CC} = 5V			0.4	V
I_z	Leakage Current	V_{CC} = 5.75, HFG hiz	-10		+10	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BIAS						
V_{BIAS}	BIAS Output Voltage	V_{CC} = 5V; 5mA < I < 15mA	3.25		3.75	V
I_{Bmax}	Max Output Current				15	mA
H+, H-						
$V_{H\pm}$	H+ H- Input Voltage Range		0		2.5	V
$I_{H\pm}$	Input Leakage Current	V_{in} = 0, +V_{CC}	-10		+10	µA
V_{OFFISR}	Comparator Offset		-15		+15	mV
VHy	Comparator Hysteresys		4		15	mV
MOTOR POWER STAGE						
R_{DSON}	High and Low side FET on Resistance	T_j = 125; V_M = 4.25V I = 1.2A			2	Ω
$I_{U/V/W}$	Spindle Output Leakage Current	V_M = 15V			100	µA
CURRENT LIMITER						
V_{Lim}	Internal Reference Voltage for current limitation		220	240	260	mV
V_{OFFLim}	Comparator Offset		-15		+15	mV
THERMAL PROTECTION						
T_S	Shutdown temperature		130		170	°C
UNDERVOLTAGE						
$V_{ccth\ (fall)}$	Undervoltage threshold (fall)		2.9	-	-	V
$V_{ccth\ (rise)}$	Undervoltage threshold (rise)		-	-	3.4	V
$V_{ccth\ (hys)}$	Undervoltage threshold (hys)		-	0.1	-	V
SYSTEM FREQUENCY						
f_{sys}	System frequency	PRS = 0 PRS = 1	10 20		20 34	MHz MHz
SLEW RATE CONTROL						
V_{SRC}	SRC Output Voltage			1.25		V
I_{SRC}	Output Current				500	µA
R_{SRC}	External Resistor on pin SRC		10			KΩ
ISR						
V_{ISR}	Input Range		0		2	V

Note 1: An SMBJIZAVCL-TR is recommended to clamp V_M in case of high impedance on power supply line.

FUNCTIONAL DESCRIPTION

STB-Thermal protection

Controller drive STB pin by open drain.

When Thermal Shutdown is excited, the device force this pin LOW.

Controller will manage STB to do a re-start.

When STB is LOW all the drivers are shut off.

Hall Sensor Bias

A regulator on chip supply a 3.3V+-10% reference on pin Bias. This regulator can supply an output current up-to 15 mA.

Figure 1.

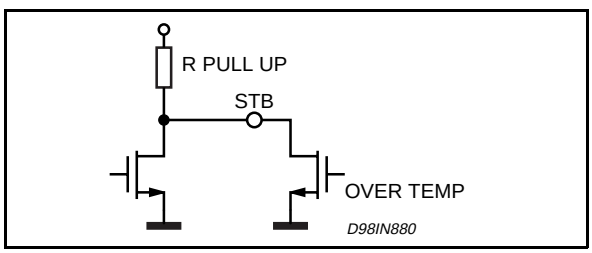


Figure 2.

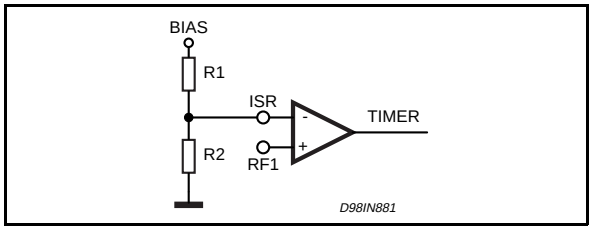
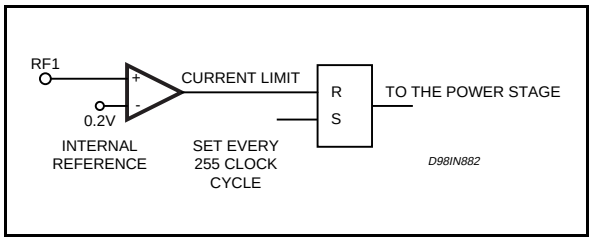


Figure 3.



Inductive Sense Start Up Block

The inductive sense method allows to determine the position and the direction of the starting rotation of the motor.

With the rotor at rest, a voltage Vn is applied subsequently to two motor phases, according to this sequence: UW, VW, VU, WU, WV, UV.

A timer measures the rise time dT to reach the reference current ISR in each phase.

This reference is fixed on the pin ISR with a resistor divider between the pin BIAS and GND.

Through a comparator is possible to determine the phase which has the minimum rise time and so the rotor position is univocally determinated.

Figure 5.

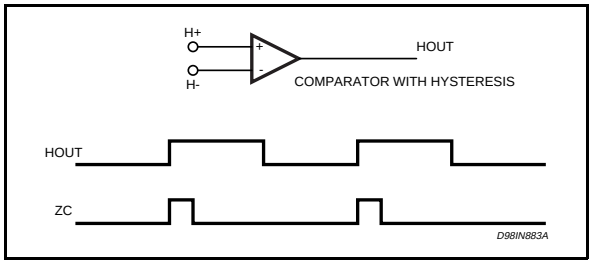
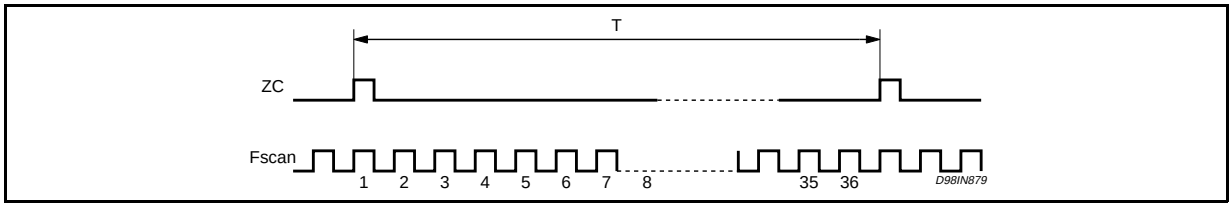


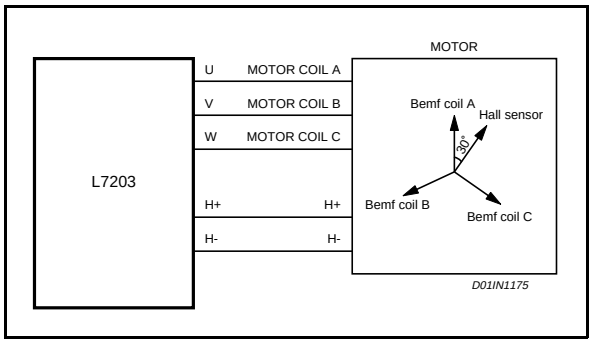
Figure 6.



The start up is a procedure allowing to start the motor avoiding any backrotation. This procedure is realized by a customized logic on chip (no modification required in the external microprocessor software).
For the Motor Connection please refer to the Fig. 4.

Current Limiter

Figure 4. Motor Connections.



The current limiter aim is to avoid that the current in the motor winding overides a fixed threshold value. The voltage input at the pin RF1 is compared with an internal 0.2V reference.

When the current exceeds the Ilimit value a flip-flop is reset masking (through a combinational logic) the signal to the power windings.

Rotor Position Detector

This block is connected to the Hall Sensor Output. A comparator with hysteresis receives the sinusoidal hall-sensor signal and generates a squared signal HOUT.

The Zero-Cross signal is generated starting from the HOUT signal as in fig. 5.

The HOUT signal can be read from the microprocessor on the output open drain pin HFG.

Frequency multiplier

The Frequency Multiplier generates the memory scan frequency (Fscan) starting from the Zero-Cross (ZC) signal from the Rotor Position Detector block. The scan frequency relates to the rate of the samples of the input signals.

The number of wave samples in a period T is 36, so this circuit generates 36 pulses between 2 Zero Crossing.

Fscan has a frequency 36 times of (1/T). The Fscan is generated from the Zero-cross frequency measured at the previous cycle.

So, if the motor speed changes, the zero-cross is not constant, the Frequency Multiplier adjusts the scan clock, ensuring the synchronization between the Zero-Cross signal and the sinusoidal output voltage.

Memory and Memory Scan

The memory stores 3x36 samples describing 3 signals. As each sample is represented in a byte, it may have a value in the range 0 to 255.

The shape of these three signals are designed in order to generate three sinusoidal voltages across the Motor coils ensuring the highest performances in term of power losses and motor speed. The shape of the signals are reported in fig. 7.

In Fig 8 is swown the "differential" voltage across the motor coil U and the motor coil V. Obviously, the voltage shape across the motor coil U and W and the voltage across the motor coil V and W are also sinusoidal and dephased of 120 and 240 degrees respect the voltage shown in fig. 8.

The Memory and Memory scan block receives the scan clock, and at each clock provides the sample addressed by an internal address register.

Figure 7.

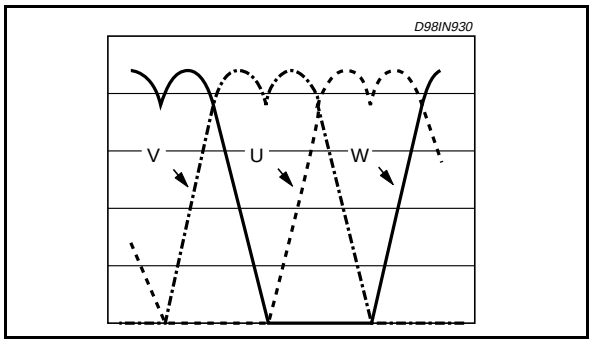
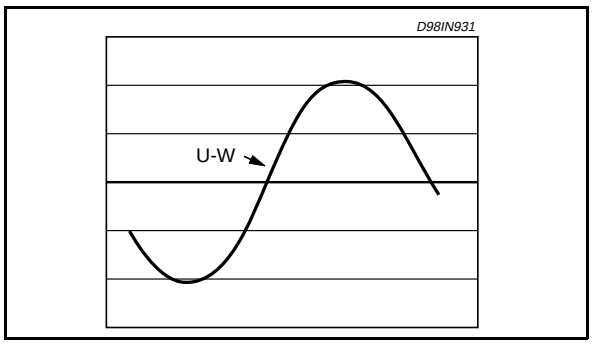


Figure 8.



This register is initialized with the memory address of the wave sample synchronized with the Zero-Cross signal. The maximum efficiency (i.e. the maximum motor speed for a particular value of current) for the motor driving may be reached ensuring a particular value PH of dephase between the Zero-Cross signal and the voltage output signal.

This value is written by the external controller using PHS pin (see Phase Shift Block section).

Kval Block and PWM interface

This unit contains a register storing the Kval value. The Kval value represents a multiplying factor to modulate the 3 profile signals amplitude and it is generated starting from the PWMIN signal coming from the external system controller.

The Kval block receives the PWMIN signals and calculates the Kval value through the reference triangular signal.

This signal is generated by a 10 bit counter that starts counting from 1023 to 0 at Fsys rate, and then restart up to 1023. The resolution is ±1LSB.

Internal triangular wave is synchronized with the PWMIN falling edge.

The PWMIN signal contains information regarding both the amplitude and to the sign of the control variable. If the duty cycle is less than 50% the Kval is in the range (-1023, -1), while if the duty cycle is equal or greater than 50% the kval is in the range (0, 1023).

A negative Kval value (i.e. PWM duty cycle from 0 to 50%) indicates an active brake and generates a 180 degree shift in the voltage profile scan.

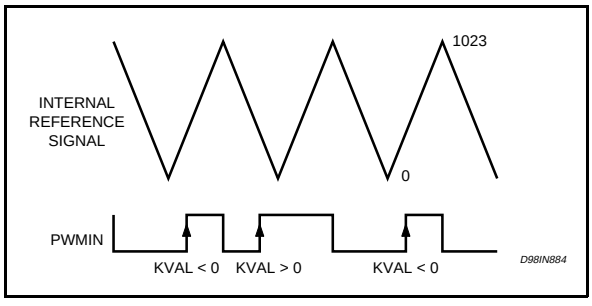
The rising edge of the PWMIN signal determines the kval on the reference triangular waveform.

If the PWMIN signal is stable during the entire cycle, the Kval is evaluated according to the following rule:

- PWMIN signal stable to 1 -> Kval = +1023
- PWMIN signal stable to 0 -> Kval = -1023

In order to ensure the synchronization between

Figure 9.



the PWMIN signal and the internal signals, the PWMIN signal rate must be calculated by the external microcontroller using the same frequency signal provided to the chip through the pin fsys.

Digital Multiplier

This unit contains a multiplier executing the multiplication of each sample provided by the memory by the value stored in kval register.

The output value is a 10-bit word, plus the sign bit.

PWM Converter

The PWM converter receives from the digital multiplier three 10 bit digital number and converts it into three PWM signals.

A counter counts up (from 0 to 255) and down (from 255 to 0) at the Fsys rate in continuos mode. Three 8-bit input registers are written with the 8 most significant bit of the word to be converted and compared to the counter value. The comparator output is:

Figure 10.

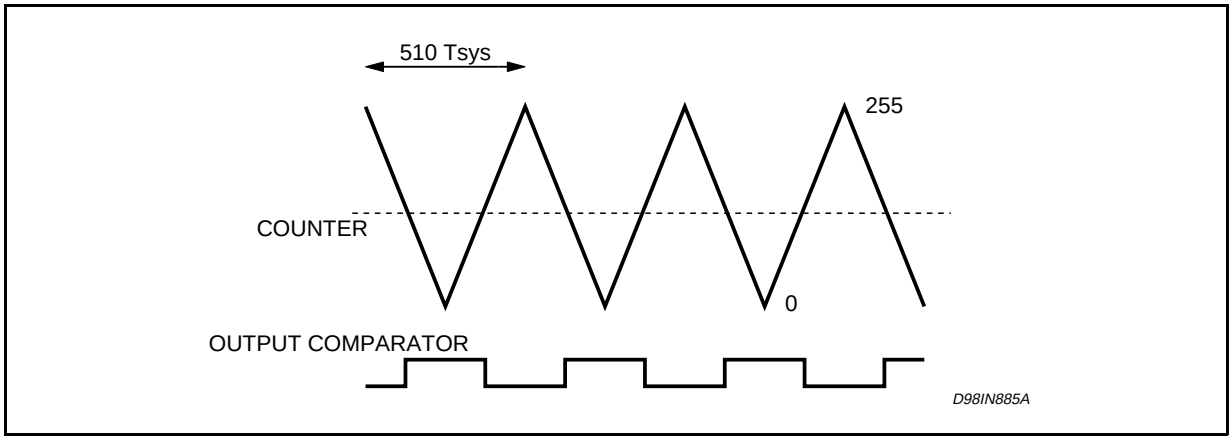
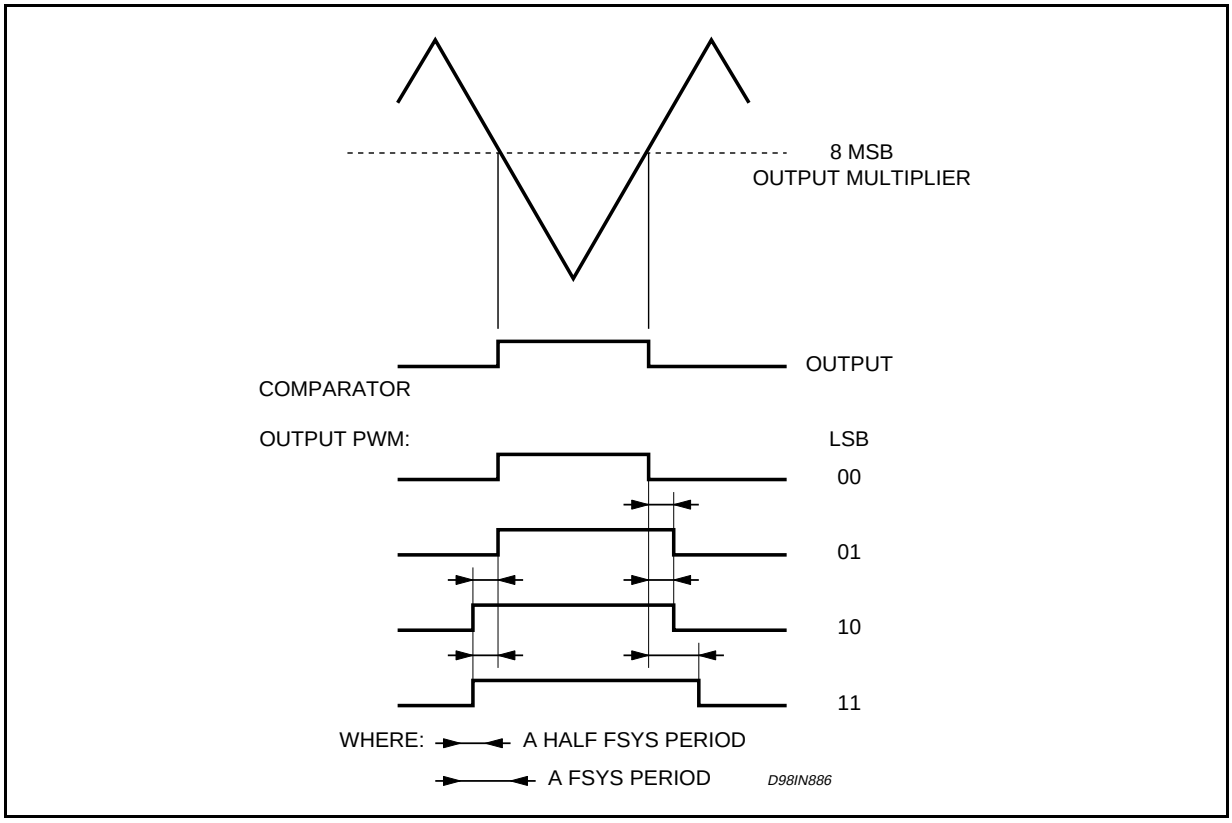


Figure 11.



- 0, if the input value is smaller than the counter output
- 1, if the input value is equal or greater than the counter output

The comparator output is "adjusted" with a combinational logic with the 2 low significant bit of the word to be converted in order to reach a 10 bit precision.

The comparator output duty cycle is extended with a half fsys period for every low bit step how is showed in the figure 11.

Phase Shift Block

This block regulates the phase of the driving signal to control the dephasing between the Zero-Cross signal and the voltage sinusoidal output signal.

It is possible to demonstrate that the maximum efficiency for the motor driving may be reached ensuring a particular value PH of dephase between the Zero-Cross signal and the voltage output signal.

The Phase Shift BLock, starting from the PHS input signal synchronize the wave output with the Zero-Cross signal to ensure the optimum dephase.

The PHS signal expresses the phase shift through the duration of its value according to the following rule:

Table 1.

PHS on	NPhase		Phase Shift (degree)
time µs (Tsys = 50ns)	decimal	bit	
0	0	00000 000	LATCH
0.2	1	00000 001	1.25
0.4	2	00000 010	2.50
0.6	3	00000 011	3.75
0.8	4	00000 100	5.00
1.0	5	00000 101	6.25
1.2	6	00000 110	7.50
1.4	7	00000 111	8.75
1.6	8	00001 000	10
1.8	9	00001 001	11.25
2.0	10	00001 010	12.50
2.2	11	00001 011	13.75
2.4	12	00001 100	15.00
2.6	13	00001 101	16.25
2.8	14	00001 110	17.50
3.0	15	00001 111	18.75
3.2	16	000010 000	20
3.4	17	000010 001	21.25
3.6	18	000010 010	22.50
3.8	19	000010 011	23.75
4.0	20	000010 100	25.00
4.2	21	000010 101	26.25
4.4	22	000010 110	27.50
4.6	23	000010 111	28.75
	.	.	.
	.	.	.
	.	.	.
	.	.	.
16.0	80	001010 000	100
16.2	81	001010 001	101.25
16.4	82	001010 010	102.50
16.6	83	001010 011	103.75
16.8	84	001010 100	105.00
17.0	85	001010 101	106.25
17.2	86	001010 110	107.50
17.4	87	001010 111	108.75
	.	.	.
	.	.	.
	.	.	.
	.	.	.

Table 1. (continued)

PHS on	NPhase		Phase Shift (degree)
time µs	decimal	bit	
56.0	280	100011 000	350
56.2	281	100011 001	351.25
56.4	282	100011 010	352.50
56.6	283	100011 011	353.75
56.8	284	100011 100	355.00
57.0	285	100011 101	356.25
57.2	286	100011 110	357.50
57.4	287	100011 111	358.75
> 57.6	288	100100 000	0

PHS on = tsys * 4 * Nphase

where: tsys = 50ns if fsys = 20MHz

The resulting PHASE SHIFT value is:

PHASE SHIFT = Nphase(8:3) x 10 + Nphase(2:0) x 1.25

For istance if Nphase = 00011 110
PHASE SHIFT = 3 x 10 + 6 x 1.25 = 37.5

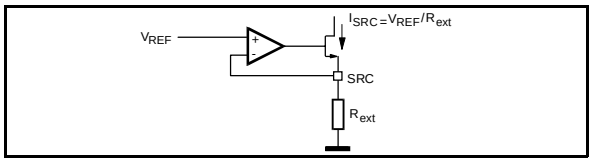
Low Voltage Detector

This circuit detects if V_{CC} is lower than a fixed threshold. If this event happens the internal logic is resetted and the output FETS are forced in High impedance.

Slew Rate Control Circuit

This circuit fixes the slew rate for the output stage in order to reduce EMI.
A reference current is generated by means of an internal reference voltage and an external resistor.
The I_{SRC} is used to fix slew rate with a linear law:

Figure 12.



$$\text{SLEW RATE} = R_{SLR/ISRC} \cdot \frac{V_{REF}}{R_{EXT}}$$

R_{ext} recommended value >10KΩ

Prescaler Pin

The PRS Pin should be forced to ground when the FSYS frequency is lower (or equal) than 20MHz and should be forced to V_{CC} when FSYS frequency is higher than 20MHz, in order to set the correct timing during the inductive sense, start up and resynchronization phases.
Example of different phase shift settings are shown in the following pictures.

Figure 13. Phase relation between OUTPUT sinusoidal voltage (PWM_IN > 50%) and Hall sensor signal writin Phase shift = 0° (default value)

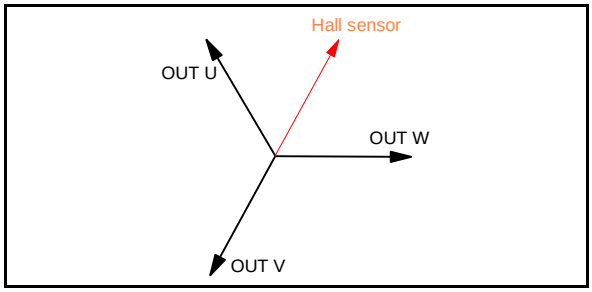


Figure 14. Phase relation between OUTPUT sinusoidal voltage (PWM_IN > 50%) and Hall sensor signal writing Phase shift = 30°

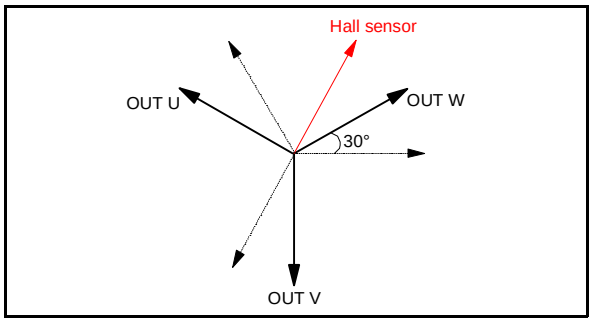
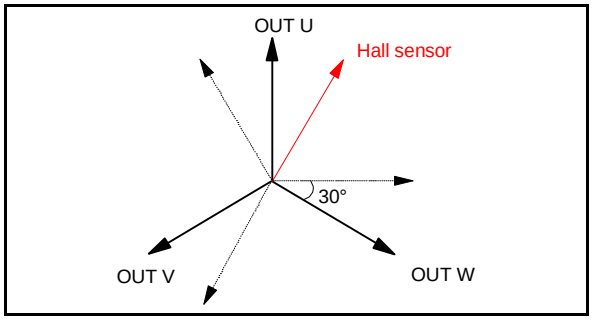
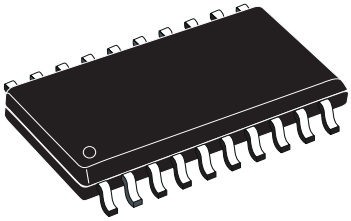


Figure 15. Phase relation between OUTPUT sinusoidal voltage (PWM_IN > 50%) and Hall sensor signal writing Phase shift = 330°

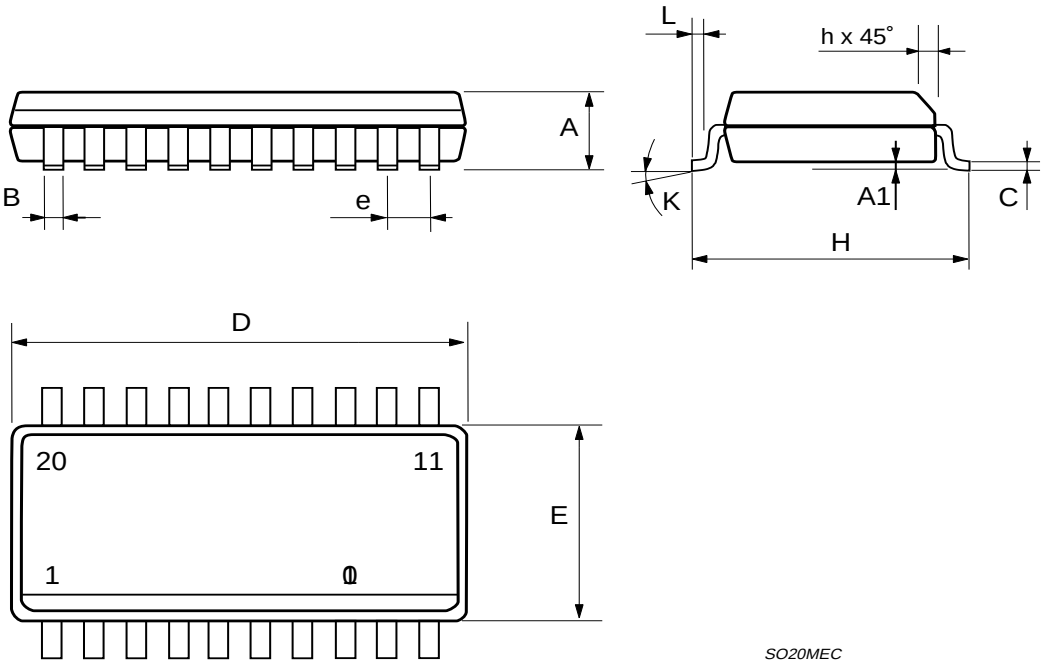


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0˚ (min.)8˚ (max.)					

OUTLINE AND MECHANICAL DATA



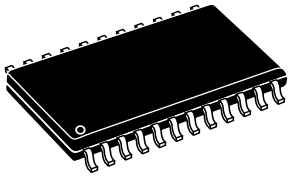
SO20



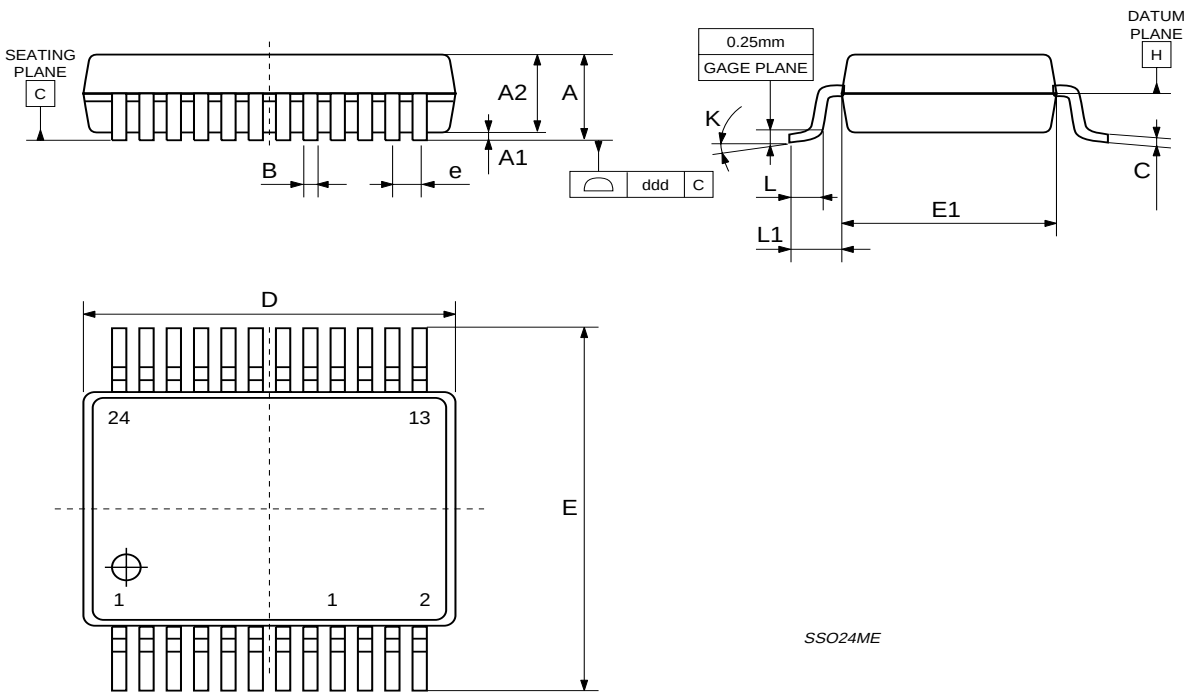
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.00			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.060		0.079
B (2)	0.22		0.38	0.009		0.015
C	0.09		0.25	0.003		0.01
D (1)	7.9	8.2	8.5	0.31	0.32	0.33
E	7.4	7.8	8.2	0.29	0.30	0.32
E1 (1)	5.0	5.3	5.6	0.20	0.21	0.22
e		0.65			0.025	
L	0.55	0.75	0.95	0.022	0.029	0.004
L1		1.25			0.05	
k	0° (min), 4° (typ), 8° (max)					
ddd			0.1			0.004

(1) "D and E1" dimensions do not include mold flash or protusions, but do include mold mismatch and are mesaured at datum plane "H". Mold flash or protusions shall not exceed 0.20mm in total (both side).
(2) "B" dimension does not include dambar protusion/intrusion.

OUTLINE AND MECHANICAL DATA



SSO24
Shrink Small Outline Package



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