AN4541
Application note

EMI filters for SD3.0 card high-speed SD card protection and filtering devices

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Introduction

Non-volatile SD card memory is now widely implemented in various formats (standard, mini and micro) in multimedia hardware such as cameras, computers, GPS and mobile phones. Capacity has rapidly increased to 64 GB, while the data transfer speed has simultaneously reached 95 MB/s for "UHS-I, class 1". These new capabilities are described by the SD3.01 standard, which all devices implementing the standard must adhere to.

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1 Market environment

All sensitive electronic equipment such as mobile phones, computers and peripherals require protection against electrostatic discharge using components able to clamp high voltages, as defined by each standard level, including IEC61000-4-2. Introducing a clamping device between all the parts directly in contact with external environment is a key factor in obtaining reliable and robust equipment, and these devices have to be as transparent as possible in normal working mode in order to maintain signal integrity.

Filtering unwanted frequencies is another interesting feature which, combined with the above mentioned clamping technology, can save PCB area and cost.

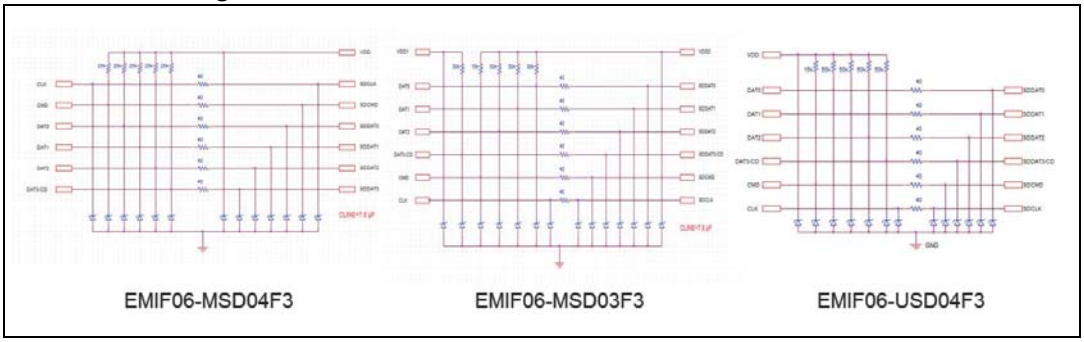
1.1 STMicroelectronics solutions

STMicroelectronics produces three different devices suitable for this application and compliant with the standard, which integrate two kinds of pull-up resistor values and the possibility of implementing electrical card detection:

- EMIF06-MSD04F3
- EMIF06-USD04F3
- EMIF06-MSD03F3

The schematics of these devices are shown below.

Figure 1. STMicroelectronics EMI filter for SD card offer



The basic characteristics of these three filters are the same, especially with respect to the key line capacitance feature. Therefore, all discussion is based on the EMIF06-MSD04F3.

This application note describes the following topics:

1. Filter structure
2. Clamping characteristics
3. SD3.0 timing constraints and PCB layout recommendations
4. Rejection capabilities
5. Electrical card detection capability

2 The ∏ filter structure

The remaining voltage across a TVS device is linked to its clamping characteristic. *Figure 2* shows the voltage across a unidirectional device versus the current flowing through it.

Figure 2. Typical clamping characteristic of a unidirectional TVS

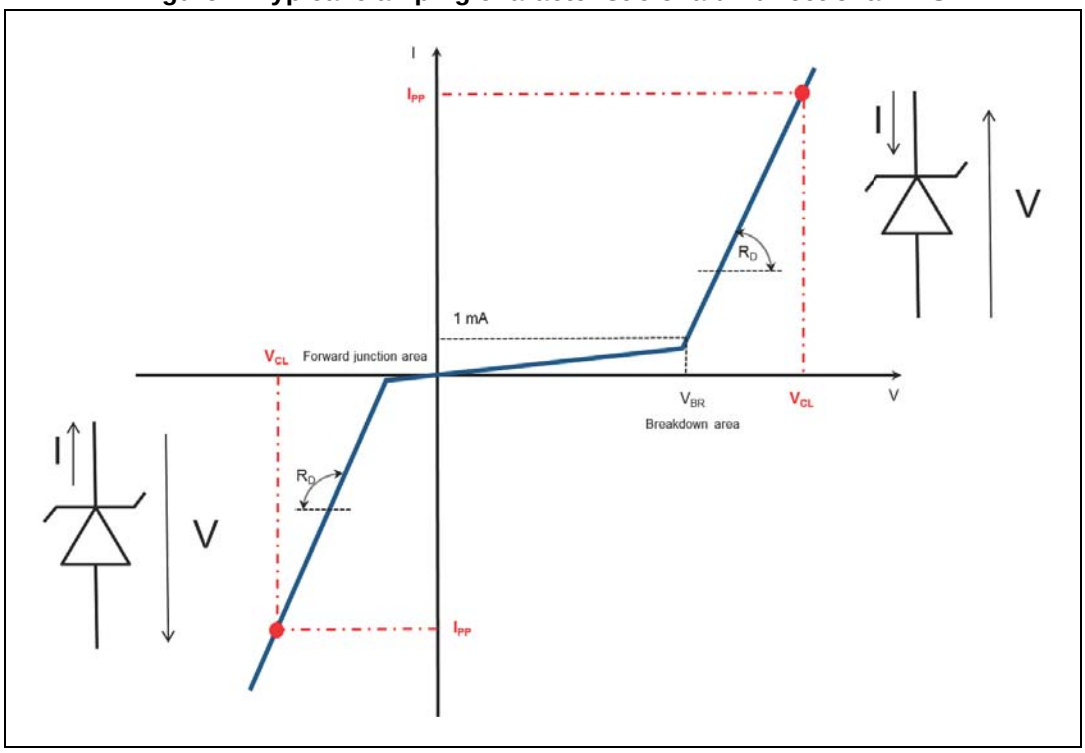


Figure 3 and *Figure 4* show how a structure with two TVSs and a resistor (or a more complex impedance) between them can minimize the clamping voltage. The majority of the current flows through the first TVS, while the remainder (limited by the resistor) flows through the second, effectively reducing the clamping voltage with respect to a single TVS.

Figure 3. Positive surge

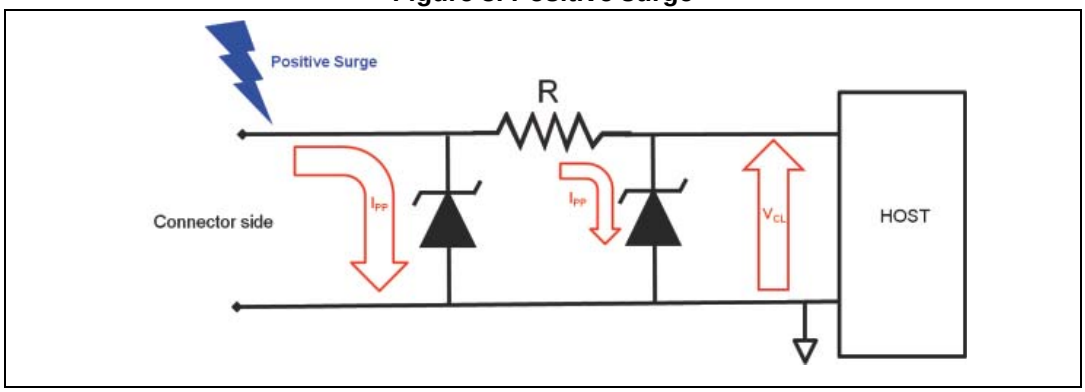
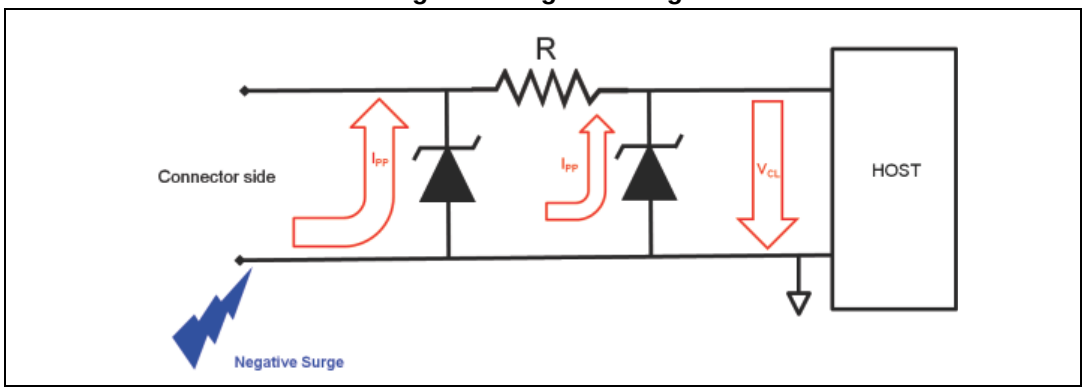


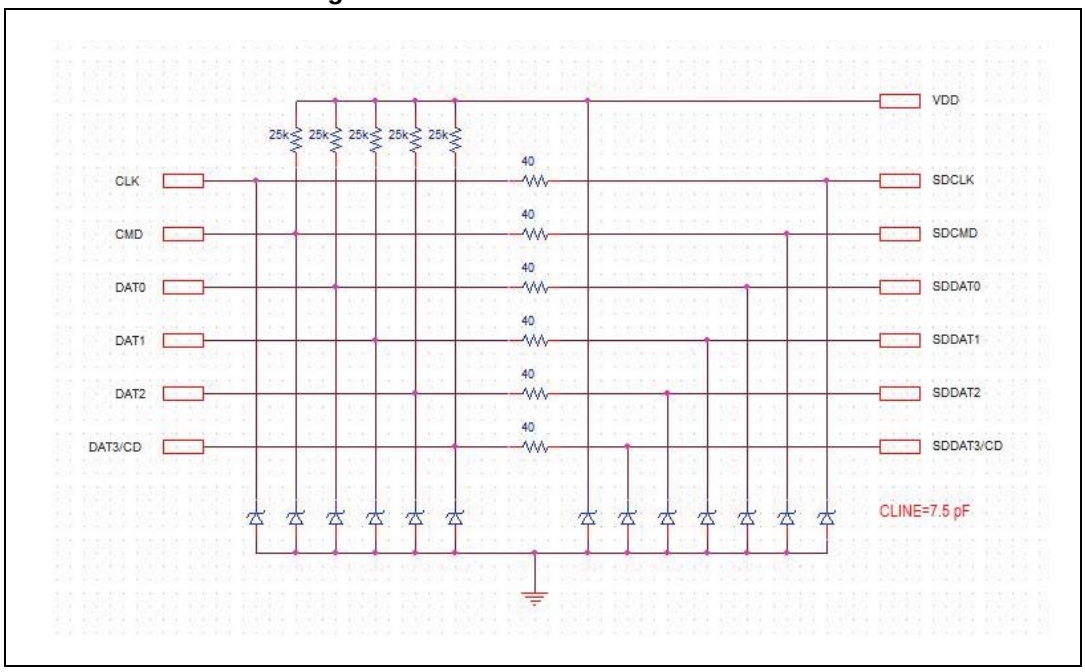
Figure 4. Negative surge



The Host driving the memory card is physically isolated (due to the timing constraints) from the card connector, which is thus exposed to potential ESD damage.

The EMIF06-MSD04F3 provides protection for the six SD card data and clock lines, while a single TVS protects the V_{DD} line (*Figure 5*).

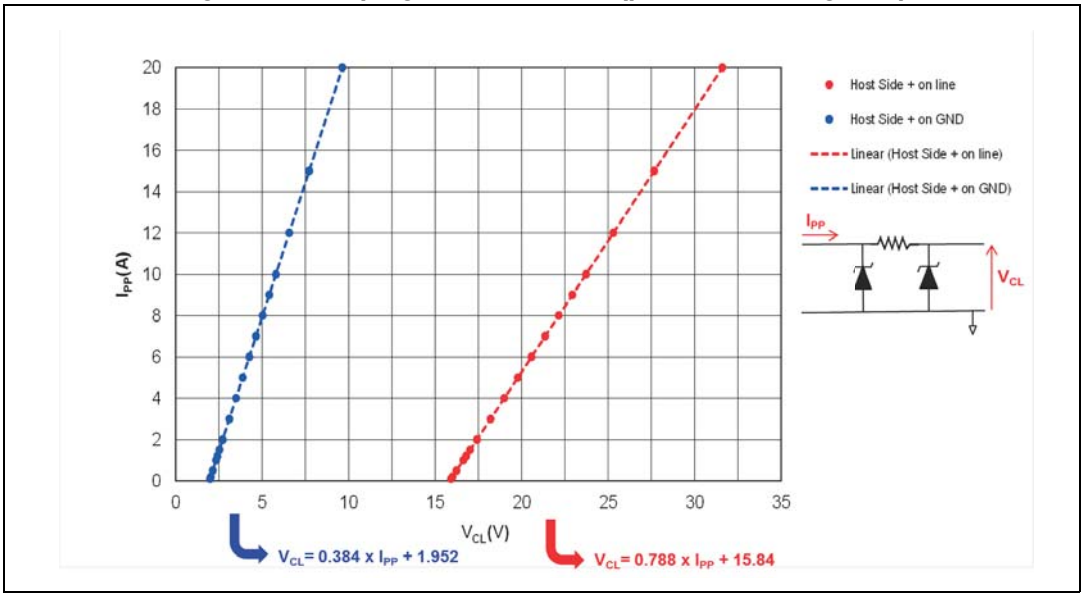
Figure 5. EMIF06-MSD04F3 schematic



3 EMIF06-MSD04F3 clamping characteristics

The clamping characteristic is measured as described in the application note AN4022, with short triangular pulse $t_P \leq 100$ ns. The results are shown in *Figure 6*.

Figure 6. Clamping characteristics (positive and negative)



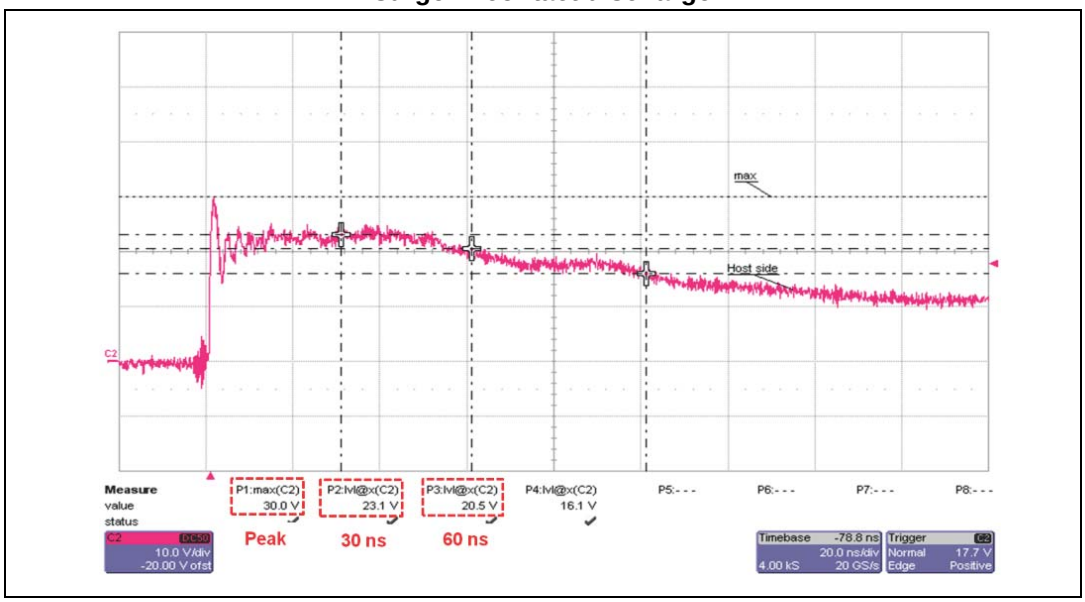
These formulas can be used to calculate the remaining voltages at the host input. *Table 1* shows the values for an 8 kV pulse IEC61000-4-2 (level 4, contact discharge).

Table 1. Calculated clamping voltage at host input for a ±8 kV IEC61000-4-2 ESD surge

V_{PP} = ±8 kV	V_{CL} (V)	
	Positive	Negative
I_{PP} = 16 A (t = 30 ns)	28.4	8.1
I_{PP} = 8 A (t = 60 ns)	22.0	5.0

Figure 7 shows the measured clamping voltages when an 8 kV surge is applied on a data line.

Figure 7. Measured clamping voltage at host input for a +8 kV IEC61000-4-2 ESD surge in contact discharge



Note: Calculated values (*Table 1*) are close to the measured values (*Figure 7*) and the same evaluation can be made in negative.

Comparing the current waveform flowing through the protected host in *Figure 8* with *Figure 9*, with both waveforms with and without the protection device, the current level is much lower.

Note than the impedance load is equal to 5 Ω.

Figure 8. Measured current through the host for an +8 kV IEC61000-4-2 ESD surge, with EMIF06-MSD04F3

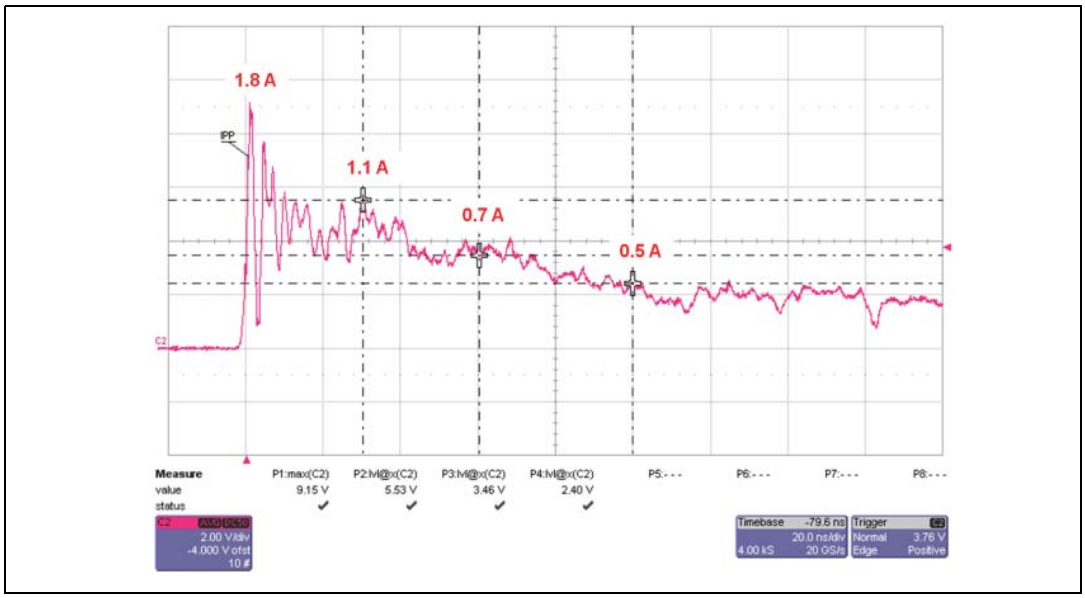
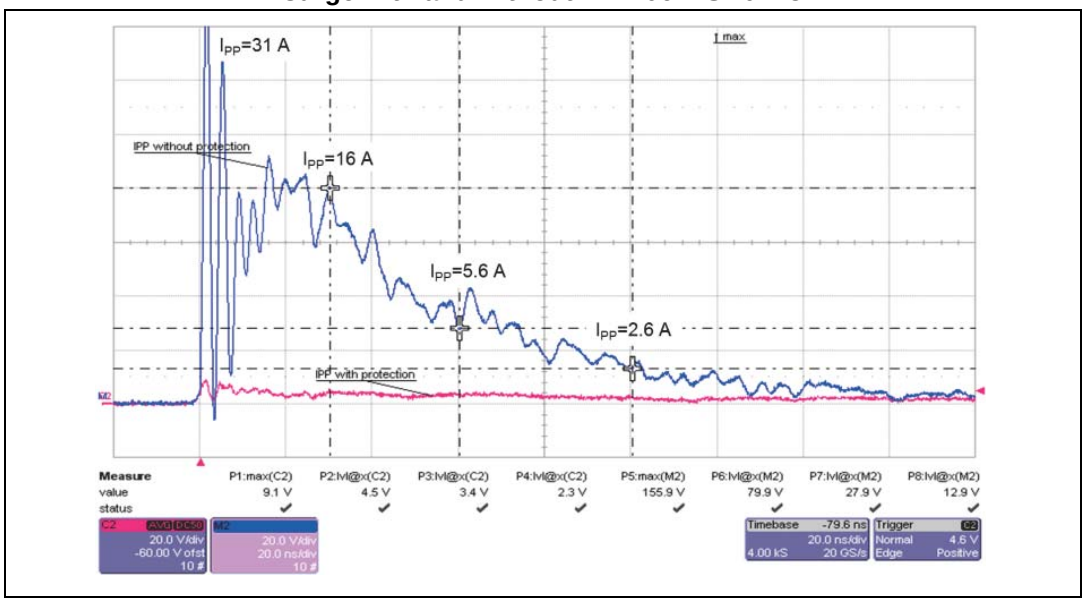


Figure 9. Comparison of the current through the host for an +8 kV IEC61000-4-2 ESD surge with and without EMIF06-MSD04F3



The EMIF06-MSD04F3 is compliant with IEC61000-4-2 level 4 for external lines and level 2 for internal lines.

To maximize the effectiveness of the protection device:

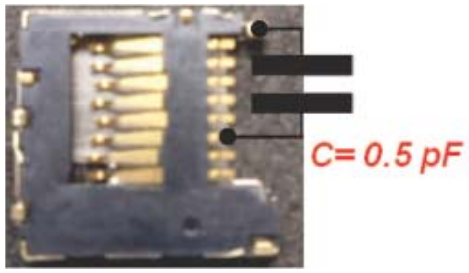
- place it as close as possible to the SD card connector (to shunt the surge as close as possible to its source)
- minimize the return to the ground inductance
- if possible, place the vias between the different ground planes of the PCB

4 SD3.0 constrains

As the SD standard requires that data lines are pulled-up to V_{DD}, the STMicroelectronics EMIF devices include pull-up resistors on each line (*Figure 1*). The standard specifies 10 kΩ ≤ $R_{PULL-UP}$ ≤ 100 kΩ (90 kΩ for R_{DAT3}).

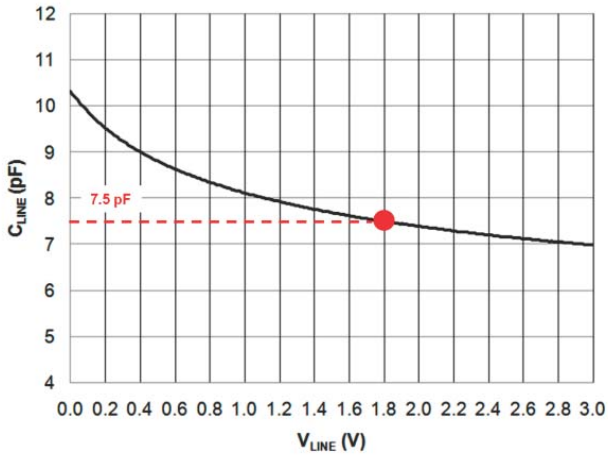
One of the main issues for UHS-I compliance is to manage the capacitance budget of the link host-card. The recommended approximate value is 21 pF (Physical Layer specification, table 6-12, page 159), including the SD card capacitance that is assumed to be equal to 10 pF maximum. Therefore, only 11 pF remain for the printed circuit board, the SD card connector and the protection. The typical capacitance of a µSD card connector is measured at 0.5 pF (*Figure 10*).

Figure 10. Connector parasitic capacitance



The line capacitance of the EMIF devices is 7.5 pF for 1.8 V signaling (*Figure 11*).

Figure 11. Connector parasitic capacitance



The C_{BUS} capacitance must therefore be around 3 pF.

These values are critical for obtaining the highest SD card bit rate specifications, currently around 95 MB/s in read mode and 90 MB/s in write mode for SDXC card types.

The rise and fall times specified by the standard are less than 0.96 ns and the maximum clock frequency is 208 MHz.

Figure 12 shows the test setup used to perform the different time measurements on the SD link. A High-speed card reader working on USB3.0 is connected to a PC.

Figure 12. SD3.0 link test setup

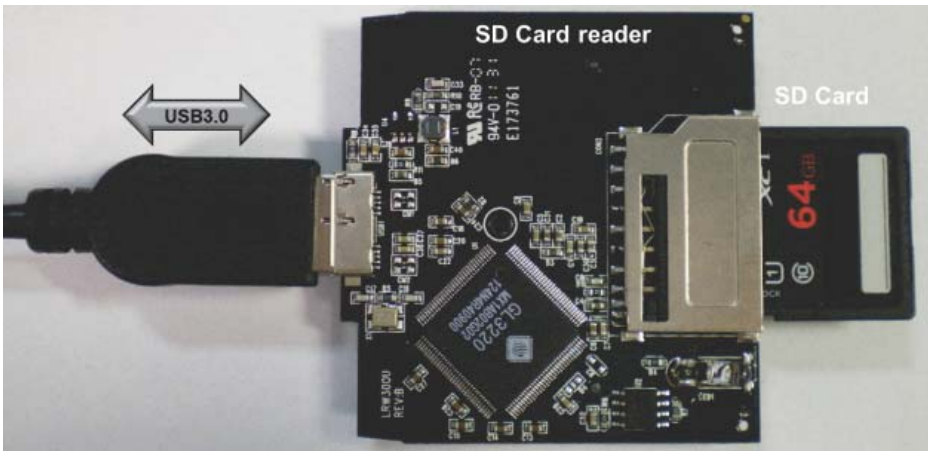
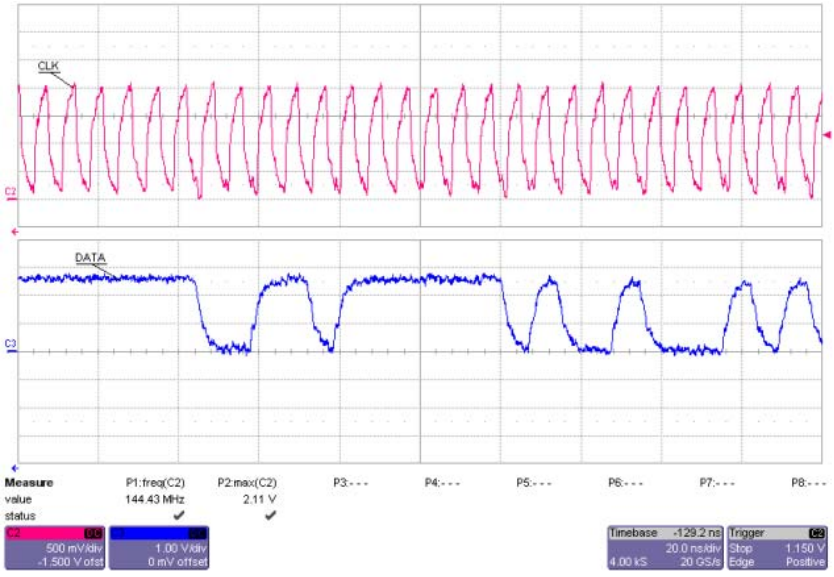


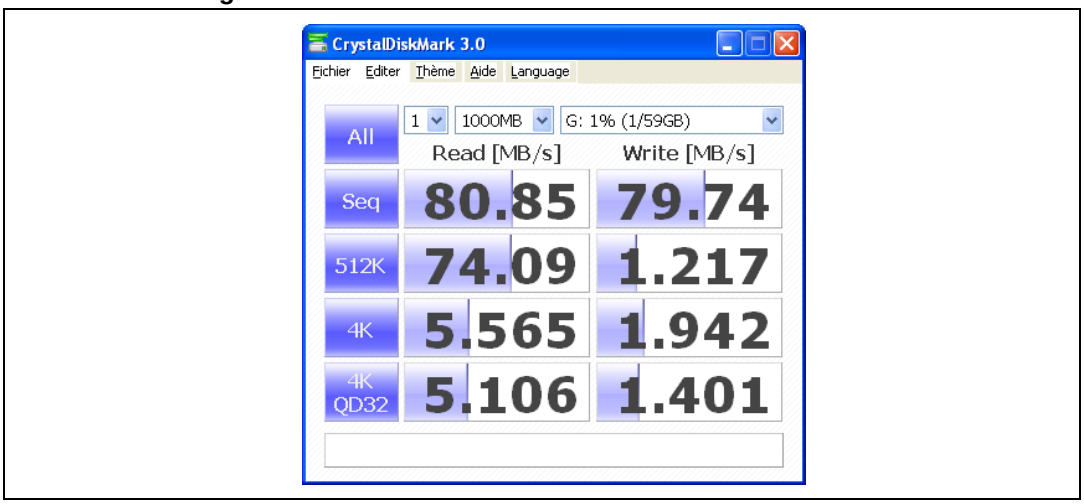
Figure 13 shows the waveforms obtained on the clock line and one data line between the Host and SD card for a class-10, speed-grade-1 SDXC device.

Figure 13. Clock and data signals on a SD3.0 link



The 201 MHz clock frequency is close to the maximum specified frequency. Data rate evaluation is shown in *Figure 14*.

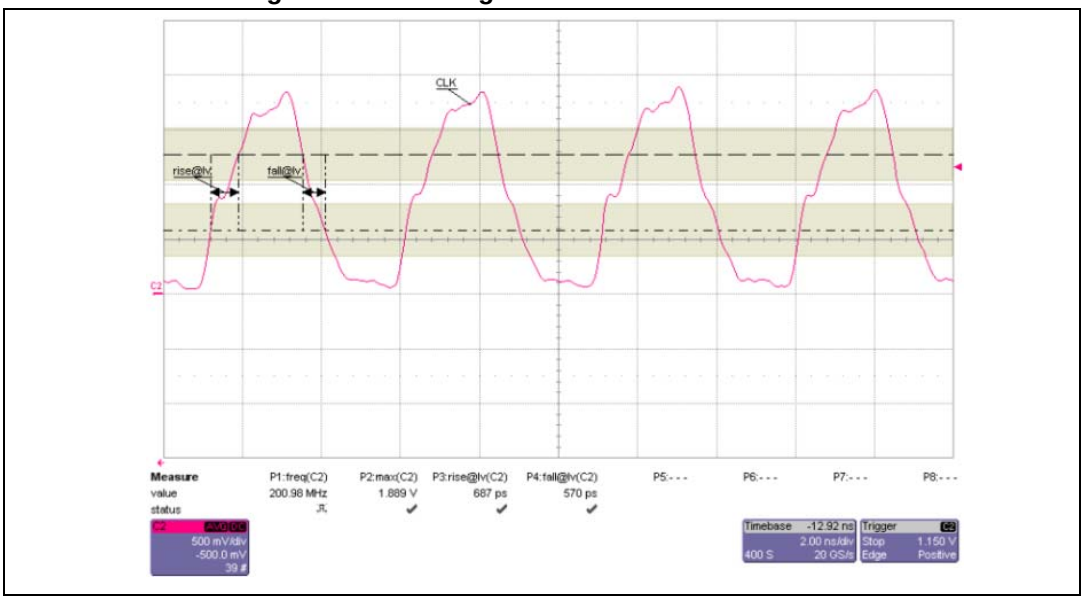
Figure 14. Data rate evaluation on the SD3.0 tested link



The approximate 80 MB/s data rate in read and write mode is close to the specified value.

Figure 15 shows the clock signal for measuring the rise and fall times. t_R and t_F are measured between 0.58 V and 1.27 V (V_{IL} max and V_{IH} min corresponding to V_{DD} supply voltage): t_R and t_F are lower than 0.96 ns, the specified maximum value in the SD3.0 standard.

Figure 15. Clock signal on the SD3.0 tested link



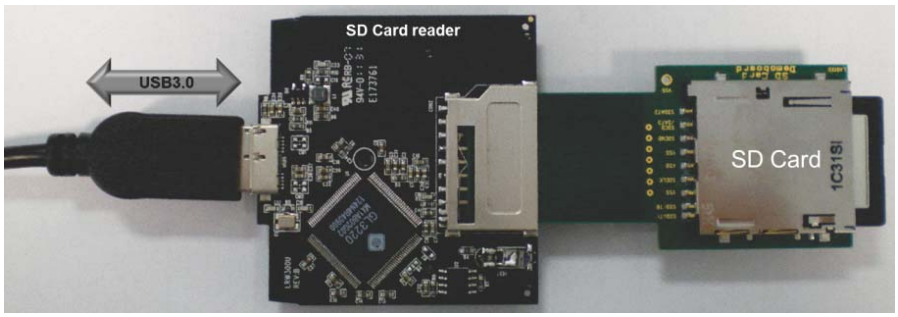
To facilitate the testing of the protection device, an interface board is inserted between the card and the host (*Figure 16*).

Figure 16. SD card demo board for EMIF06-MSD03/04F3



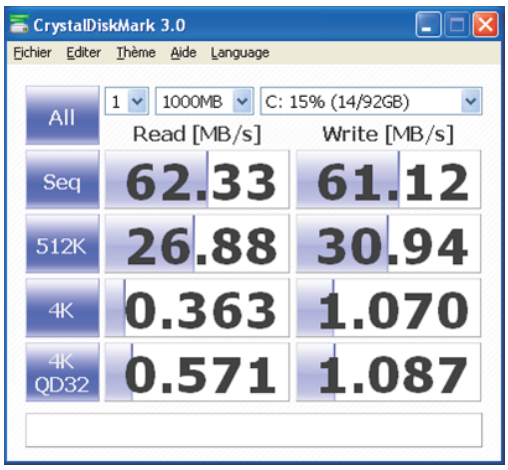
This demo board is inserted in the SD card reader (*Figure 17*).

Figure 17. EMIF06-MSD03/04F3 SD3.0 test setup



While this allows probing of the different signals between the host, the filter and the SD card, the drawback is that parasitic capacitance and inductance increase. The impact of the device under test on the bit rate of the link can be evaluated by shortening the device on the demonstration board; the PCB thus becoming a "through" device. The bit rate results for these conditions are shown in *Figure 18*.

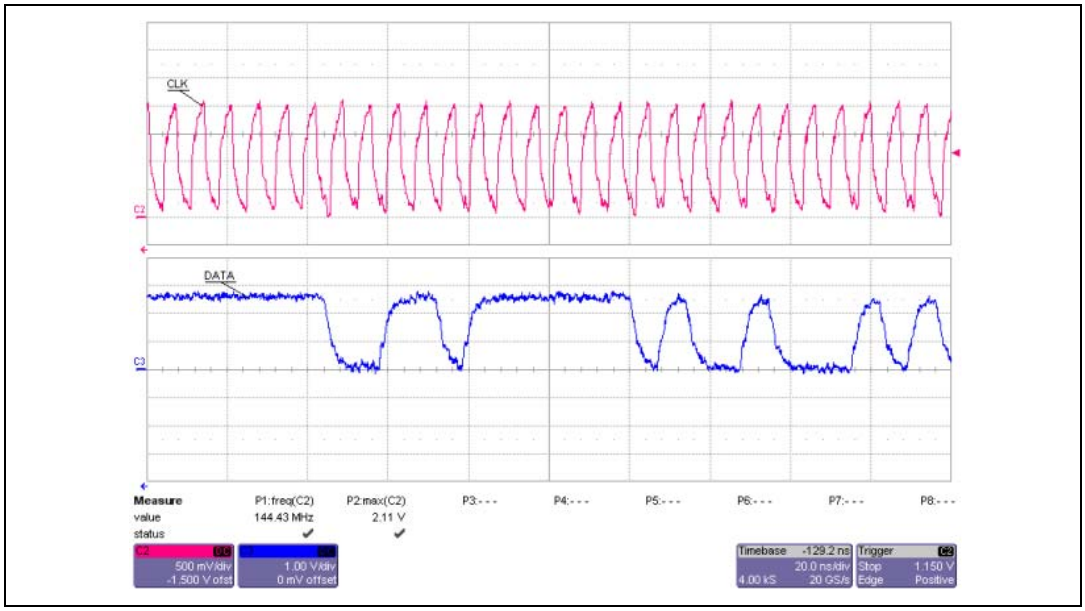
Figure 18. Data rate evaluation with demo board without EMIF06-MSD04F3



The data rate decreases from 80.8-79.7 MB/s to 62.3-61.2 MB/s.

By inserting the demo board with the EMIF06-MSD04F3, the same test as in*Figure 14* is performed to obtain the new waveforms in*Figure 19*.

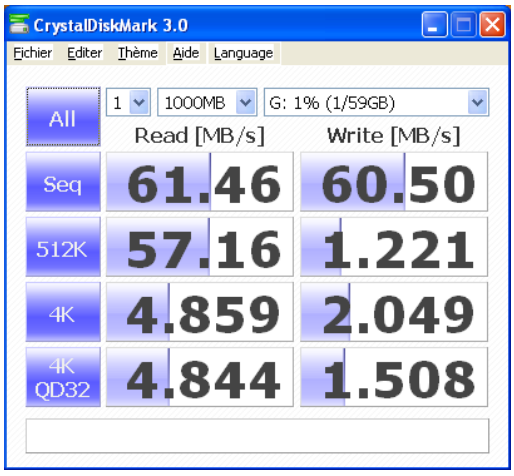
Figure 19. Clock and data signals on an SD3.0 link with EMIF06-MSD04F3 and its demo PCB



The transmission performs well and the clock frequency decreases to 145 MHz due to the added capacitance $C_{LINE}=C_{PCB}+C_{EMIF}$.

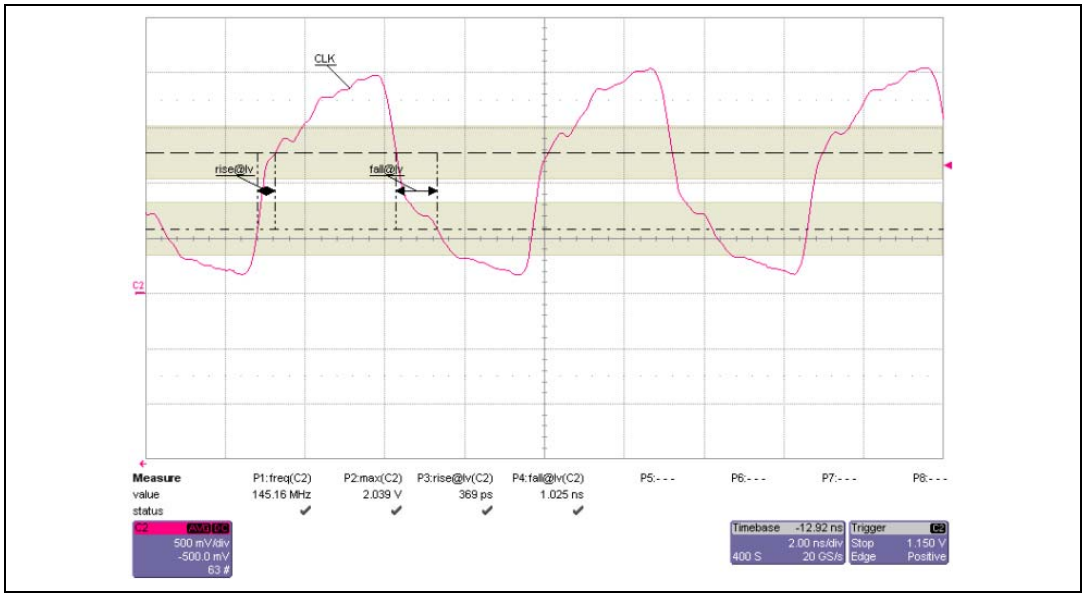
The data rate results are given in *Figure 20*.

Figure 20. Data rate evaluation on the SD3.0 tested link with EMIF06-MSD04F3 and its demo PCB



The clock signal waveform is shown in *Figure 21*.

Figure 21. Clock signal on the SD3.0 tested link with EMIF06-MSD04F3 and its demo PCB

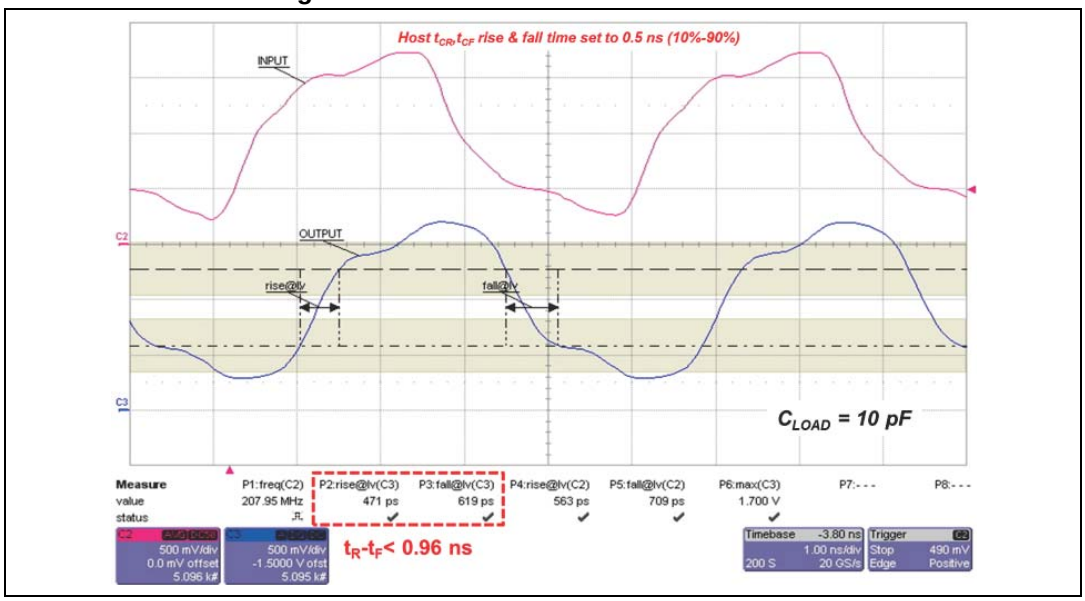


The characteristics of the Host are adapted to ensure the system obtains the best balance, even if the added filter does not impact the link greatly: the data rate only decreases from 62.3-61.1 MB/s to 61.4-60.5 MB/s.

We can therefore conclude that the filter alone between the host and the card can maintain the maximum capacitance value of the link below the maximum recommended value, which in turn guarantees the maximum data rate of the card.

The EMIF06-MSD04F3, loaded with 10 pF (capacitance equivalent to the SD card) and driven by a pulse generator having a 50 Ω line impedance, outputs the waveforms shown in *Figure 22*. Its shows that rise and fall times are in accordance with the SD3.0 standard.

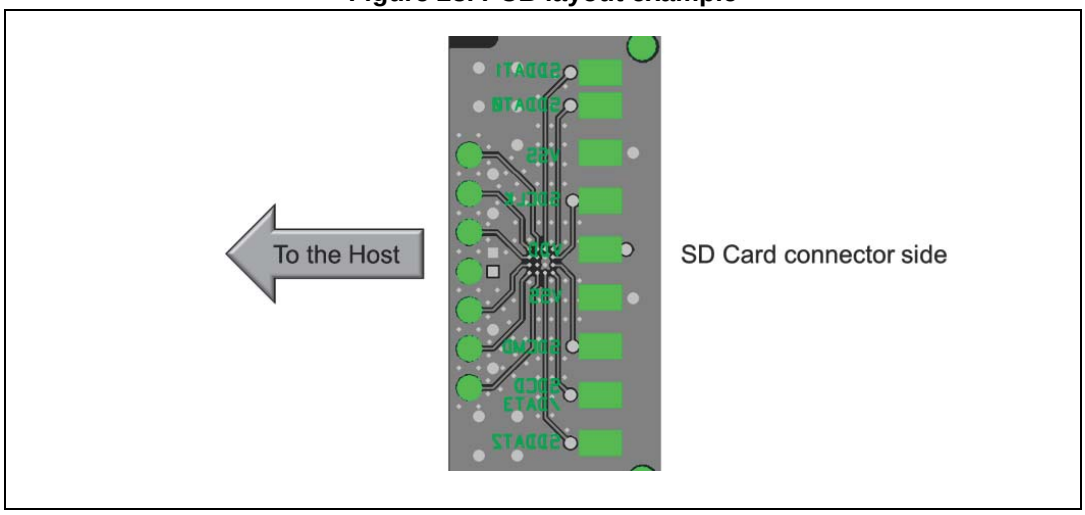
Figure 22. EMIF06-MSD04F3 at F= 208 MHz



Minimizing the parasitic between host and card is a key point, and the SD3.0 standard specifies a maximum inductance of 16 nH in the link.

An example of PCB layout is shown in *Figure 23*.

Figure 23. PCB layout example



It is also important that the data and clock signals arrive simultaneously at the host/card inputs for the read/write timing to be taken into account. The design symmetry of the EMIF06-MSD04F3 allows this and the skew between the different lines is less than 20 ps. Note than the transmission speed on a standard PCB is around 7 ps/mm.

5 Rejection capability

The data and clock frequency used in this link can cause high frequency noise and corresponding harmonics to radiate and disturb other subsystems, especially in the RX part of the phone. This can induce antenna desense which can cause calls to drop or high BER.

EMIF06-MSD04F3 introduces attenuation in the RX frequency range higher than -12 dB, limiting these risks. A rejection simulation schematic for a typical layout is shown in *Figure 24* and the filter frequency response is given in *Figure 25*.

Figure 24. Rejection simulation schematic

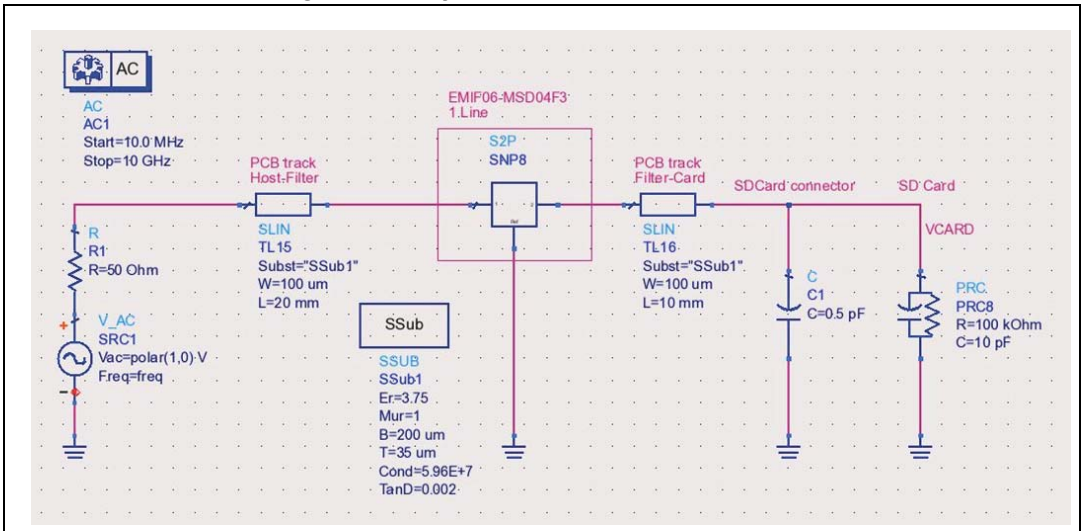
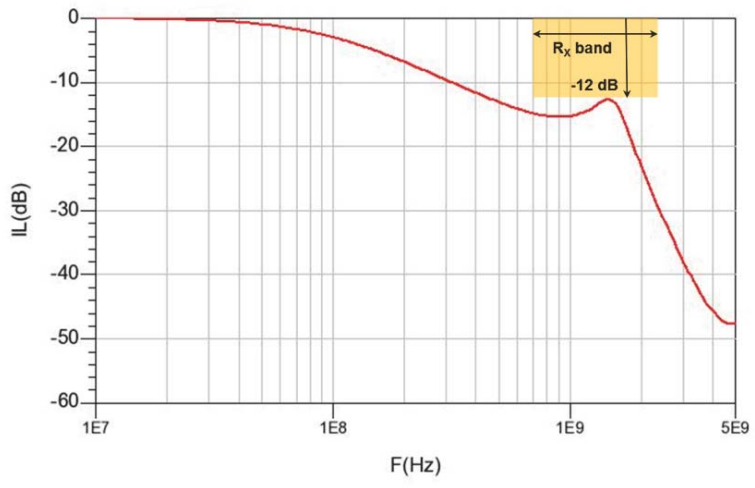
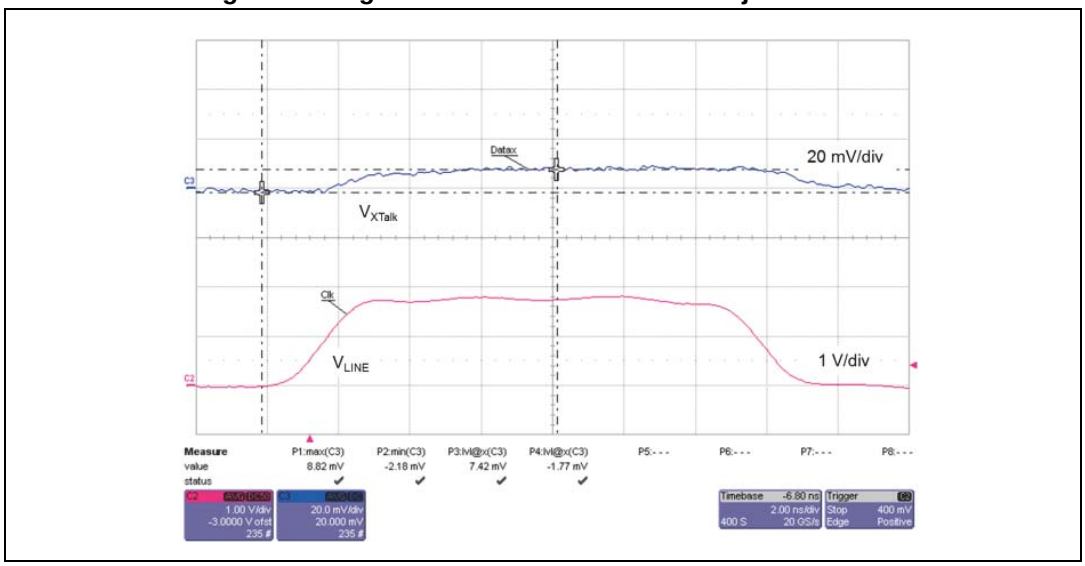


Figure 25. Filter attenuation versus frequency



Crosstalk between two adjacent lines may also be an issue. This parameter is also specified, and *Figure 26* demonstrates that the noise generated, for example, by the clock on a data line is negligible.

Figure 26. Digital crosstalk between two adjacent lines



6 Card detection

Mechanical or electrical card detection can be implemented.

The EMIF06-MSD03F3 device can be chosen for applications requiring electrical card detection. This filter has the same electrical characteristics as the EMIF06-MSD04F3, but the CD/Dat3 pin is disconnected from the V_{DD} host side (*Figure 5*). After the power-up, this pin is connected to V_{DD} through the internal 50 kΩ pull-up resistor of the SD card; the host can drive a pull-down resistor (typically 470 kΩ) connected to this pin and detect the logic level change, specifically, card insertion. After this sequence, the internal 50 kΩ resistor must be disconnected by the SET_CLR_CARD_DETECT command (ACMD42).

7 Conclusion

STMicroelectronics EMIF devices include protection and filtering functions for SD card Ultra High Speed applications.

Their electrical characteristics have been optimized to guarantee low clamping voltages in order to protect the host driver, often exposed to ESD surges during card insertion and removal.

Through careful PCB layout, it is possible to obtain the highest data rate transmission allowable on the new SD3.01-compliant µSD or SD cards used by many portable devices.

The filtering capabilities of the EMIF devices can help the designer to limit the noise generated during the read and write operations and improve EMI robustness, especially on devices such as phones or tablets, which are particularly exposed to this issue.

8 Revision history

Table 2. Document revision history

Date	Revision	Changes
05-Dec-2014	1	Initial release.

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