0.5A DUAL CHANNEL CURRENT-LIMITED POWER SWITCH

Description

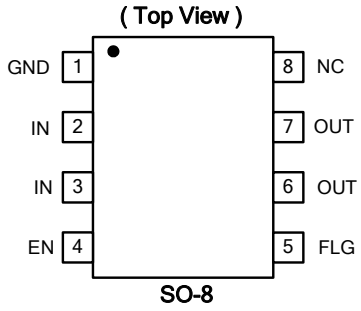
The AP2142 and AP2152 are integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB 2.0 and available with both polarities of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

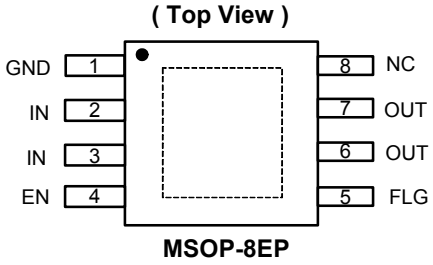
All devices are available in SO-8 and MSOP-8EP packages.

Features

- Dual USB port power switches
- Over-current and thermal protection
- 0.8A accurate current limiting
- Reverse Current Blocking
- 115mΩ on-resistance
- Input voltage range: 2.7V – 5.5V
- 0.6ms typical rise time
- Very low shutdown current: 1uA (max)
- Fault report (FLG) with blanking time (7ms typ)
- ESD protection: 4.5KV HBM, 350V MM
- Active high (AP2152) or active low (AP2142) enable
- Ambient temperature range -40ºC to 85°C
- SO-8 and MSOP-8EP (Exposed Pad): Available in "Green" Molding Compound (No Br, Sb)
  - **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. "Green" Device (Note 3)**
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

Pin Assignments





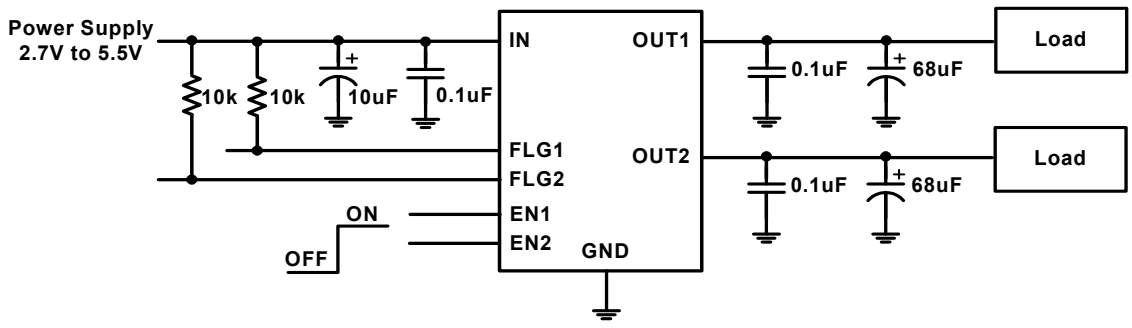
Applications

- Consumer electronics – LCD TV & Monitor, Game Machines
- Communications – Set-Top-Box, GPS, Smartphone
- Computing – Laptop, Desktop, Servers, Printers, Docking Station, HUB

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

AP2152 Enable Active High



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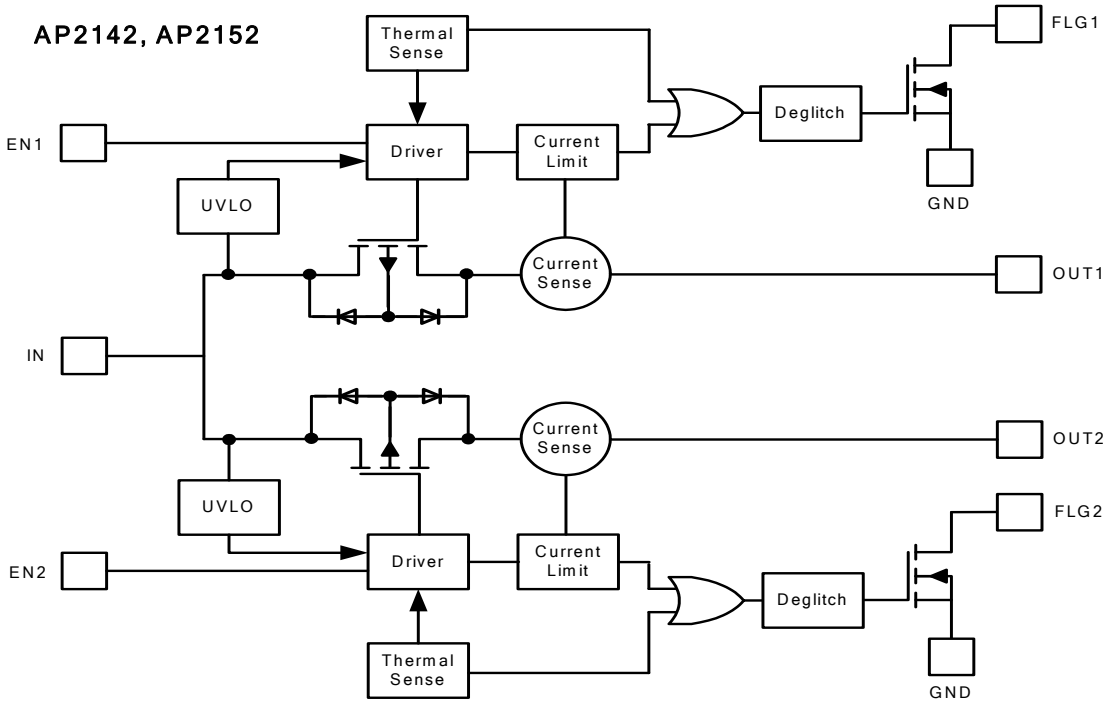
Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (typ)	Recommended Maximum Continuous Load Current
AP2142	2	Active Low	0.8A	0.5A
AP2152	2	Active High	0.8A	0.5A

Pin Descriptions

Pin Name	Pin Number		Function
	SO-8	MSOP-8EP	
GND	1	1	Ground
IN	2	2	Voltage input pin
EN1	3	3	Switch 1 enable input, active low (AP2142) or active high (AP2152)
EN2	4	4	Switch 2 enable input, active low (AP2142) or active high (AP2152)
FLG2	5	5	Switch 2 over-current and over-temperature fault report; open-drain flag is active low when triggered
OUT2	6	6	Switch 2 voltage output pin
OUT1	7	7	Switch 1 voltage output pin
FLG1	8	8	Switch 1 over-current and over-temperature fault report; open-drain flag is active low when triggered
Exposed Tab	—	Exposed Tab	Exposed pad. It should be connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path.

Functional Block Diagram



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Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3	kV
ESD MM	Machine Model ESD Protection	300	V
V_{IN}	Input Voltage	6.5	V
V_{OUT}	Output Voltage	V_{IN} + 0.3	V
V_{EN} , V_{FLG}	Enable Voltage	6.5	V
I_{LOAD}	Maximum Continuous Load Current	Internal Limited	A
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{ST}	Storage Temperature Range (Note 4)	-65 to 150	°C

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices

Note: 4. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C)

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
V_{IN}	Input voltage	2.7	5.5	V
I_{OUT}	Output Current	0	500	mA
V_{IL}	EN Input Logic Low Voltage	0	0.8	V
V_{IH}	EN Input Logic High Voltage	2	V_{IN}	V
T_A	Operating Ambient Temperature	-40	85	°C

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Electrical Characteristics (@T_A = +25°C, V_{IN} = +5V, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{UVLO}	Input UVLO	R_{LOAD} = 1kΩ		1.6	1.9	2.5	V
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0			0.5	1	μA
I_Q	Input Quiescent Current, Dual	Enabled, I_{OUT} = 0			100	160	μA
I_{LEAK}	Input Leakage Current	Disabled, OUT grounded				1	μA
I_{REV}	Reverse Leakage Current	Disabled, V_{IN} = 0V, V_{OUT} = 5V, I_{REV} at V_{IN}			1		μA
$R_{DS(ON)}$	Switch on-resistance	V_{IN} = 5V, I_{OUT} = 0.5A, -40°C ≤ T_A ≤ +85°C	MSOP-8EP		115	150	mΩ
			SO-8		120	160	mΩ
		V_{IN} = 3.3V, I_{OUT} = 0.5A, -40°C ≤ T_A ≤ 85°C			140	180	mΩ
I_{SHORT}	Short-circuit current limit	Enabled into short circuit, C_L = 68μF			0.6		A
I_{LIMIT}	Over-Load Current Limit	V_{IN} = 5V, V_{OUT} = 4.8V, C_L = 68μF, -40°C ≤ T_A ≤ +85°C		0.6	0.8	1.0	A
I_{Trig}	Current limiting trigger threshold	V_{IN} = V_{EN}, Output Current Slew rate (<100A/WS), C_L = 68μF			1.0		A
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 2.7V to 5.5V				0.8	V
V_{IH}	EN Input Logic High Voltage	V_{IN} = 2.7V to 5.5V		2			V
I_{SINK}	EN Input leakage	V_{EN} = 5V				1	μA
$T_{D(ON)}$	Output turn-on delay time	C_L=1μF, R_{LOAD} = 10Ω			0.05		ms
T_R	Output turn-on rise time	C_L=1μF, R_{LOAD} = 10Ω			0.6	1.5	ms
$T_{D(OFF)}$	Output turn-off delay time	C_L=1μF, R_{LOAD} = 10Ω			0.01		ms
T_F	Output turn-off fall time	C_L=1μF, R_{LOAD} = 10Ω			0.05	0.1	ms
R_{FLG}	FLG output FET on-resistance	I_{FLG} =10mA			30	50	Ω
T_{Blank}	FLG blanking time	C_{IN} =10μF, C_L = 68μF		4	7	15	ms
T_{SHDN}	Thermal shutdown threshold	Enabled, R_{LOAD} = 1kΩ			140		°C
T_{HYS}	Thermal shutdown hysteresis				25		°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-8 (Note 5)			110		°C/W
		MSOP-8EP (Note 6)			60		°C/W

Notes: 5. Test condition for SO-8: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad layout.
6. Test condition for MSOP-8EP: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer ground plane.

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Typical Performance Characteristics

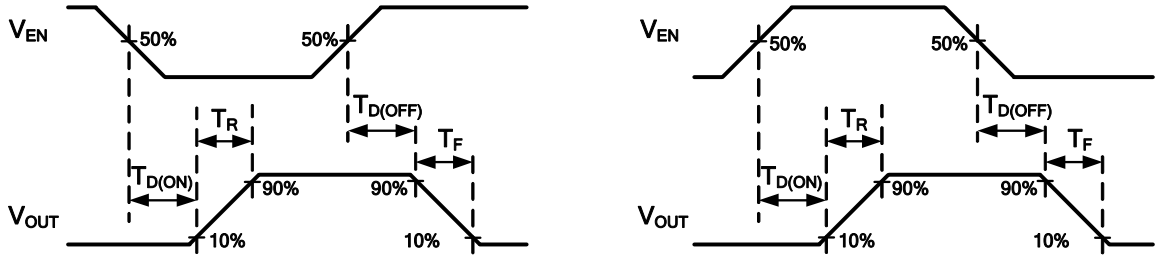
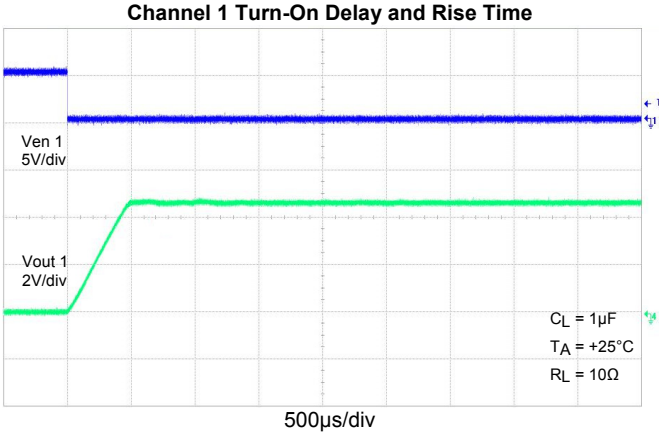


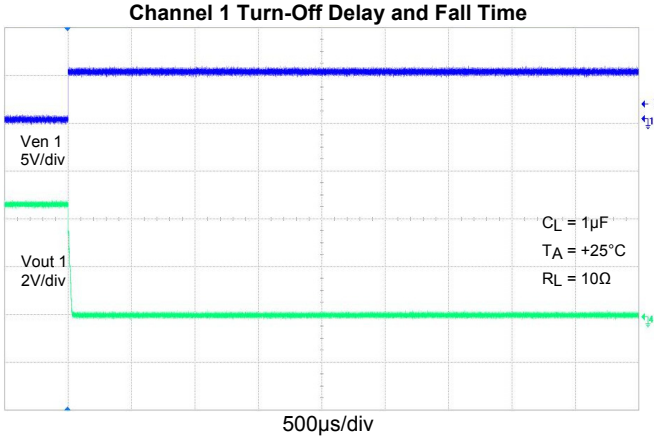
Figure 1. Voltage Waveforms: AP2142 (left), AP2152 (right)

All Enable Plots are for AP2142 Active Low

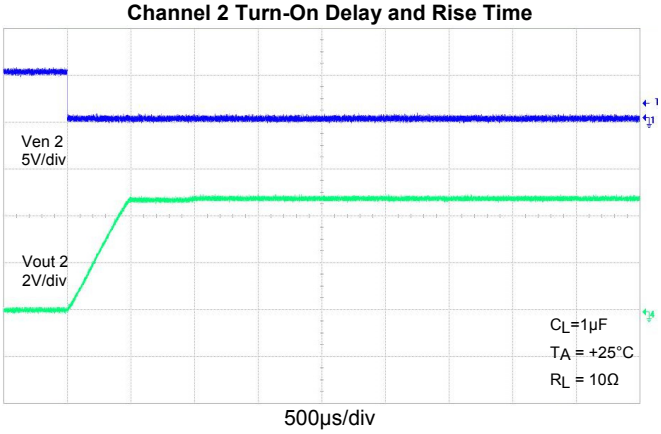
Channel 1 Turn-On Delay and Rise Time



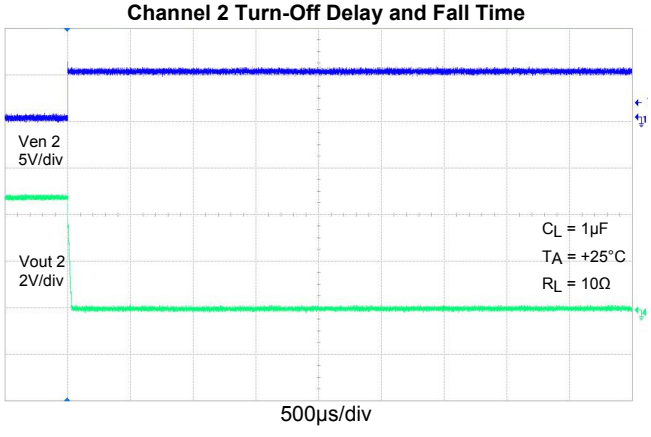
Channel 1 Turn-Off Delay and Fall Time



Channel 2 Turn-On Delay and Rise Time



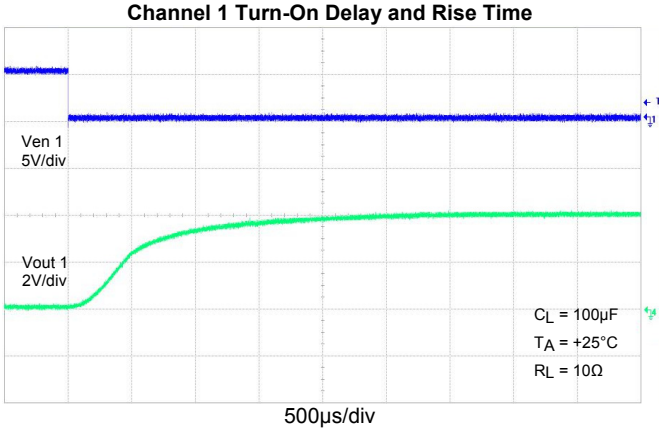
Channel 2 Turn-Off Delay and Fall Time



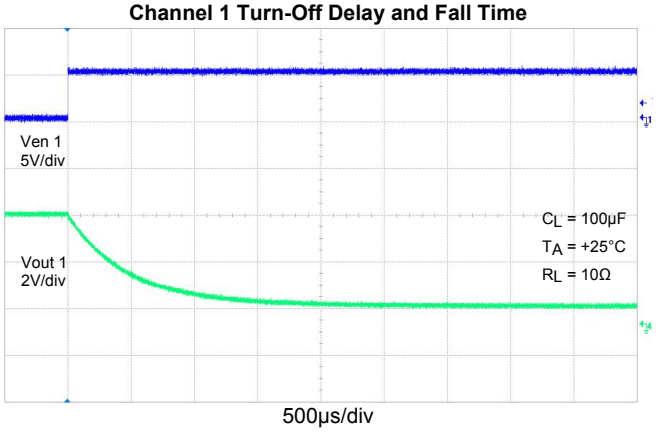
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Typical Performance Characteristics (cont.)

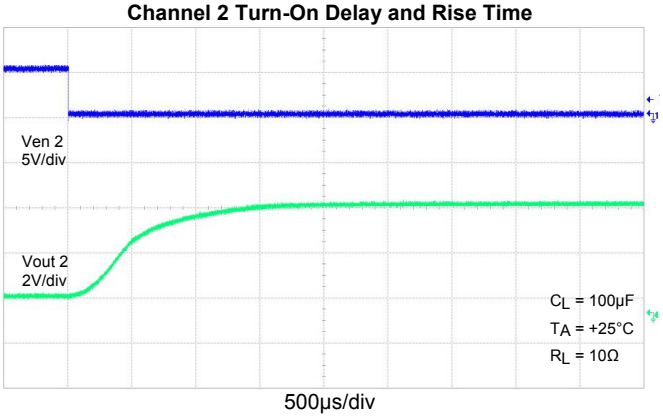
Channel 1 Turn-On Delay and Rise Time



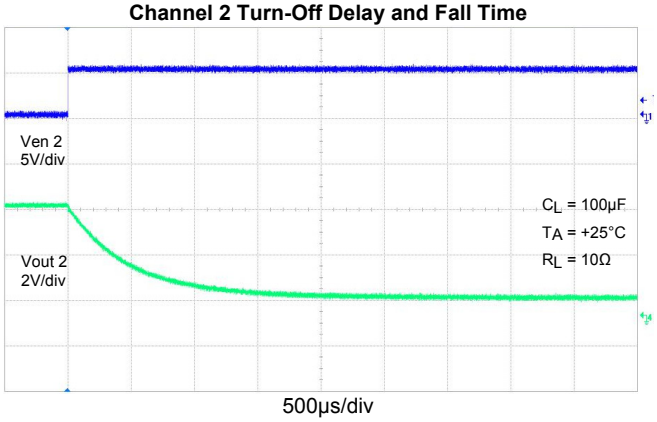
Channel 1 Turn-Off Delay and Fall Time



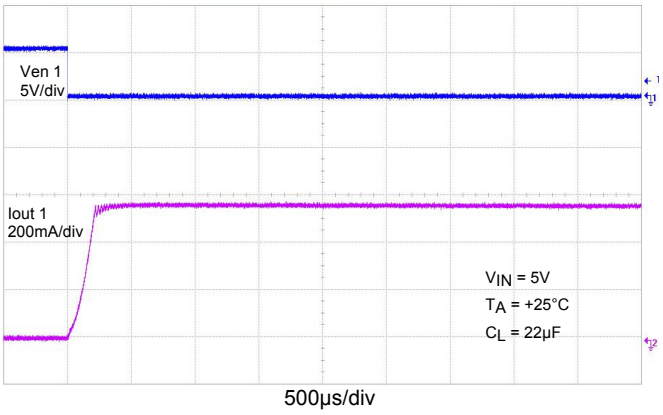
Channel 2 Turn-On Delay and Rise Time



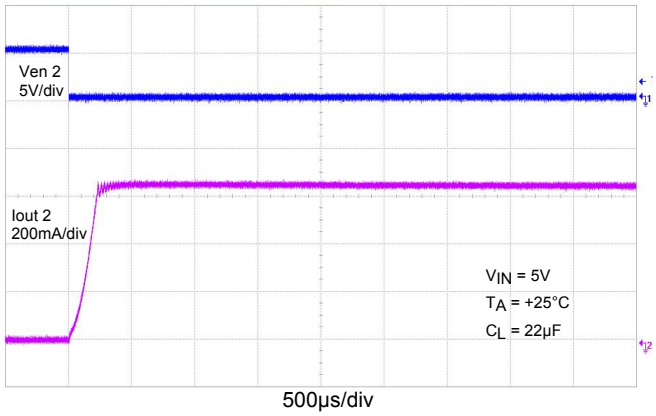
Channel 2 Turn-Off Delay and Fall Time



Channel 1 Short Circuit Current, Device Enabled Into Short



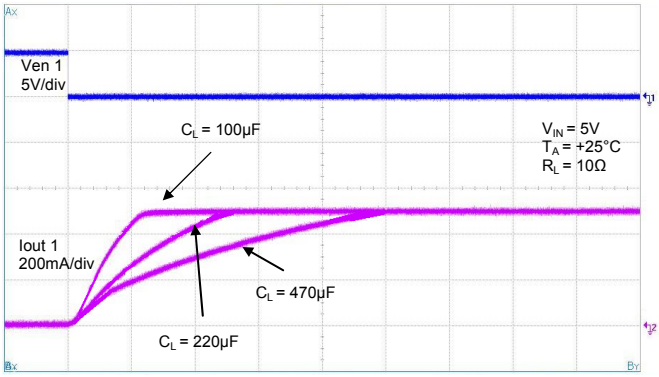
Channel 2 Short Circuit Current, Device Enabled Into Short



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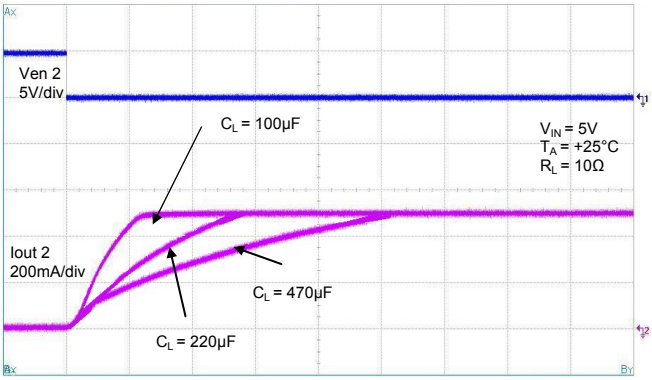
Typical Performance Characteristics (cont.)

Channel 1 Inrush Current



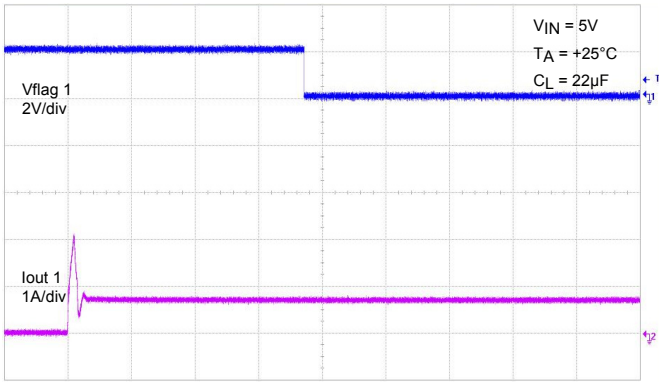
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Channel 2 Inrush Current



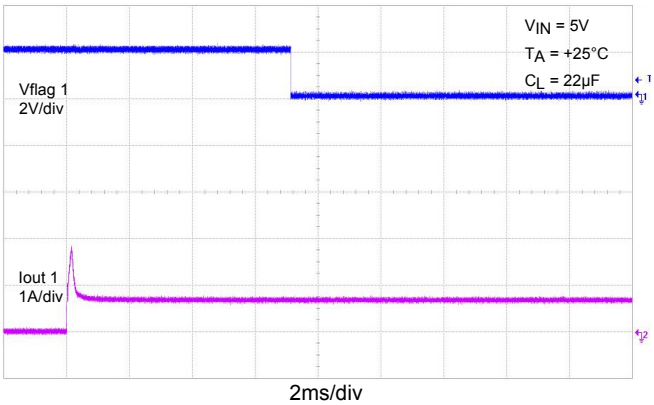
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Channel 1
1 Ω Load Connected to Enabled Device



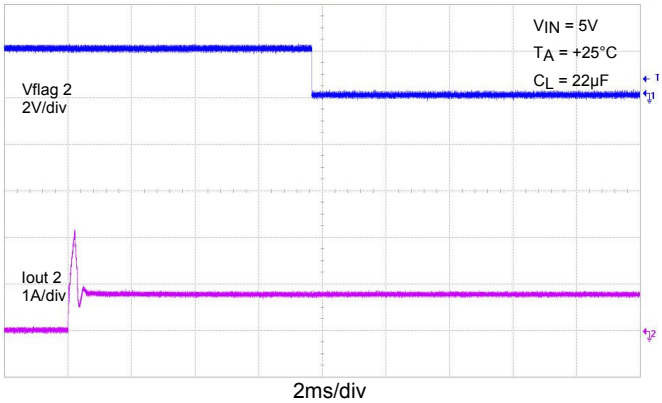
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Channel 1
2Ω Load Connected to Enabled Device



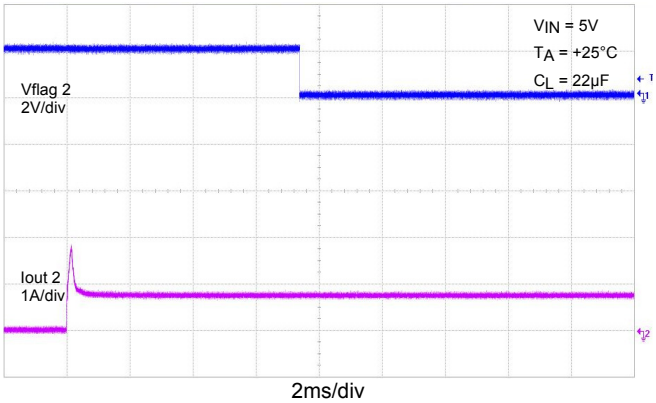
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Channel 2
1 Ω Load Connected to Enabled Device



2ms/div

Channel 2
2Ω Load Connected to Enabled Device

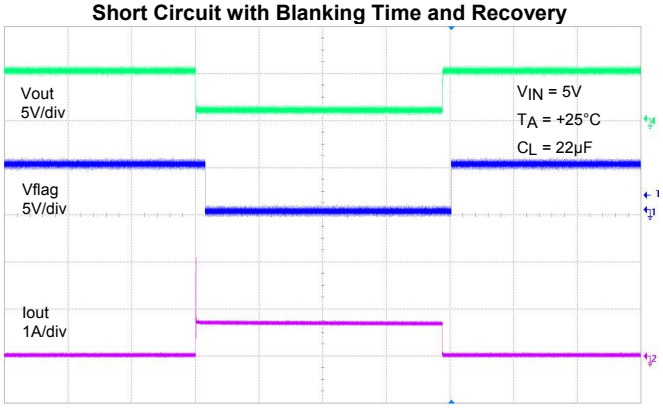


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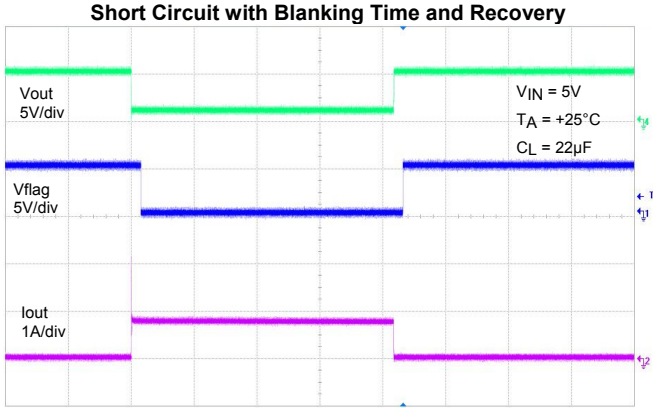
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Typical Performance Characteristics (cont.)

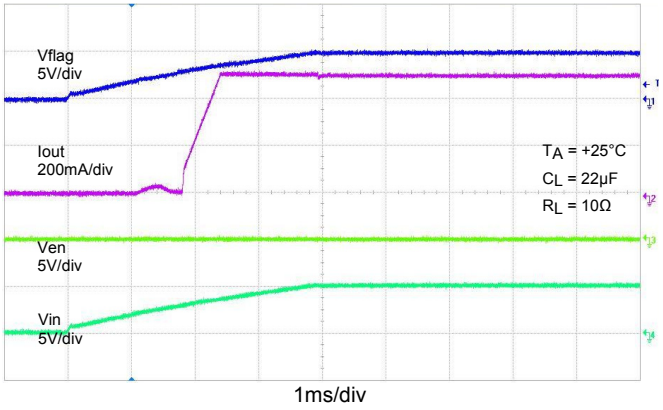
Channel 1
Short Circuit with Blanking Time and Recovery



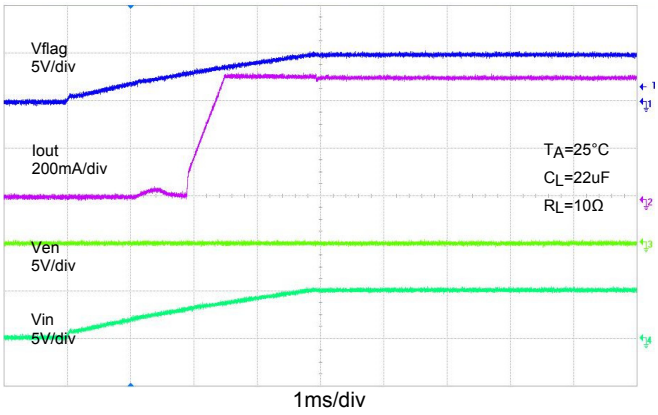
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Short Circuit with Blanking Time and Recovery



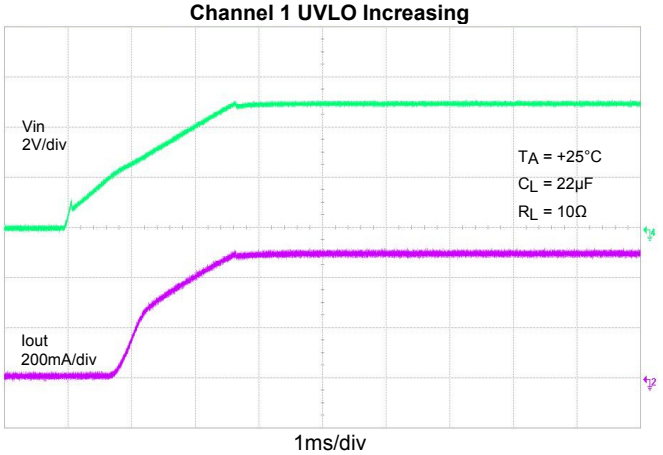
Channel 1 Power On



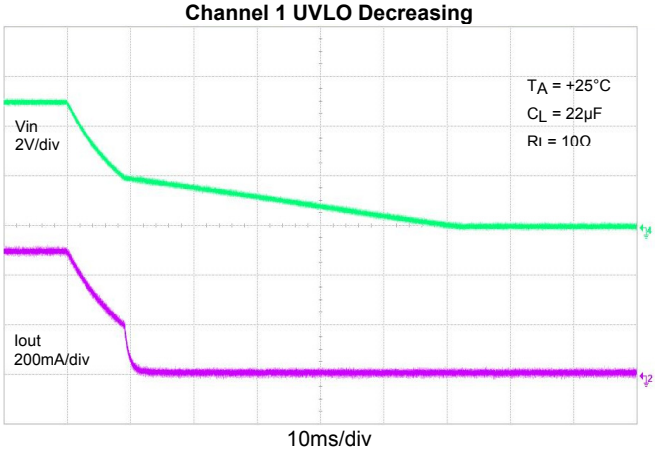
Channel 2 Power On



Channel 1 UVLO Increasing



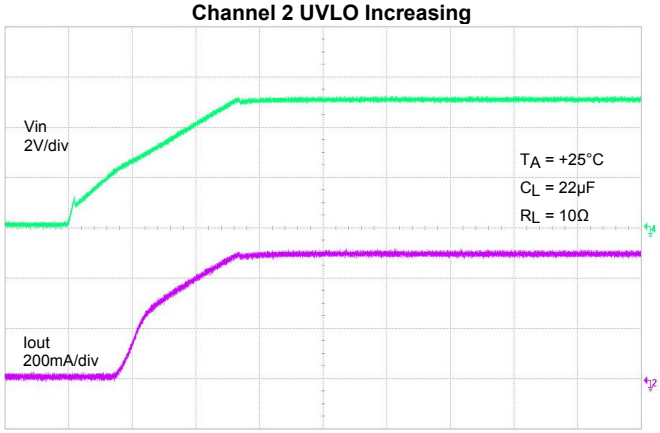
Channel 1 UVLO Decreasing



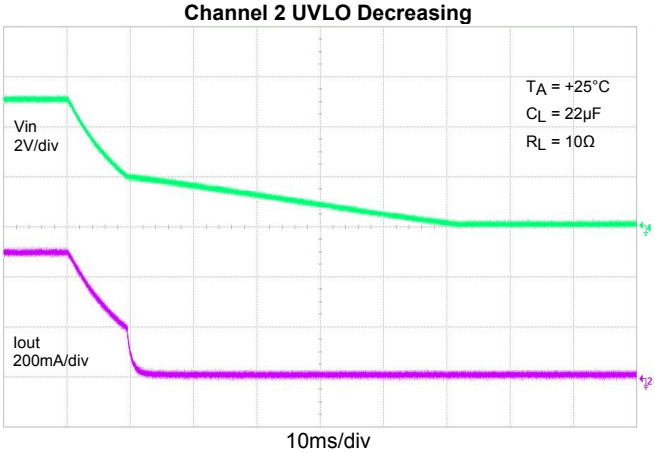
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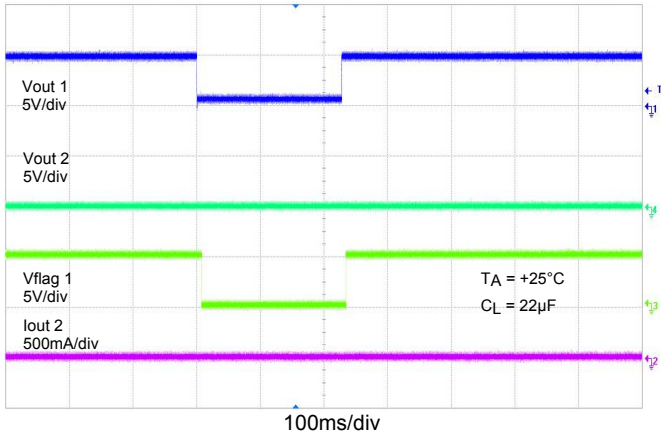
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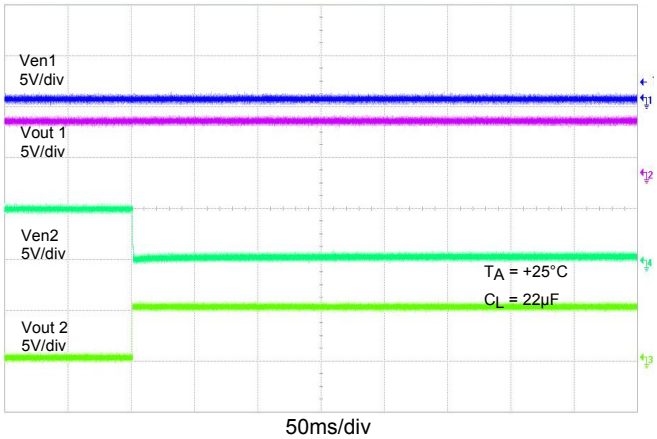
Channel 2 UVLO Decreasing



Channel 1 Enabled and Shorted with Channel 2 Disabled

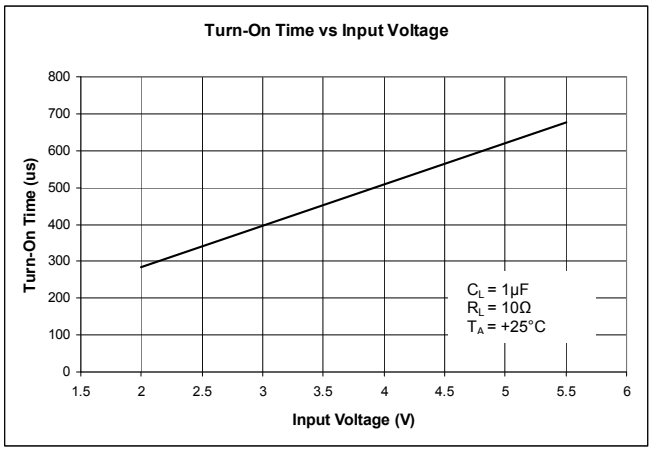


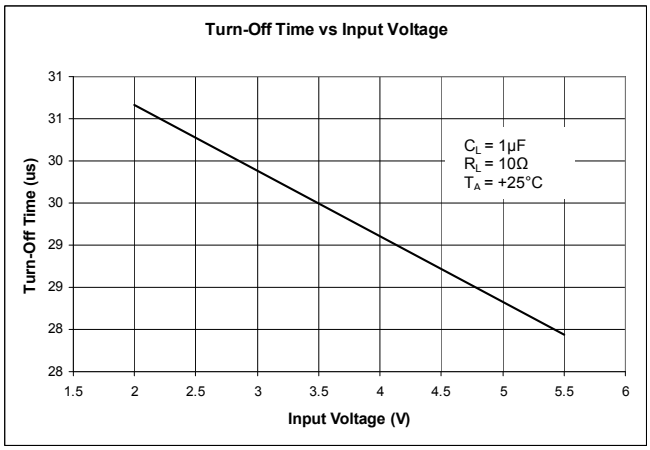
Channel 1 Disabled and Channel 2 Enabled

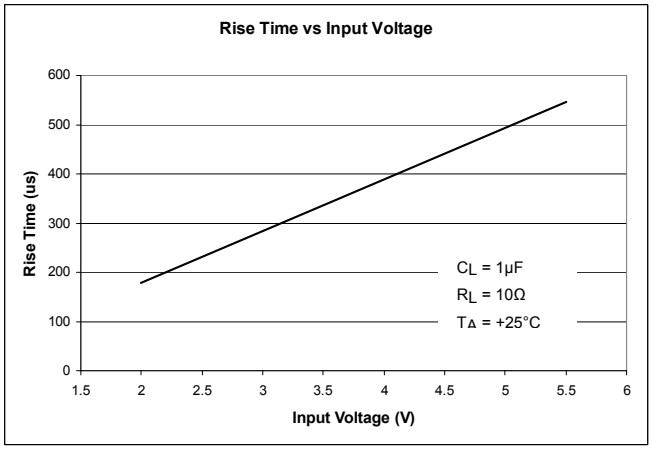


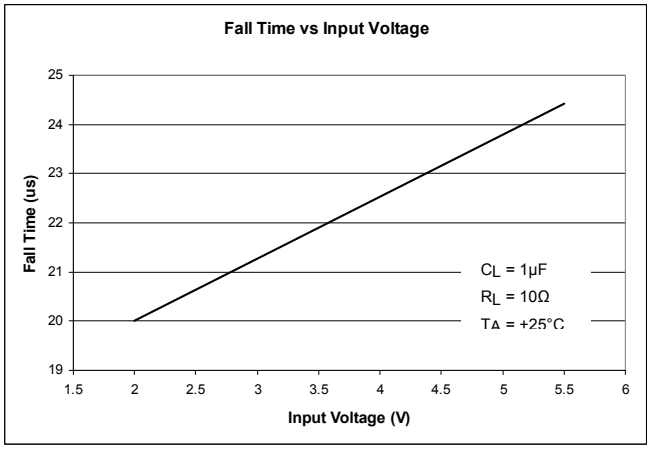
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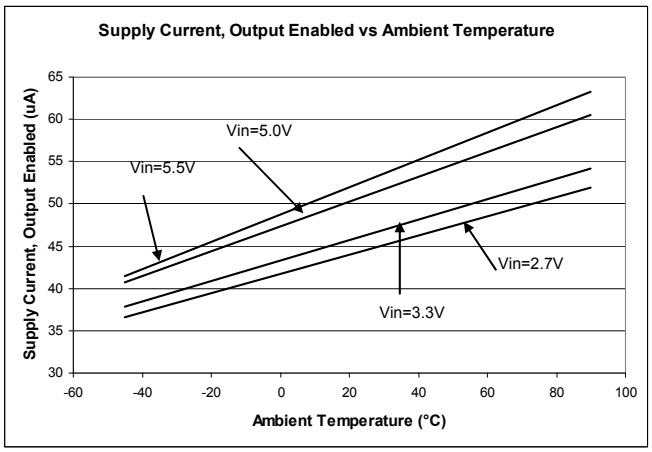
Typical Performance Characteristics (cont.)

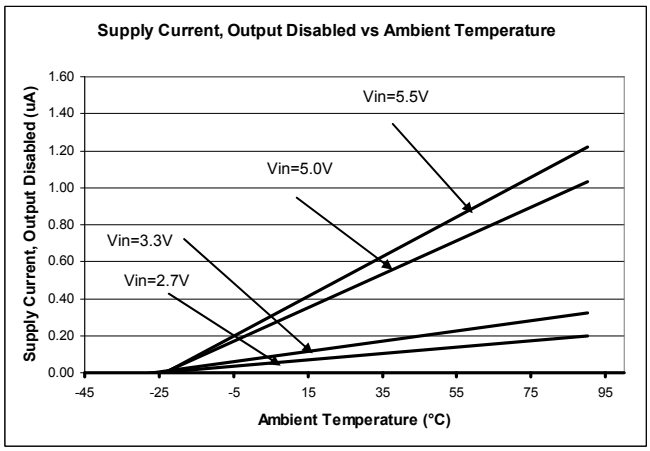






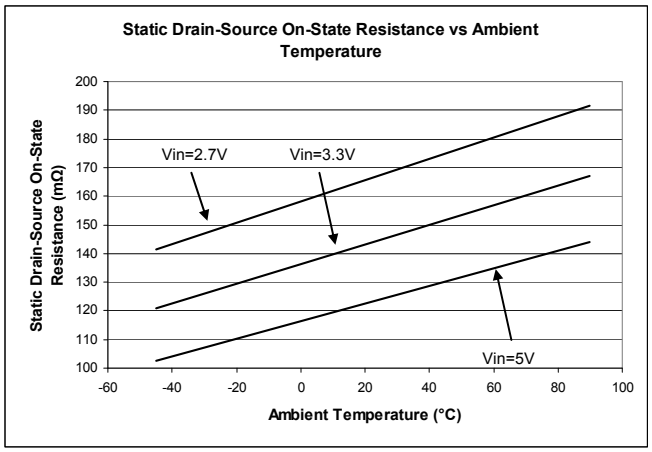


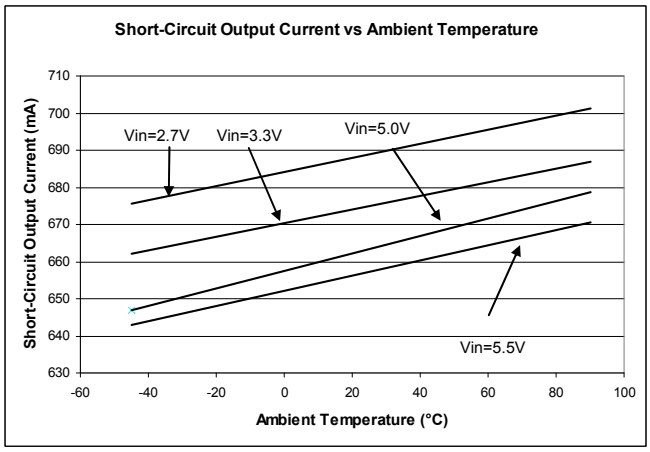


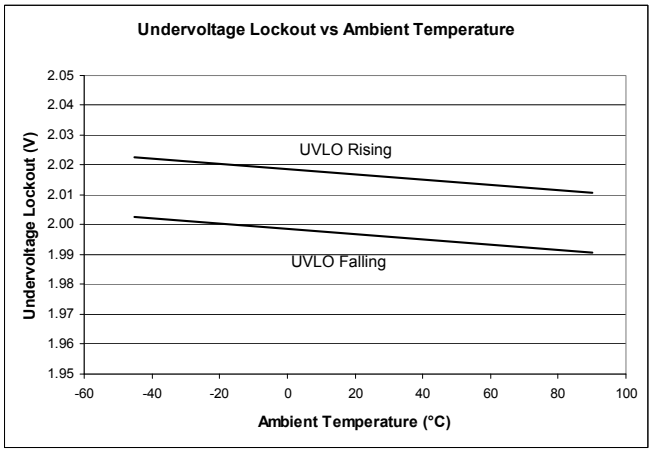


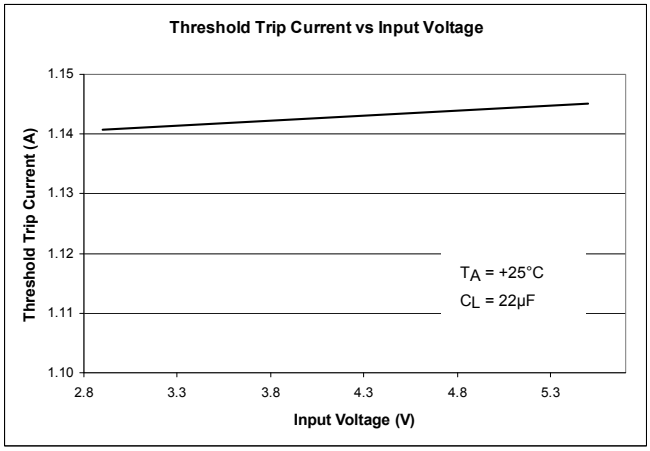
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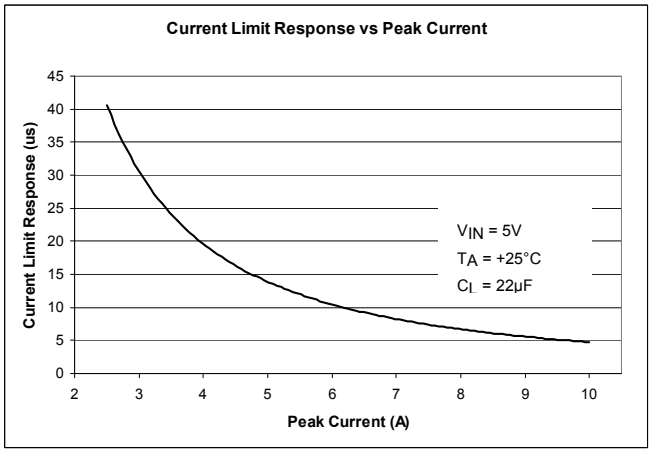
Typical Performance Characteristics (cont.)











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Application Information

Power Supply Considerations

A 0.01-µF to 0.1-µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before V_{IN} has been applied. The AP2142/AP2152 senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT}.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT}.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIG}) is reached or until the thermal limit of the device is exceeded. The AP2142/AP2152 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT}.

FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2142/AP2152 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A= Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2142/AP2152 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

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Application Information (cont.)

Under-Voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Host/Self-Powered HUBs

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

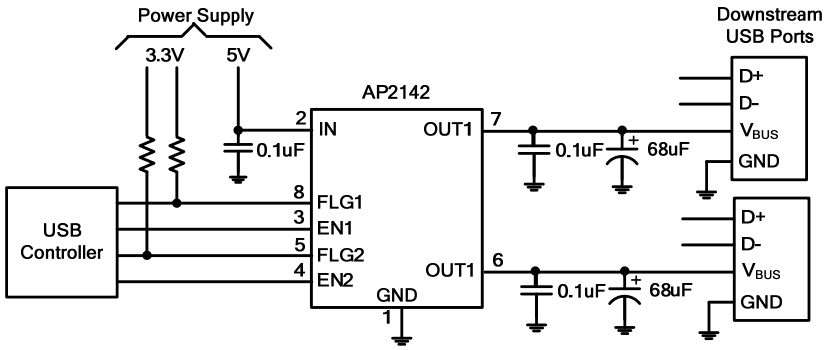


Figure 2. Typical Two-Port USB Host / Self-Powered Hub

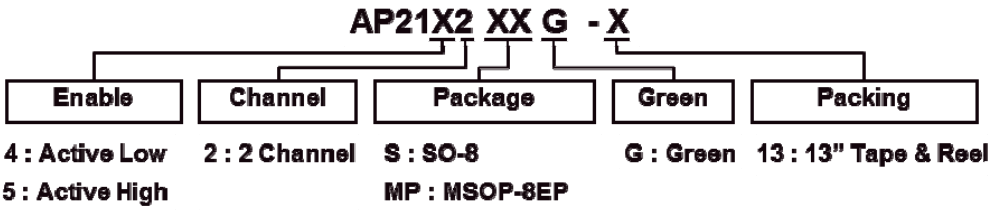
Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2142/AP2152, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2142/AP2152 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2142/AP2152 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

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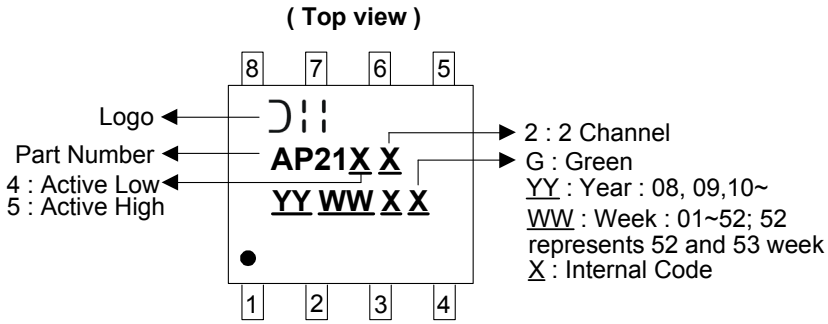
Ordering Information



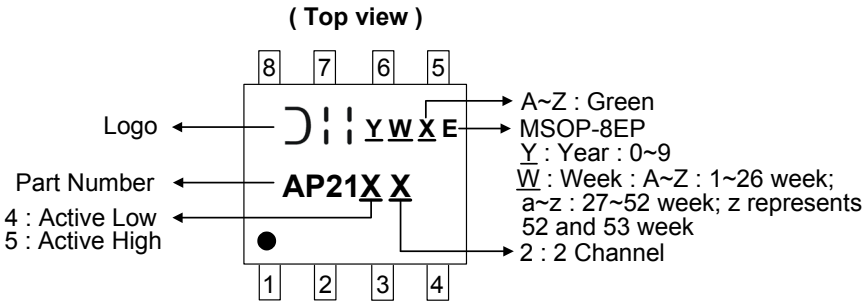
Part Number	Package Code	Packaging	13" Tape and Reel	
			Quantity	Part Number Suffix
AP21X2SG-13	S	SO-8	2500/Tape & Reel	-13
AP21X2MPG-13	MP	MSOP-8EP	2500/Tape & Reel	-13

Marking Information

(1) SO-8



(2) MSOP-8EP

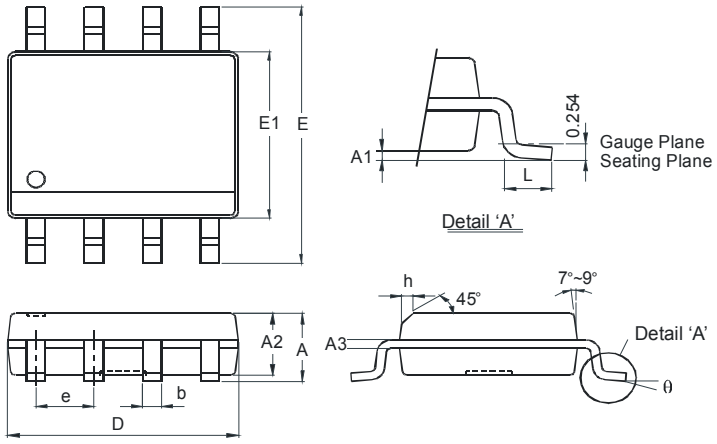


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Package Outline Dimensions (All dimensions in mm.)

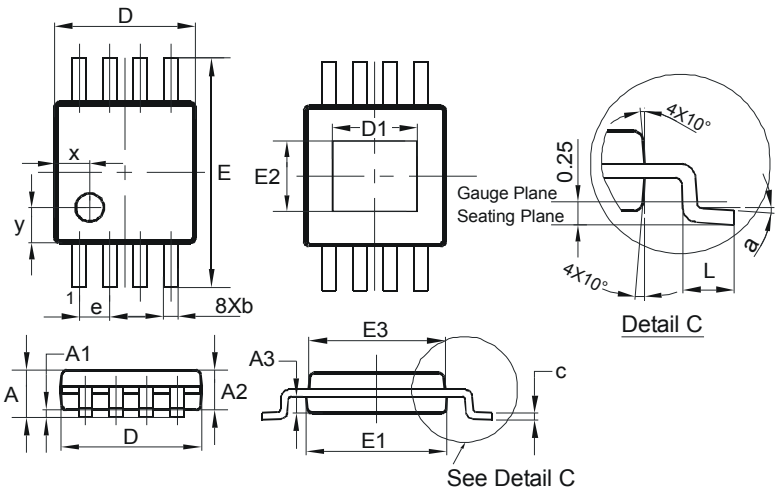
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

(1) Package type: SO-8



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

(2) Package type: MSOP-8EP



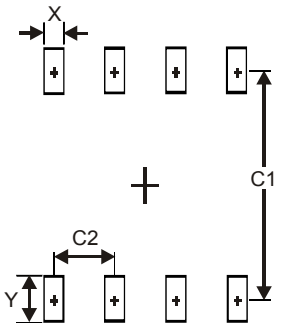
MSOP-8EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

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Suggested Pad Layout

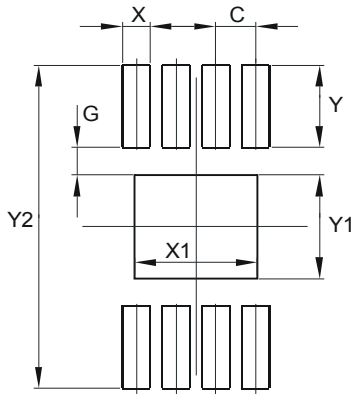
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) Package type: SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

(2) Package type: MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

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