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NTE7156
Integrated Circuit
DC–Coupled Vertical Deflection Circuit

Description:

The NTE7156 is a power circuit in a 9–Lead SIP type package designed for use in 90° and 110° color deflection systems for field frequencies of 50Hz to 120Hz. This device provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

Features:

- Few External Components
- Highly Efficient Fully DC–Coupled Vertical Output Bridge Circuit
- Vertical Flyback Switch
- Guard Circuit
- Protection Aaginst:
  - Short–Circuit of the Output Pins (7 and 4)
  - Short–Circuit of the Output Pins to V_P
- Temperature Protection
- High EMC Immunity Because of Common Mode Inputs
- A Guard Signal in Zoom Mode

Absolute Maximum Ratings:

DC Supply

Supply Voltage, V_P
- Non–Operating 40V
- Operating 25V

Flyback Supply Voltage, V_{FB} 50V
- Note 1 . . . . . 60V

Vertical Circuit

Output Current (Peak–to–Peak Value, Note 2), $I_{O(P–P)}$ 3A

Output Voltage (Pin7), $V_{O(A)}$ 52V
- Note 1 . . . . . 62V

Flyback Switch

Peak Output Current, I_M . . . . . ±15A

Thermal Data

Virtual Junction Temperature, T_{VJ} . . . . . +150°C

Operating Ambient Temperature Range, T_A . . . . . –20° to +75°C

Storage Temperature Range, T_{stg} . . . . . –55° to +150°C

Thermal Resistance, Virtual Junction–to–Ambient, $R_{thVJ–C}$ 40K/W

Thermal Resistance, Virtual Junction–to–Case, $R_{thVJ–A}$ 4K/W

Short–Circuit Time (Note 3), t_{sc} . . . . . 1 Hour

Note 1. A flyback supply voltage of > 50V up to 60V is allowed in application. A 22–nF capacititor in series with a 22Ω resistor (depending on I_O and the inductance of the coil) has to be connected between Pin7 and GND. The decoupling capacitor of V_{FB} has to be connected between Pin6 and Pin3. This supply voltage line must have a resistance of 33Ω.

Note 2. I_O maximum determined by current protection.

Note 3. Up to V_P = 18V.

Electrical Characteristics: (V_P = 17.5V, T_A = +25°C, V_{FB} = 45V, f_i = 50Hz, $I_{I(sb)}$ = 400µA unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Supply						
Operating Supply Voltage	V_P		9	–	25	V
Flyback Supply Voltage	V_{FB}		V_P	–	50	V
		Note 1	V_P	–	60	V
Supply Current	I_P	No Load, No Signal	–	30	55	mA
Vertical Circuit						
Output Voltage Swing (Scan)	V_O	I_{diff} = 0.6mA$_{(P–P)}$, V_{diff} = 1.8V$_{(P–P)}$, I_O = 3A$_{(P–P)}$	19.8	–	–	V
Linearity Error	LE	I_O = 3A$_{(P–P)}$, Note 4	–	1	3	%
		I_O = 50mA$_{(P–P)}$, Note 4	–	1	3	%
Output Voltage Swing (Flyback) $V_{O(A)} – V_{O(B)}$	V_O	I_{diff} = 0.3mA, I_O = 1.5A	–	39	–	V
Forward Voltage of the Internal Efficiency Diode ($V_{O(A)} – V_{FB}$)	V_{DF}	I_O = –1.5A, I_{diff} = 0.3mA	–	–	1.5	V
Output Offset Current	$\|I_{OS}\|$	I_{diff} = 0, $I_{I(sb)}$ = 50µA to 500µA	–	–	30	mA
Offset Voltage at the Input of the Feedback Amplifier ($V_{I(fb)} – V_{O(B)}$)	ΔV_{OS} T	I_{diff} = 0	–	–	72	µV/K
DC Output Voltage	$V_{O(A)}$	I_{diff} = 0, Note 5	–	8	–	V
Open Loop Voltage Gain ($V_{7–4}/V_{1–2}$)	G_{VO}	Note 6, Note 7	–	80	–	dB
Open Loop Voltage Gain ($V_{7–4}/V_{9–4}$, $V_{1–2}$ = 0)		Note 6	–	80	–	dB
Voltage Ratio $V_{1–2}/V_{9–4}$	V_R		–	0	–	dB
Frequency Response (–3dB)	f_{res}	Open Loop, Note 8	–	40	–	Hz
Current Gain (I_O/I_{diff})	G_I		–	5000	–	
Current Gain Drift as a Function of Temperature	ΔG_C T		–	–	$10^{–4}$	K
Signal Bias Current	$I_{I(sb)}$		50	400	500	µA
Flyback Supply Current	I_{FB}	During Scan	–	–	100	µA
Power Supply Ripple Rejection	PSRR	Note 9	–	80	–	dB
DC Input Voltage	$V_{I(DC)}$		–	2.7	–	V
Common Mode Input Voltage	$V_{I(CM)}$	$I_{I(sb)}$ = 0	0	–	1.6	V
Input Bias Current	I_{bias}	$I_{I(sb)}$ = 0	–	0.1	0.5	µA
Common Mode Output Current	$I_{O(CM)}$	$\Delta I_{I(sub)}$ = 300µA$_{(P–P)}$, f_i = 50Hz, I_{diff} = 0	–	0.2	–	mA
Guard Circuit						
Output Current	I_O	Not Active, $V_{O(guard)}$ = 0V	–	–	50	µA
		Active, $V_{O(guard)}$ = 3.6V	1.0	–	2.5	mA
Output Voltage on Pin8	$V_{O(guard)}$	I_O = 100µA	4.6	–	5.5	V
Allowable Voltage on Pin8		Maximum Leakage Current = 10µA	–	–	40	V

Notes:

Note 1. A flyback supply voltage of > 50V up to 60V is allowed in application. A 22–nF capacititor in series with a 22Ω resistor (depending on I_O and the inductance of the coil) has to be connected between Pin7 and GND. The decoupling capacitor of V_{FB} has to be connected between Pin6 and Pin3. This supply voltage line must have a resistance of 33Ω.

Note 4. The linearity error is measured without S–correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
Divide the output signal $I_4 - I_7$ (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 21 (block 10). Thus part 1 and 22 are unused. The equations for linearity error for adjacent blocks (LEAB) and linearity error for not adjacent blocks (LENAB) are given below:

$$LEAB = \frac{a_k - a_{(k+1)}}{a_{avg}} \; ; \; LEAB = \frac{a_{max} - a_{min}}{a_{avg}}$$

Note 5. Referenced to V_P.

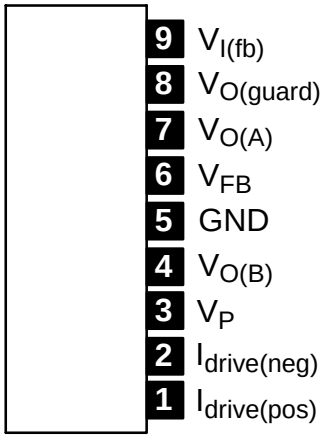
Note 6. The V values within formulae relate to voltages at or across relative pin numbers, i.e. V_{7-4}/V_{1-2} = voltage value across Pin7 and Pin4 divided by voltage value across Pin1 and Pin2.

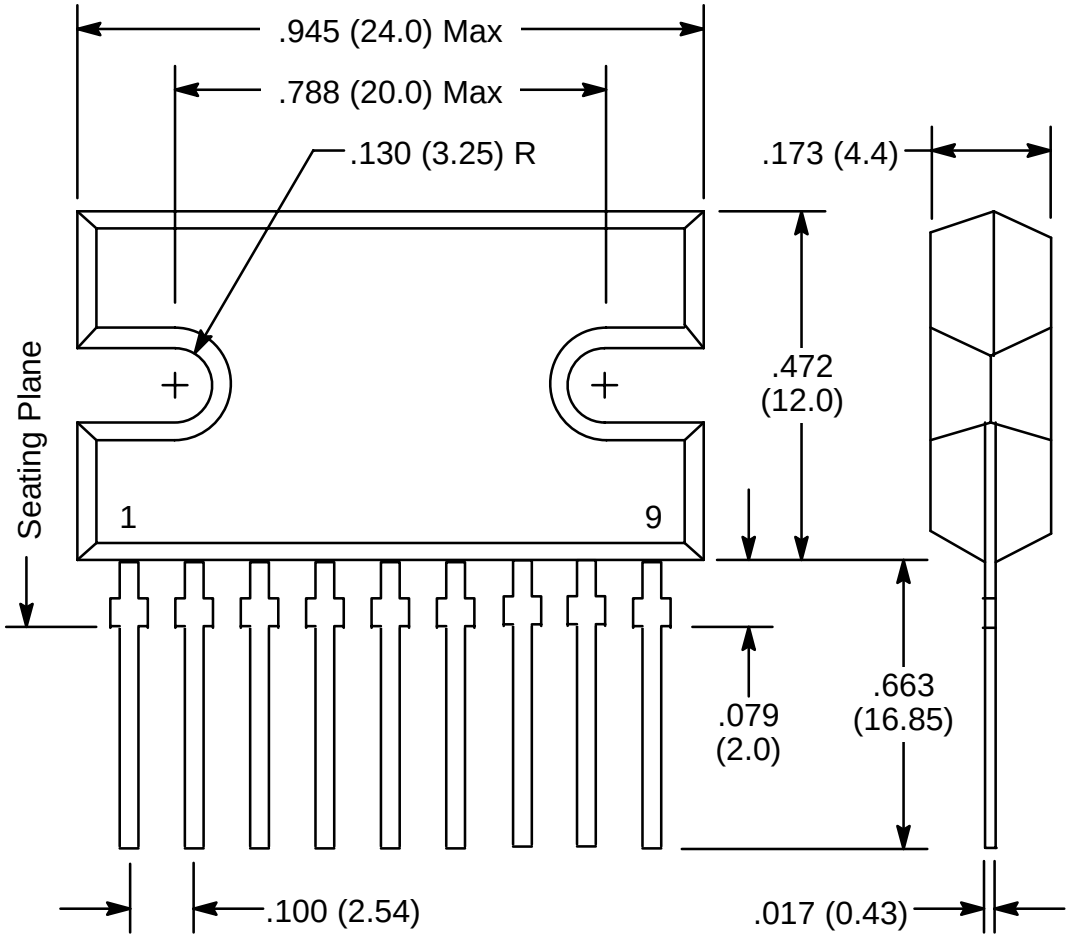
Note 7. V_{9-4} AC short–circuited.

Note 8. Frequency response V_{7-4}/V_{9-4} is equal to frequency response V_{7-4}/V_{1-2}.

Note 9. At $V_{(ripple)}$ = 500mV eff; measured across R_M; f_i = 50Hz.

Pin Connection Diagram
(Front View)




.945 (24.0) Max
.788 (20.0) Max
.130 (3.25) R
.173 (4.4)
Seating Plane
.472
(12.0)
1
9
.079
(2.0)
.663
(16.85)
.100 (2.54)
.017 (0.43)