

# iAPX88/188, MCS 196, MCS51 Compatible\*

64K

**X88064**

8192 x 8 Bit

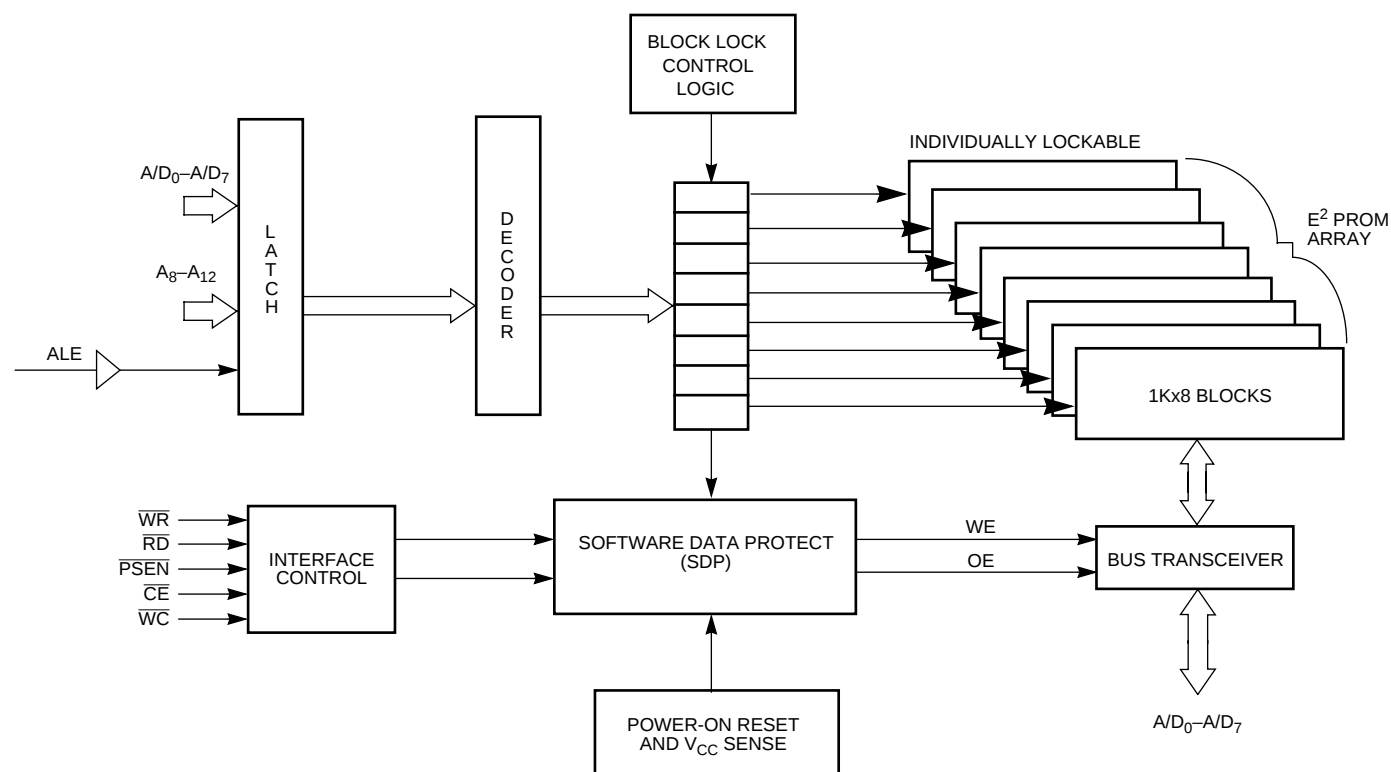
## E<sup>2</sup> Microcontroller Peripheral

- **Block Lock Write Control**
  - Eight 1K Byte Blocks
  - Lockable Independently or in Combination
- **Multiplexed Address/Data Bus**
  - Direct Interface to Popular Microcontrollers
- **High Performance CMOS**
  - Fast Access Times, 60ns and 80 ns
  - Low Power
    - 30mA Active Maximum
    - 150µA Standby Maximum
- **Software Data Protection**
- **Toggle Bit Polling**
  - Early End of Write Detection
- **Page Mode Write**
  - Allows up to 32 Bytes to be Written in One Write Cycle

### DESCRIPTION

The X88064 is a high speed byte wide microperipheral device with eight 1K byte blocks of E<sup>2</sup>PROM and can be directly connected to industry standard high performance microprocessors. This peripheral provides two levels of memory write control, the standard Software Data Program (SDP) control and Block Lock.

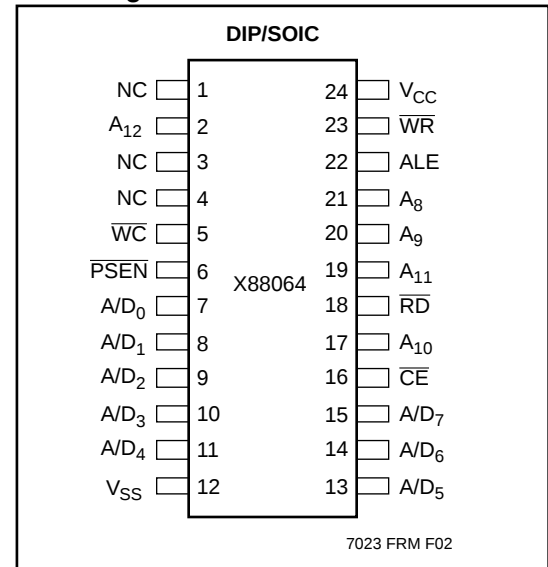
Block Lock provides a higher level of memory write control above SDP. This allows the software developer to partition any or all of the eight 1K byte blocks as In-Circuit Programmable ROM (ICPROM). Once locked, a block of memory must first be unlocked before being written. Not even a write operation using the SDP sequence will change the contents of a locked block. Since a distinct, 6 byte, software command sequence locks and unlocks the memory, the software developer has complete control of the memory contents.



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Software Data Program Control provides a lower level of memory write management. SDP controls write operations to the entire memory. When enabled, the host microprocessor must send a special 3 byte command sequence before any byte or page writes to unlocked locations in the memory.

## Pin configuration



## PIN NAMES

| PIN NAME                           | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                             |
|------------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\overline{\text{PSEN}}$           | I   | Content of $\text{E}^2$ memory can be read by lowering the $\overline{\text{PSEN}}$ and holding both $\overline{\text{RD}}$ and $\overline{\text{WR}}$ HIGH. The device then places on the data bus ( $\text{AD}_0\text{--}\text{AD}_7$ ) the contents of $\text{E}^2$ memory at the latched address.                                                   |
| $\text{A}_8\text{--}\text{A}_{12}$ | I   | Non-multiplexed high-order Address Bus inputs for the upper byte of the address.                                                                                                                                                                                                                                                                        |
| $\text{AD}_0\text{--}\text{AD}_7$  | I/O | Multiplexed low-order Address and Data Bus. The addresses are latched when ALE makes a HIGH to LOW transition.                                                                                                                                                                                                                                          |
| $\overline{\text{WR}}$             | I   | During a byte/page write cycle $\overline{\text{WR}}$ is brought LOW while $\overline{\text{RD}}$ is held HIGH and the data is placed on the bus. The rising edge of $\overline{\text{WR}}$ latches data into the device.                                                                                                                               |
| $\overline{\text{RD}}$             | I   | The $\overline{\text{RD}}$ input is active LOW and is used to read content of the $\text{E}^2$ memory at the latched address. Both $\overline{\text{PSEN}}$ and $\overline{\text{WR}}$ signals must be held HIGH during $\overline{\text{RD}}$ controlled read operation.                                                                               |
| $\overline{\text{WC}}$             | I   | $\overline{\text{WC}}$ input has to be held LOW during a write cycle. It can be permanently tied HIGH in order to disable write to the $\text{E}^2$ memory. Taking $\overline{\text{WC}}$ HIGH prior to $t_{\text{BLC}}$ (100ns, the time delay from the last write cycle to the start of internal programming cycle) will inhibit the write operation. |
| $\overline{\text{CE}}$             | I   | The device select ( $\overline{\text{CE}}$ ) is an active LOW input. This signal has to be asserted prior to ALE HIGH to LOW transition in order to generate a valid internal device select signal. Holding this pin HIGH and ALE LOW will place the device in standby mode.                                                                            |
| ALE                                | I   | Address Latch Enable input is used to latch the addresses present on the address lines $\text{A}_8\text{--}\text{A}_{12}$ and $\text{AD}_0\text{--}\text{AD}_7$ into the device. The addresses are latched when ALE transitions from HIGH to LOW.                                                                                                       |

# X88064

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## PRINCIPLES OF OPERATION

The X88064 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88064 provides 8K bytes of E<sup>2</sup>PROM which can be used either for Program Storage, Data Storage, or a combination of both, in systems based upon Harvard (80XX) architectures. The X88064 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a “Seamless” interface.

The interface inputs on the X88064 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the  $\overline{\text{PSEN}}$  or the  $\overline{\text{RD}}$  signal, which essentially maps the X88064 into both the Program and the Data Memory address map.

The X88064 also features an advanced implementation of the Software Data Protection scheme, called Block Lock, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88064 also features a Write Control input ( $\overline{\text{WC}}$ ), which serves as an external control over the completion of a previously initiated page load cycle.

The X88064 also features the industry standard E<sup>2</sup>PROM characteristics such as byte or page mode write and Toggle Bit Polling.

## DEVICE OPERATION MODES

### Mixed Program/Data Memory

By properly assigning the address space, a single X88064 can be used as both the Program and Data Memory. This would be accomplished by connecting all of the Microcontroller control outputs to the corresponding inputs of the X88064.

The Data Storage can be fully protected by enabling Block Lock Control.

### Program Memory Mode

This mode of operation is read-only. The  $\overline{\text{PSEN}}$  and  $\overline{\text{ALE}}$  inputs of the X88064 are tied directly to the  $\overline{\text{PSEN}}$  and  $\overline{\text{ALE}}$  outputs of the microcontroller. The  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  inputs are tied HIGH.

When  $\overline{\text{ALE}}$  is HIGH, the  $\text{A/D}_0\text{--A/D}_7$  and  $\text{A}_8\text{--A}_{12}$  addresses flow into the device. The addresses, both low and high order, are latched when  $\overline{\text{ALE}}$  transitions LOW ( $\text{V}_{\text{IL}}$ ).  $\overline{\text{PSEN}}$  will then go LOW and after  $t_{\text{PLDV}}$ , valid data is presented on the  $\text{A/D}_0\text{--A/D}_7$  pins.  $\overline{\text{CE}}$  must be LOW during the entire operation.

### Data Memory Mode

This mode of operation allows both read and write functions. The  $\overline{\text{PSEN}}$  input is tied to  $\text{V}_{\text{IH}}$  or to  $\text{V}_{\text{CC}}$  through a pull-up resistor. The  $\overline{\text{ALE}}$ ,  $\overline{\text{RD}}$ , and  $\overline{\text{WR}}$  inputs are tied directly to the microcontroller's  $\overline{\text{ALE}}$ ,  $\overline{\text{RD}}$ , and  $\overline{\text{WR}}$  outputs.

#### Read

This operation is quite similar to the Program Memory read. A HIGH to LOW transition on  $\overline{\text{ALE}}$  latches the addresses and the data will be output on the  $\text{A/D}$  pins after  $\overline{\text{RD}}$  goes LOW ( $t_{\text{RLDV}}$ ).

#### Write

A write is performed by latching the addresses on the falling edge of  $\overline{\text{ALE}}$ . Then  $\overline{\text{WR}}$  is strobed LOW followed by valid data being presented at the  $\text{A/D}_0\text{--A/D}_7$  pins. The data will be latched into the X88064 on the rising edge of  $\overline{\text{WR}}$ . To write to the X88064, with the SDP feature enabled, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

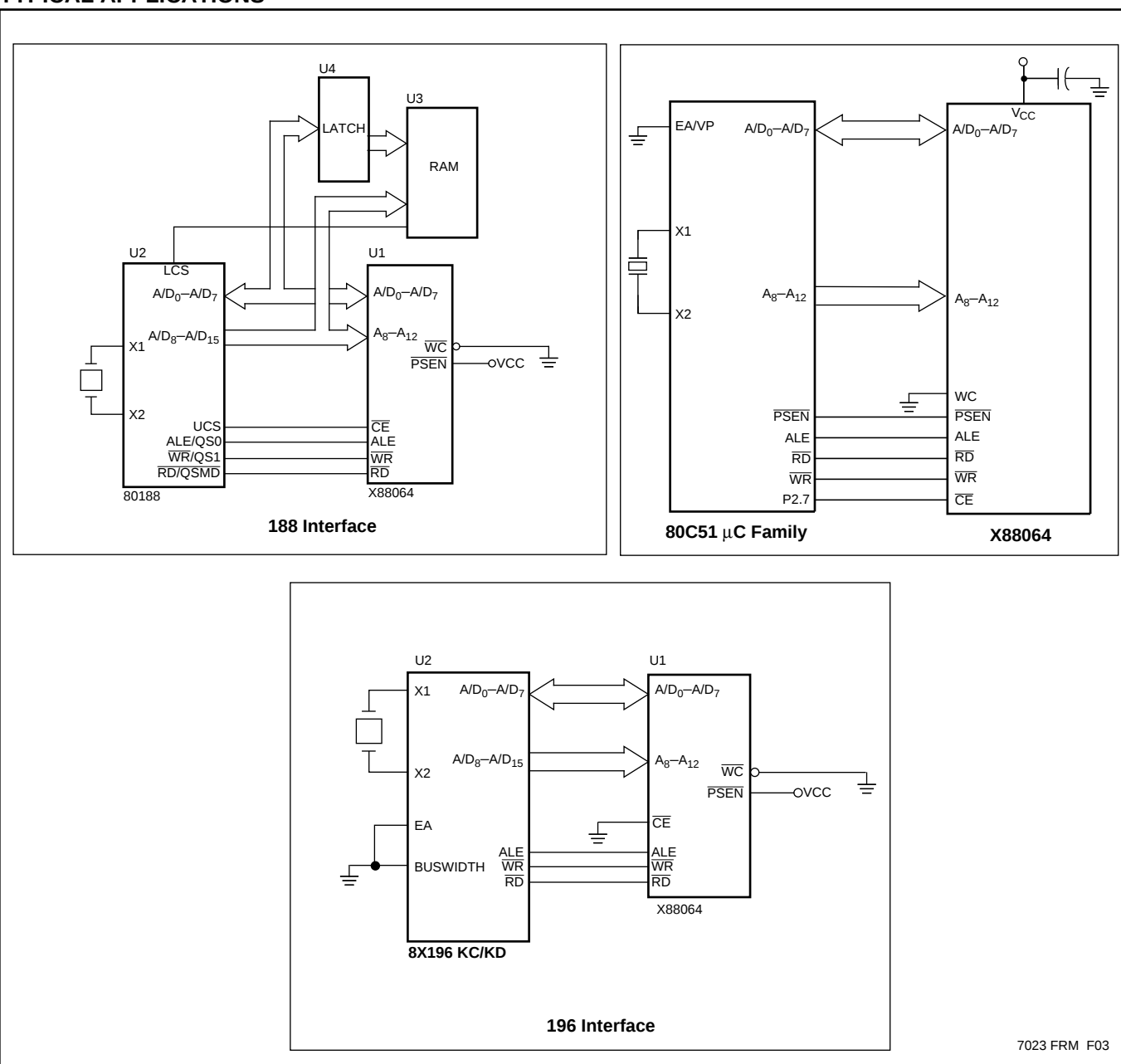
# X88064

## MODE SELECTION

| $\overline{CE}$ | $\overline{PSEN}$ | $\overline{RD}$ | $\overline{WR}$ | Mode          | I/O              | Power          |
|-----------------|-------------------|-----------------|-----------------|---------------|------------------|----------------|
| V <sub>CC</sub> | X                 | X               | X               | Standby       | High Z           | Standby (CMOS) |
| HIGH            | X                 | X               | X               | Standby       | High Z           | Standby (TTL)  |
| LOW             | LOW               | HIGH            | HIGH            | Program Fetch | D <sub>OUT</sub> | Active         |
| LOW             | HIGH              | LOW             | HIGH            | Data Read     | D <sub>OUT</sub> | Active         |
| LOW             | HIGH              | HIGH            | —               | Write         | D <sub>IN</sub>  | Active         |

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## TYPICAL APPLICATIONS



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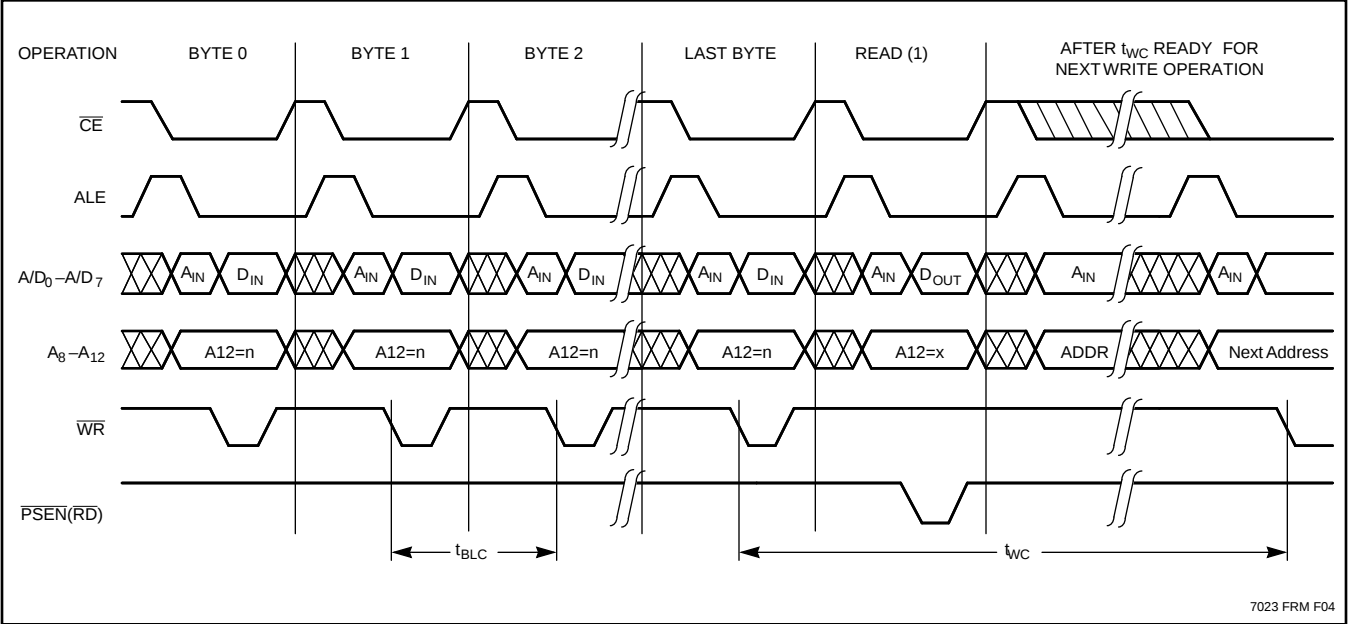
# X88064

## PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88064 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88064. Each individual write within a page

write operation must conform to the byte write timing requirements. The falling edge of  $\overline{WR}$  starts a timer delaying the internal programming cycle  $100\mu\text{s}$ . Therefore, each successive write operation must begin within  $100\mu\text{s}$  of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for  $\overline{WR}$  Controller Operation



**Notes:** (1) For each successive write within a page write cycle  $A_5$ - $A_{12}$  must be the same.

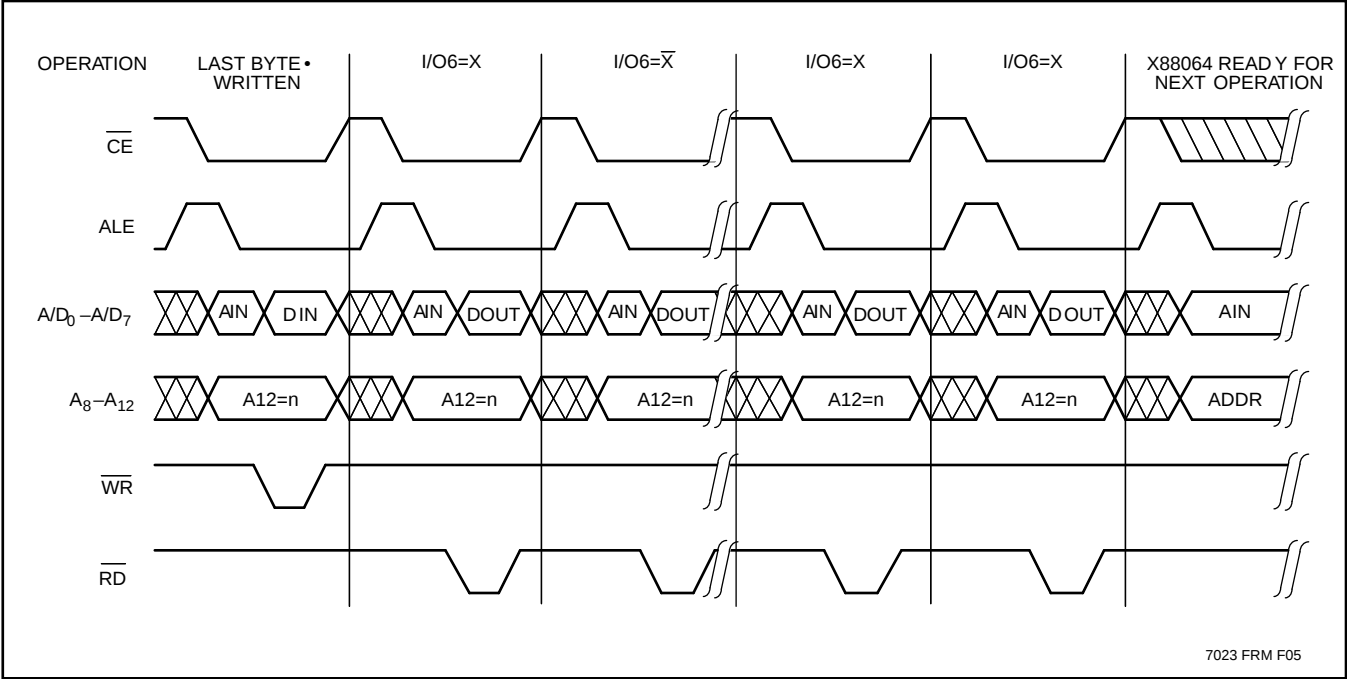
# X88064

## TOGGLE BIT POLLING

Because the X88064 typical nonvolatile write cycle time is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early completion of write. During the internal programming cycle I/O<sub>6</sub> will toggle from HIGH to LOW and LOW to HIGH on subsequent

attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

## Toggle Bit Polling RD/WR Control



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## Symbol Table

| WAVEFORM | INPUTS                      | OUTPUTS                       |
|----------|-----------------------------|-------------------------------|
|          | Must be steady              | Will be steady                |
|          | May change from LOW to HIGH | Will change from LOW to HIGH  |
|          | May change from HIGH to LOW | Will change from HIGH to LOW  |
|          | Don't Care: Changes Allowed | Changing: State Not Known     |
|          | N/A                         | Center Line is High Impedance |

## X88064

### DATA PROTECTION

The X88064 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E<sup>2</sup>PROMs and a new Block Lock Control providing a secondary level of data security.

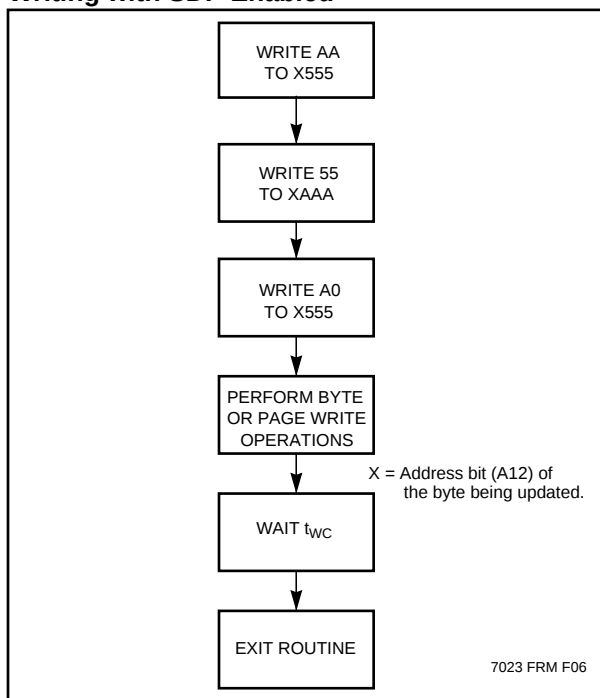
### SOFTWARE DATA PROTECTION

The X88064 offers a software controlled data protection feature. The X88064 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host then has open read and write access of the device once  $V_{CC}$  is stable.

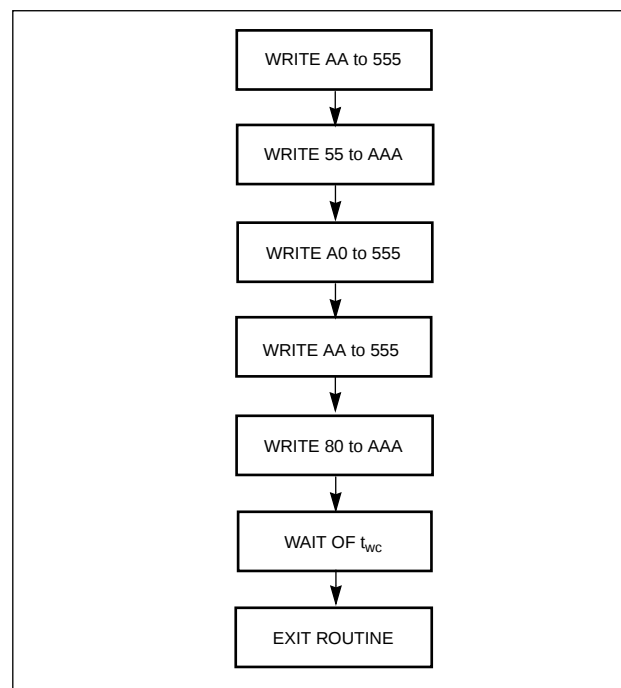
The X88064 can be automatically protected during power-up/down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the SDP deactivation command is issued.

Once the software protection is enabled, the X88064 is also protected from inadvertent and accidental writes in the powered-up state. That is, the SDP software algorithm must be issued prior to writing additional data to the device.

### Writing with SDP Enabled



### SEQUENCE TO DEACTIVATE SOFTWARE DATA PROTECTION



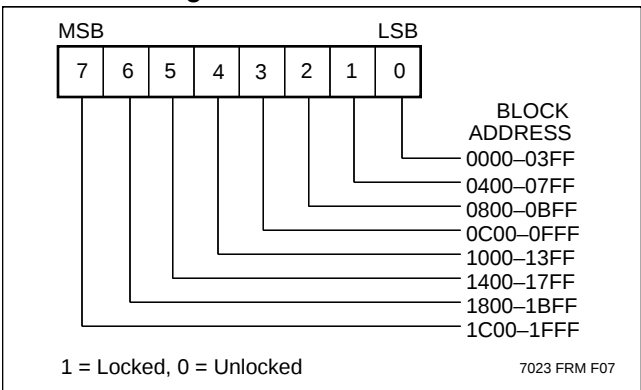
# X88064

## Block Lock Write Control

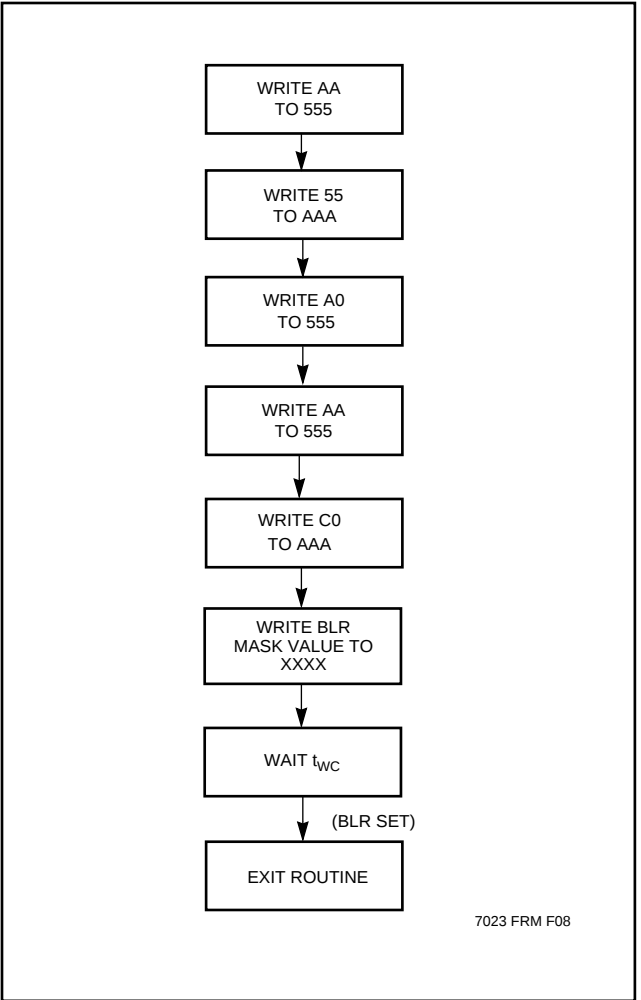
The X88064 provides a secondary level of data security referred to as Block Lock Control. This is accessed through an extension of the SDP command sequence. Block Lock allows the user to inhibit writes to any 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Lock will inhibit all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Storage and another portion is used as Data Storage.

Setting write lockout is accomplished by writing a five-byte command sequence, opening access to the Block Lock Register (BLR). After the fifth byte is written, the user writes to the BLR, selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BLR, must conform to the page write timing requirements.

## Block Lock Register Format



## Setting Block Lock Register Sequence



# X88064

## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias.....-65°C to +135°C  
 Storage Temperature .....-65°C to +150°C  
 Voltage on any Pin with  
 Respect to  $V_{SS}$  .....-1V to +7V  
 D.C. Output Current..... 5 mA  
 Lead Temperature  
 (Soldering, 10 seconds)300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temperature | Min.  | Max.  |
|-------------|-------|-------|
| Commercial  | 0°C   | +70°C |
| Industrial  | -40°C | +85°C |

| Supply Voltage | Limits       |
|----------------|--------------|
| X88064         | 5V $\pm$ 10% |
| X88064-60      | 5V $\pm$ 10% |

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## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

| Symbol          | Parameter                  | Limits |                |         | Test Conditions                                                                                     |
|-----------------|----------------------------|--------|----------------|---------|-----------------------------------------------------------------------------------------------------|
|                 |                            | Min.   | Max.           | Units   |                                                                                                     |
| $I_{CC}$        | $V_{CC}$ Current (Active)  |        | 30             | mA      | $\overline{CE} = \overline{RD} = V_{IL}$ , All I/O's = Open, Other Inputs = $V_{CC}$                |
| $I_{SB1(CMOS)}$ | $V_{CC}$ Current (Standby) |        | 150            | $\mu$ A | $\overline{CE} = V_{CC} - 0.3V$ , All I/O's = Open, Other Inputs = $V_{CC} - 0.3V$ , ALE = $V_{IL}$ |
| $I_{SB2(TTL)}$  | $V_{CC}$ Current (Standby) |        | 2.5            | mA      | $\overline{CE} = V_{IH}$ , All I/O's = Open, Other Inputs = $V_{IH}$ , ALE = $V_{IL}$               |
| $I_{LI}$        | Input Leakage Current      |        | 10             | $\mu$ A | $V_{IN} = V_{SS}$ to $V_{CC}$                                                                       |
| $I_{LO}$        | Output Leakage Current     |        | 10             | $\mu$ A | $V_{OUT} = V_{SS}$ to $V_{CC}$ , $\overline{RD} = V_{IH} = \overline{PSEN}$                         |
| $V_{IL(3)}$     | Input LOW Voltage          | -1     | 0.8            | V       |                                                                                                     |
| $V_{IH(3)}$     | Input HIGH Voltage         | 2      | $V_{CC} + 0.5$ | V       |                                                                                                     |
| $V_{OL}$        | Output LOW Voltage         |        | 0.4            | V       | $I_{OL} = 2.1$ mA                                                                                   |
| $V_{OH}$        | Output HIGH Voltage        | 2.4    |                | V       | $I_{OH} = -400$ $\mu$ A                                                                             |

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## CAPACITANCE $T_A = +25^\circ\text{C}$ , $f = 1\text{MHz}$ , $V_{CC} = 5V$

| Symbol       | Test                     | Max. | Units | Conditions     |
|--------------|--------------------------|------|-------|----------------|
| $C_{I/O(4)}$ | Input/Output Capacitance | 10   | pF    | $V_{I/O} = 0V$ |
| $C_{IN(4)}$  | Input Capacitance        | 6    | pF    | $V_{IN} = 0V$  |

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## POWER-UP TIMING

| Symbol       | Parameter         | Max. | Units |
|--------------|-------------------|------|-------|
| $t_{PUR(4)}$ | Power-Up to Read  | 1    | ms    |
| $t_{PUW(4)}$ | Power-Up to Write | 5    | ms    |

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Notes: (3)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

(4) This parameter is periodically sampled and not 100% tested.

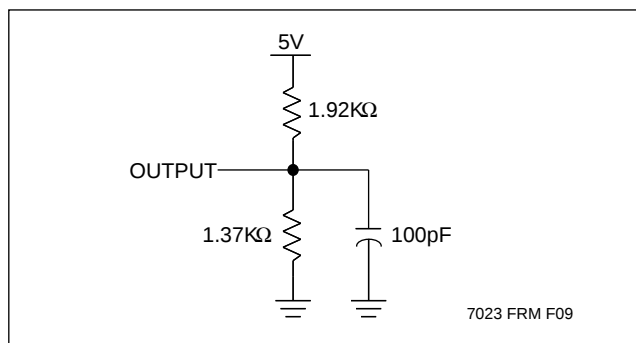
# X88064

## A.C. CONDITIONS OF TEST

|                                |          |
|--------------------------------|----------|
| Input Pulse Levels             | 0V to 3V |
| Input Rise and Fall Times      | 10ns     |
| Input and Output Timing Levels | 1.5V     |

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## EQUIVALENT A.C. TEST CIRCUIT

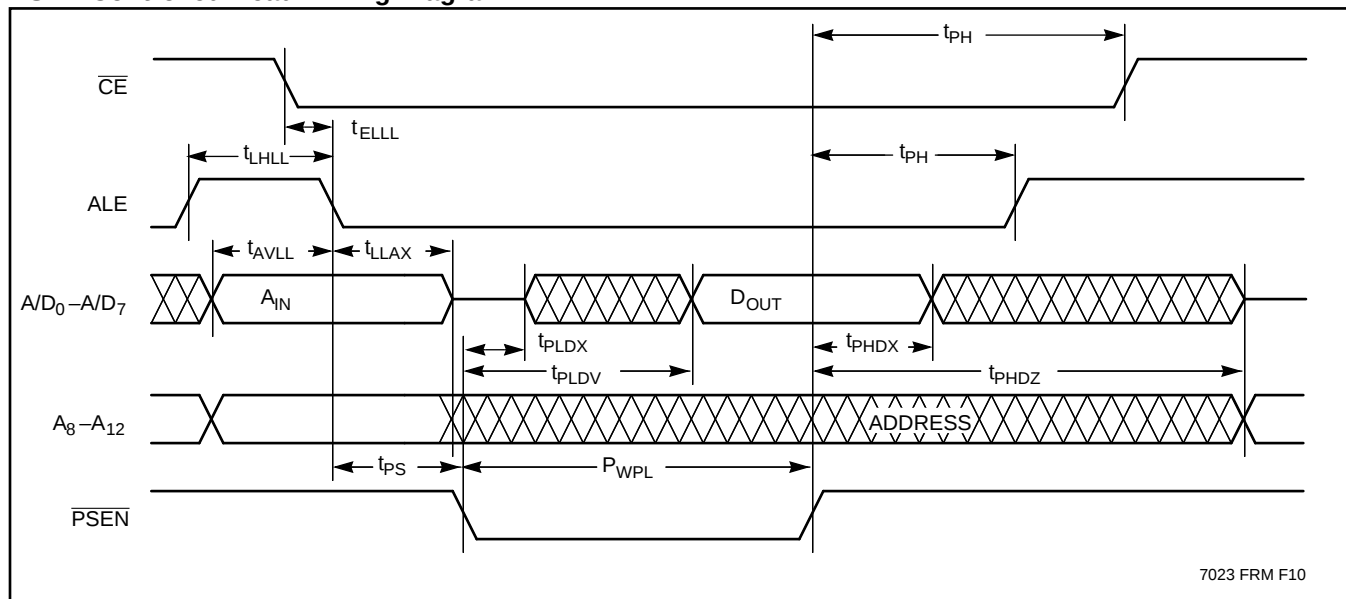


## PSEN Controlled Read Cycle

| Symbol                | Parameter                        | X88064 – 60 |      | X88064 |      | Units |
|-----------------------|----------------------------------|-------------|------|--------|------|-------|
|                       |                                  | Min.        | Max. | Min.   | Max. |       |
| t <sub>LHLL</sub>     | ALE Pulse Width                  | 60          |      | 80     |      | ns    |
| t <sub>AVLL</sub>     | Address Setup Time               | 10          |      | 10     |      | ns    |
| t <sub>LLAX</sub>     | Address Hold Time                | 20          |      | 20     |      | ns    |
| t <sub>PLDV</sub>     | PSEN Read Access Time            |             | 45   |        | 80   | ns    |
| t <sub>PHDX</sub>     | Data Hold Time                   | 0           |      | 0      |      | ns    |
| t <sub>ELLL</sub>     | Chip Enable Setup Time           | 7           |      | 7      |      | ns    |
| PW <sub>PL</sub>      | PSEN Pulse Width                 | 100         |      | 140    |      | ns    |
| t <sub>PS</sub>       | PSEN Setup Time                  | 20          |      | 30     |      | ns    |
| t <sub>PH</sub>       | PSEN Hold Time                   | 20          |      | 20     |      | ns    |
| t <sub>PHDZ</sub> (5) | PSEN Disable to Output in High Z |             | 20   |        | 30   | ns    |
| t <sub>PLDX</sub> (5) | PSEN to Output in Low Z          | 10          |      | 10     |      | ns    |

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## PSEN Controlled Read Timing Diagram



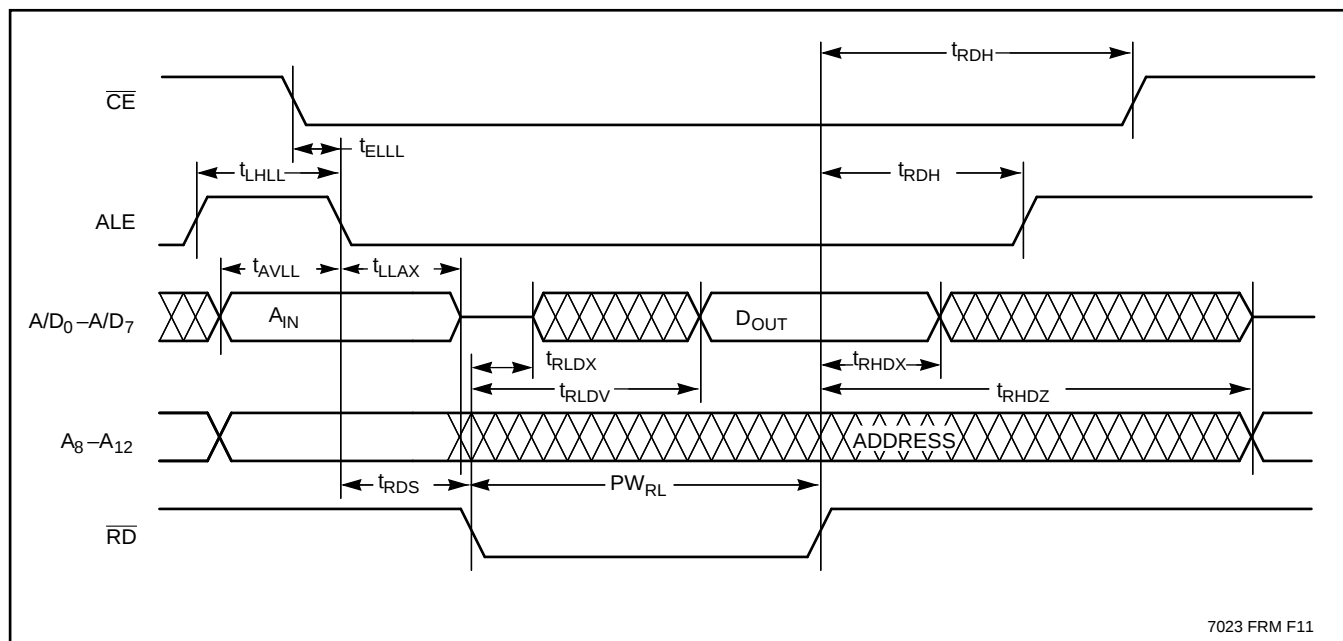
# X88064

## $\overline{\text{RD}}$ Controlled Read Cycle

| Symbol                  | Parameter                                          | X88064 – 60 |      | X88064 |      | Units |
|-------------------------|----------------------------------------------------|-------------|------|--------|------|-------|
|                         |                                                    | Min.        | Max. | Min.   | Max. |       |
| $t_{\text{LHLL}}$       | ALE Pulse Width                                    | 60          |      | 80     |      | ns    |
| $t_{\text{AVLL}}$       | Address Setup Time                                 | 10          |      | 10     |      | ns    |
| $t_{\text{LLAX}}$       | Address Hold Time                                  | 20          |      | 20     |      | ns    |
| $t_{\text{RLDV}}$       | $\overline{\text{RD}}$ Read Access Time            |             | 60   |        | 80   | ns    |
| $t_{\text{RHDX}}$       | Data Hold Time                                     | 0           |      | 0      |      | ns    |
| $t_{\text{ELLL}}$       | Chip Enable Setup Time                             | 7           |      | 7      |      | ns    |
| $\text{PW}_{\text{RL}}$ | $\overline{\text{RD}}$ Pulse Width                 | 120         |      | 150    |      | ns    |
| $t_{\text{RDS}}$        | $\overline{\text{RD}}$ Setup Time                  | 20          |      | 30     |      | ns    |
| $t_{\text{RDH}}$        | $\overline{\text{RD}}$ Hold Time                   | 20          |      | 20     |      | ns    |
| $t_{\text{RHDZ}}^{(6)}$ | $\overline{\text{RD}}$ Disable to Output in High Z |             | 20   |        | 30   | ns    |
| $t_{\text{RLDX}}^{(6)}$ | $\overline{\text{RD}}$ to Output in Low Z          | 0           |      | 0      |      | ns    |

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## $\overline{\text{RD}}$ Controlled Read Timing Diagram



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**Notes:** (6) This parameter is periodically sampled and not 100% tested.

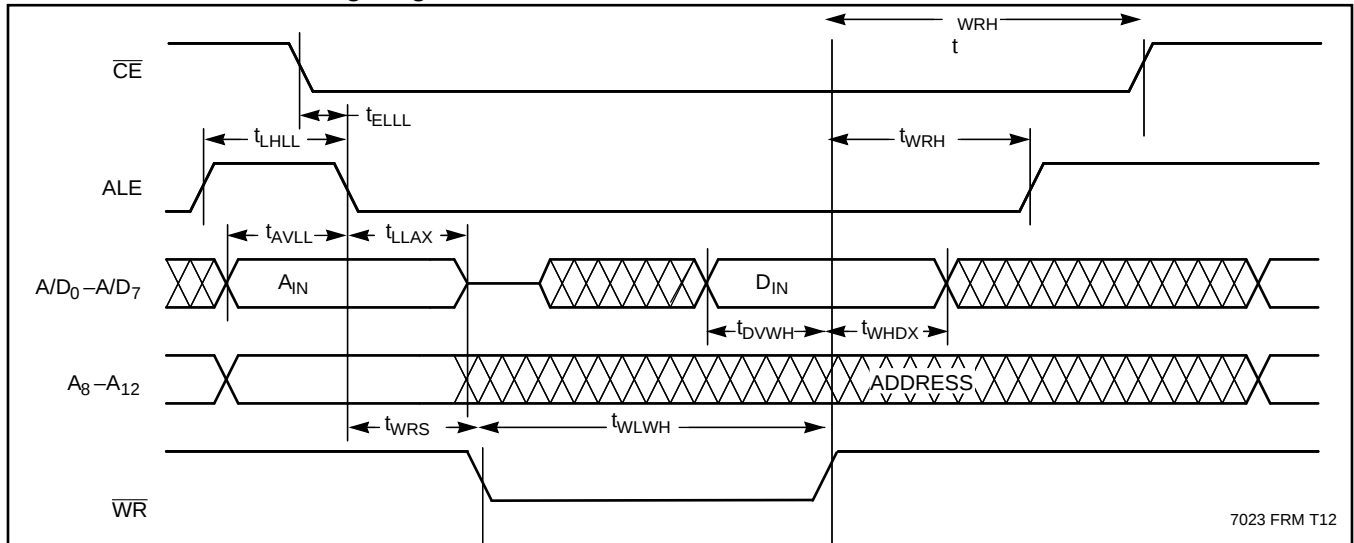
# X88064

## $\overline{\text{WR}}$ Controlled Write Cycle

| Symbol                | Parameter                          | X88064 – 60 |      | X88064 |      | Units         |
|-----------------------|------------------------------------|-------------|------|--------|------|---------------|
|                       |                                    | Min.        | Max. | Min.   | Max. |               |
| $t_{\text{LHLL}}$     | ALE Pulse Width                    | 60          |      | 80     |      | ns            |
| $t_{\text{AVLL}}$     | Address Setup Time                 | 10          |      | 10     |      | ns            |
| $t_{\text{LLAX}}$     | Address Hold Time                  | 20          |      | 20     |      | ns            |
| $t_{\text{DVWH}}$     | Data Setup Time                    | 50          |      | 50     |      | ns            |
| $t_{\text{WHDX}}$     | Data Hold Time                     | 30          |      | 30     |      | ns            |
| $t_{\text{ELLL}}$     | Chip Enable Setup Time             | 7           |      | 7      |      | ns            |
| $t_{\text{WLWH}}$     | $\overline{\text{WR}}$ Pulse Width | 100         |      | 120    |      | ns            |
| $t_{\text{WRS}}$      | $\overline{\text{WR}}$ Setup Time  | 20          |      | 30     |      | ns            |
| $t_{\text{WRH}}$      | $\overline{\text{WR}}$ Hold Time   | 20          |      | 20     |      | ns            |
| $t_{\text{BLC}}$      | Byte Load Time (Page Write)        | 0.5         | 100  | 0.5    | 100  | $\mu\text{s}$ |
| $t_{\text{WC}}^{(7)}$ | Write Cycle Time                   |             | 5    |        | 5    | ms            |

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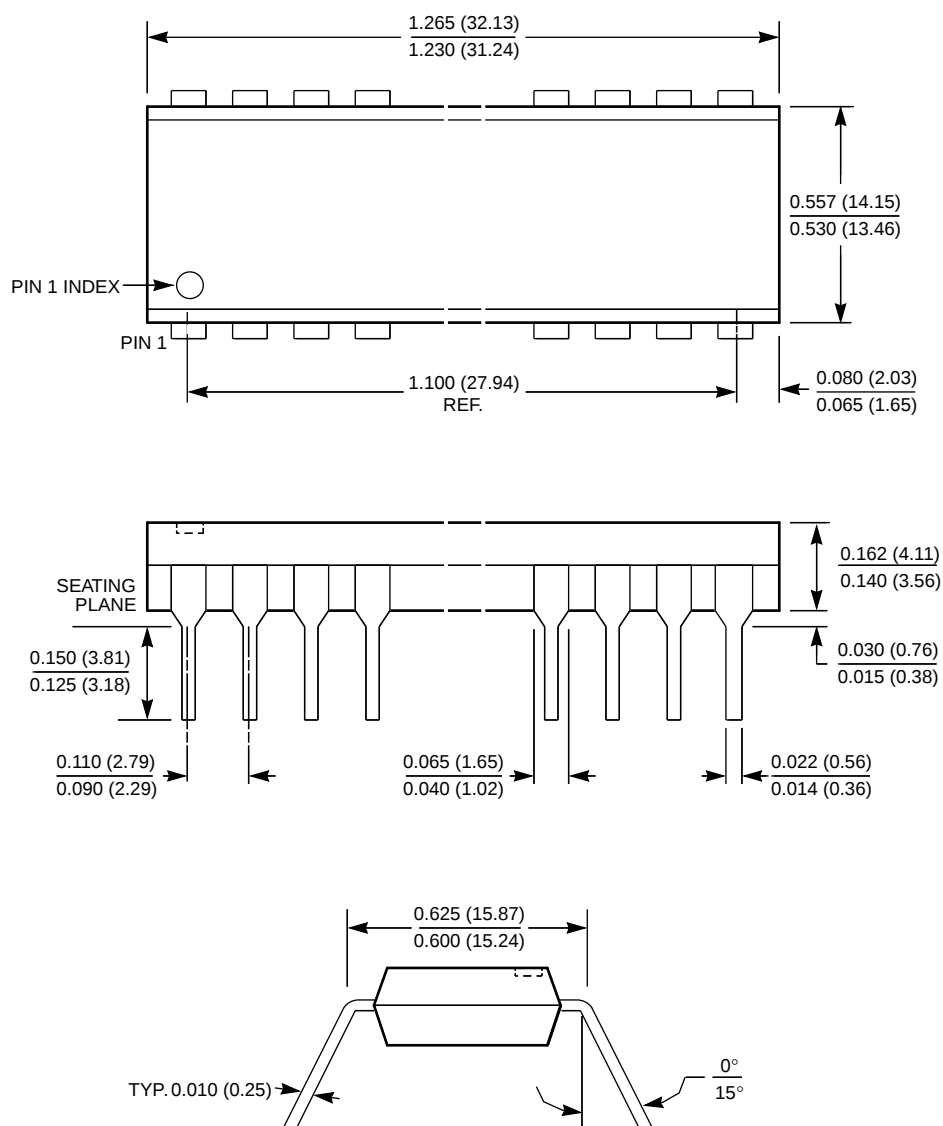
## $\overline{\text{WR}}$ Controlled Write Timing Diagram



**Notes:** (7) TWC is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

## PACKAGING INFORMATION

### 24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



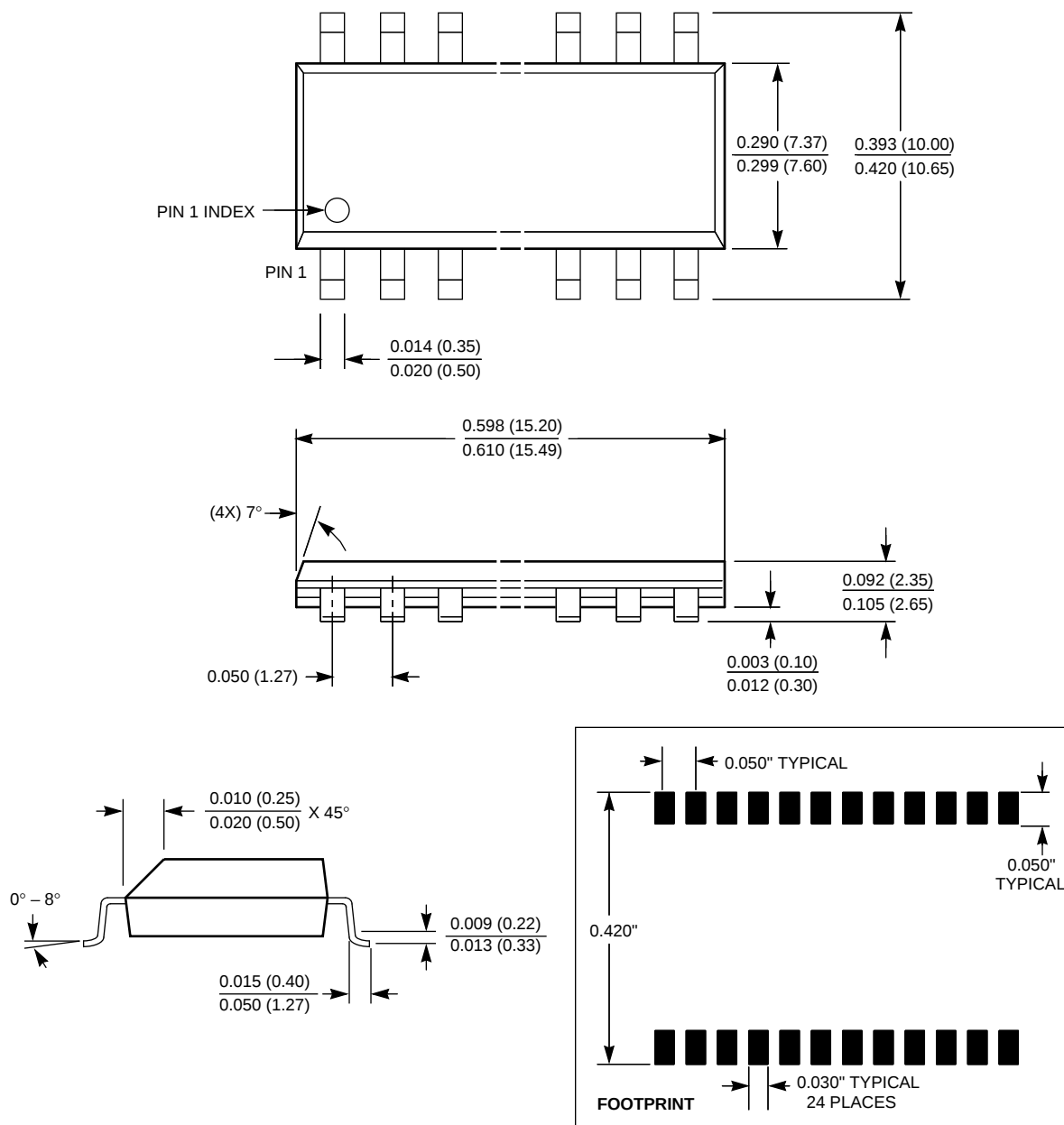
#### NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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## PACKAGING INFORMATION

### 24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



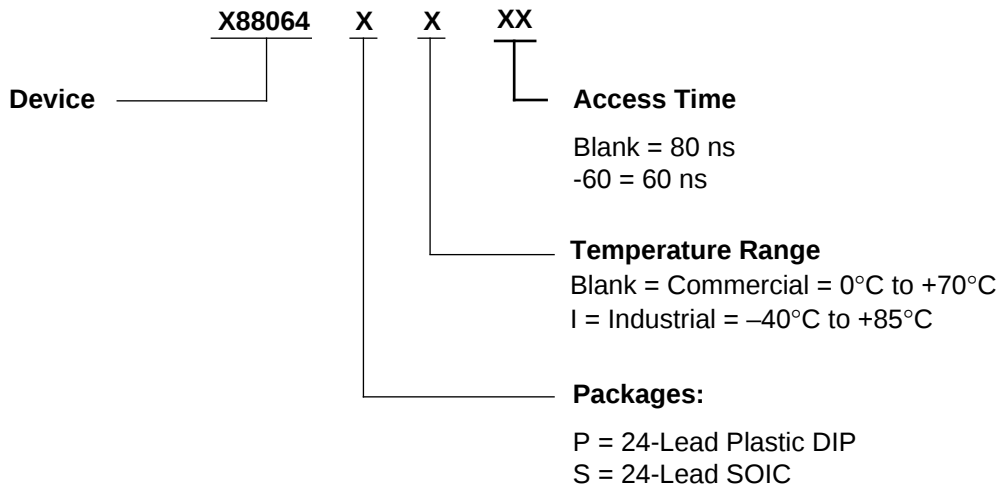
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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# X88064

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## ORDERING INFORMATION



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Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

### LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.