Low Noise, Picoampere Bias Current, JFET Input Op Amp

FEATURES

- **Input Bias Current, Warmed Up: 10pA Max**
- **100% Tested Low Voltage Noise: 8nV/√Hz Max**
- **A Grade 100% Temperature Tested**
- Offset Voltage Over Temp: 1mV Max
- Input Resistance: $10^{13}\Omega$
- Very Low Input Capacitance: 1.5pF
- Voltage Gain: 1 Million Min
- Gain-Bandwidth Product: 4.2MHz Typ
- Guaranteed Specifications with ±5V Supplies

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

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DESCRIPTION

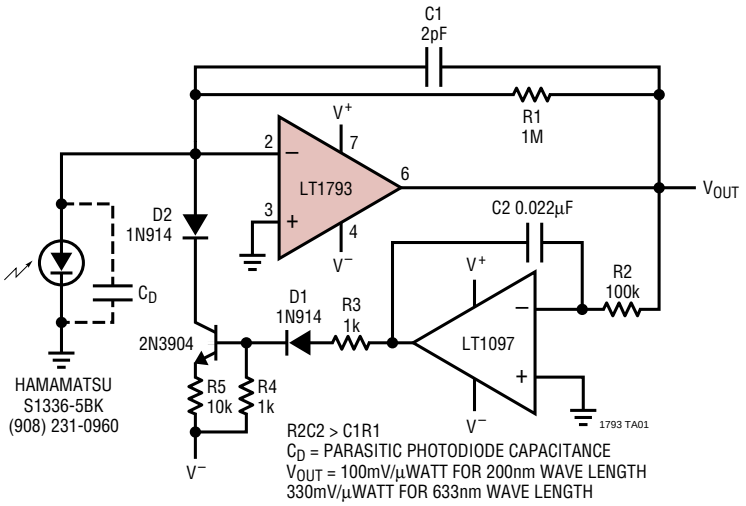
The LT®1793 achieves a new standard of excellence in noise performance for a JFET op amp. For the first time low voltage noise (6nV/√Hz) is simultaneously offered with extremely low current noise (0.8fA/√Hz), providing the lowest total noise for high impedance transducer applications. Unlike most JFET op amps, the very low input bias current (3pA typ) is maintained over the entire common mode range which results in an extremely high input resistance ($10^{13}\Omega$). When combined with a very low input capacitance (1.5pF) an extremely high input impedance results, making the LT1793 the first choice for amplifying low level signals from high impedance transducers. The low input capacitance also assures high gain linearity when buffering AC signals from high impedance transducers.

The LT1793 is unconditionally stable for gains of 1 or more, even with 1000pF capacitive loads. Other key features are 250µV V_{OS} and a voltage gain over 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate (3.4V/µs) and gain-bandwidth product (4.2MHz).

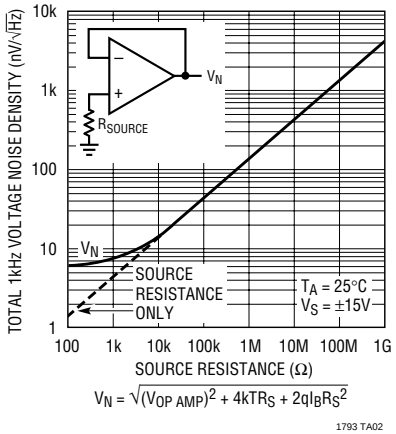
Specifications at ±5V supply operation are also provided. For an even lower voltage noise please see the LT1792 data sheet.

TYPICAL APPLICATION

Low Noise Light Sensor with DC Servo



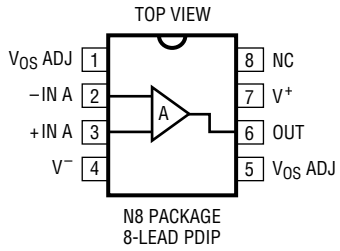
1kHz Output Voltage Noise Density vs Source Resistance



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range
  Commercial (Note 8) ..... –40°C to 85°C
  Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

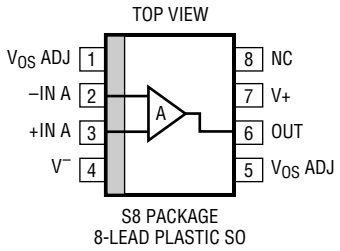


N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 80°C/W

ORDER PART NUMBER

LT1793ACN8
LT1793CN8
LT1793AIN8
LT1793IN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 160°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1793ACS8
LT1793CS8
LT1793AIS8
LT1793IS8

S8 PART MARKING

1793A 1793AI
1793 1793I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1793AC/LT1793AI MIN	LT1793AC/LT1793AI TYP	LT1793AC/LT1793AI MAX	LT1793C/LT1793I MIN	LT1793C/LT1793I TYP	LT1793C/LT1793I MAX	UNITS
V_{OS}	Input Offset Voltage			0.25	0.8		0.25	0.9	mV
		V_S = ±5V		0.45	1.4		0.45	1.6	mV
I_{OS}	Input Offset Current	Warmed Up (Note 3)		1.5	7		2.5	15	pA
		T_J = 25°C (Note 6)		0.5	2		0.7	4	pA
I_B	Input Bias Current	Warmed Up (Note 3)		3	10		4.0	20	pA
		T_J = 25°C (Note 6)		1	3		1.5	5	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		11.5			11.5		nV/√Hz
		f_O = 1000Hz		6	8		6	8	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1kHz (Note 4)		0.8			1		fA/√Hz
R_{IN}	Input Resistance								
	Differential Mode			10^{14}			10^{14}		Ω
	Common Mode	V_{CM} = –10V to 13V		10^{13}			10^{13}		Ω
C_{IN}	Input Capacitance			1.5			1.5		pF
		V_S = ±5V		2.0			2.0		pF
V_{CM}	Input Voltage Range (Note 5)		13.0	13.5		13.0	13.5		V
			–10.5	–11.0		–10.5	–11.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = –10V to 13V	83	102		81	96		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	85	98		83	95		dB

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1793AC/LT1793AI MIN	LT1793AC/LT1793AI TYP	LT1793AC/LT1793AI MAX	LT1793C/LT1793I MIN	LT1793C/LT1793I TYP	LT1793C/LT1793I MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k V_O = ±10V, R_L = 1k	1000 500	4500 3500		900 400	4400 3000		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k R_L = 1k	±13.0 ±12.0	±13.2 ±12.3		±13.0 ±12.0	±13.2 ±12.3		V V
SR	Slew Rate	$R_L \geq$ 2k (Note 7)	2.3	3.4		2.3	3.4		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	2.5	4.2		2.5	4.2		MHz
I_S	Supply Current	 V_S = ±5V		4.2 4.2	5.20 5.15		4.2 4.2	5.20 5.15	mA mA
	Offset Voltage Adjustment Range	R_{POT} (to V_{EE}) = 10k		13			13		mV

The ● denotes specifications which apply over the temperature range 0°C ≤ T_A ≤ 70°C, otherwise specifications are at T_A = 25°C. V_S = ±15V, V_{CM} = 0V, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1793AC MIN	LT1793AC TYP	LT1793AC MAX	LT1793C MIN	LT1793C TYP	LT1793C MAX	UNITS
V_{OS}	Input Offset Voltage	 V_S = ±5V	● ●		0.50 0.75	1.0 1.6		1.0 1.6	3.5 4.2	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		5	13		8	50	µV/°C
I_{OS}	Input Offset Current		●		15	100		20	130	pA
I_B	Input Bias Current		●		130	400		150	500	pA
V_{CM}	Input Voltage Range (Note 5)		● ●	12.9 –10.0	13.4 –10.8		12.9 –10.0	13.4 –10.8		V V
CMRR	Common Mode Rejection Ratio	V_{CM} = –10V to 12.9V	●	79	100		77	95		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±20V	●	83	97		81	94		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10k V_O = ±10V, R_L = 1k	● ●	900 500	3600 2600		800 400	3400 2400		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 10k R_L = 1k	● ●	±12.9 ±11.9	±13.2 ±12.15		±12.9 ±11.9	±13.2 ±12.15		V V
SR	Slew Rate	$R_L \geq$ 2k (Note 7)	●	2.2	3.3		2.2	3.3		V/µs
GBW	Gain-Bandwidth Product	f_O = 100kHz	●	2.2	3.3		2.2	3.3		MHz
I_S	Supply Current	 V_S = ±5V	● ●		4.2 4.2	5.30 5.25		4.2 4.2	5.30 5.25	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the temperature range $-40°C \le T_A \le 85°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted. (Notes 8, 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1793AC/LT1793AI MIN	LT1793AC/LT1793AI TYP	LT1793AC/LT1793AI MAX	LT1793C/LT1793I MIN	LT1793C/LT1793I TYP	LT1793C/LT1793I MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.65	1.3		1.6	4.8	mV
		$V_S = \pm5V$	●		1.00	1.9		2.0	5.5	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 6)	●		5	13		9	50	µV/°C
I_{OS}	Input Offset Current		●		80	300		100	400	pA
I_B	Input Bias Current		●		700	2400		800	3000	pA
V_{CM}	Input Voltage Range (Note 5)		●	12.6	13.0		12.6	13.0		V
			●	–10.0	–10.5		–10.0	–10.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10V$ to 12.6V	●	78	99		76	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm20V$	●	81	96		79	93		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k$	●	850	3300		750	3000		V/mV
		$V_O = \pm10V$, $R_L = 1k$	●	400	2200		300	2000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±12.8	±13.1		±12.8	±13.1		V
		$R_L = 1k$	●	±11.8	±12.1		±11.8	±12.1		V
SR	Slew Rate	$R_L \ge 2k$	●	2.1	3.2		2.1	3.2		V/µs
GBW	Gain-Bandwidth Product	$f_O = 100kHz$	●	2	3.1		2	3.1		MHz
I_S	Supply Current		●		4.2	5.40		4.2	5.40	mA
		$V_S = \pm5V$	●		4.2	5.35		4.2	5.35	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers.

Note 3: I_B and I_{OS} readings are extrapolated to a warmed-up temperature from 25°C measurements and 32°C characterization data.

Note 4: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \bullet 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 5: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade) to 2.8mV (C grade).

Note 6: This parameter is not 100% tested.

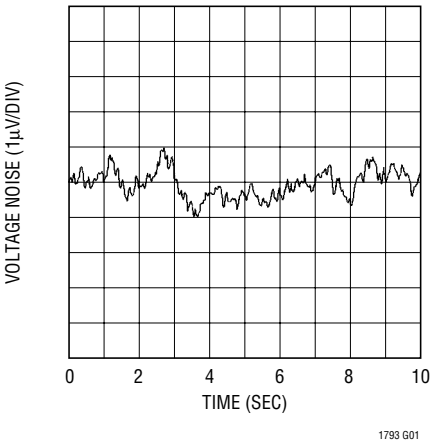
Note 7: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

Note 8: The LT1793AC and LT1793C are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at –40°C and 85°C. The LT1793I is guaranteed to meet the extended temperature limits. The LT1793AC and LT1793AI grade are 100% temperature tested for the specified temperature range.

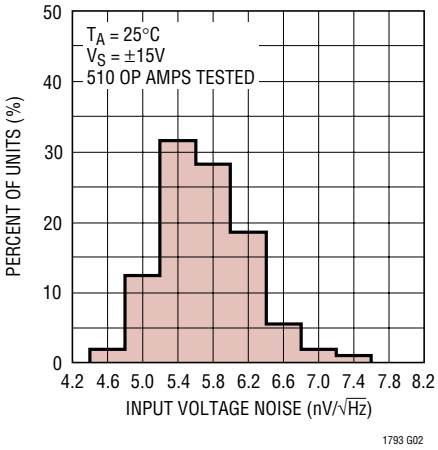
Note 9: The LT1793 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

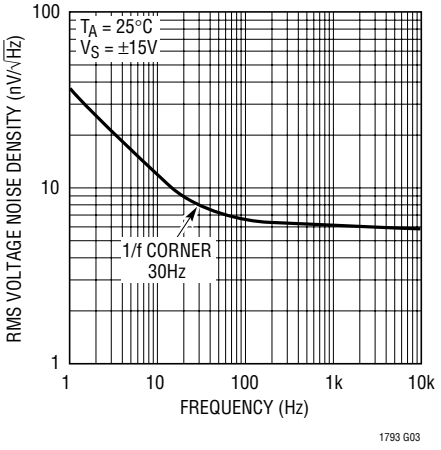
0.1Hz to 10Hz Voltage Noise



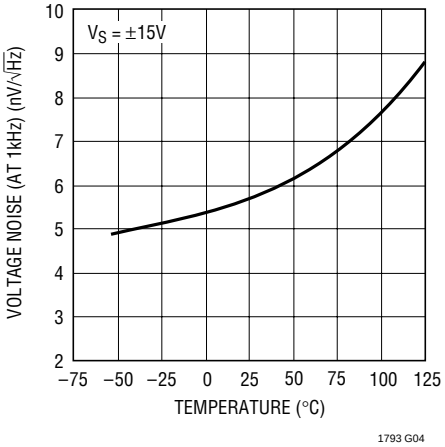
1kHz Input Noise Voltage Distribution



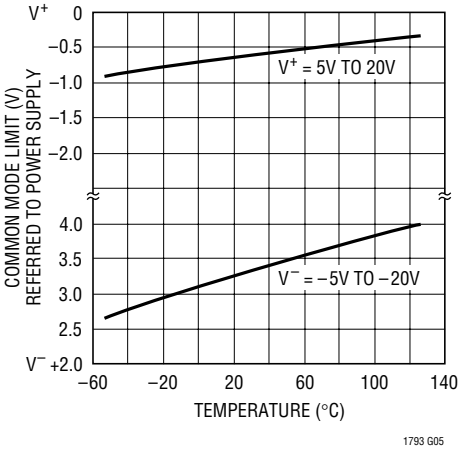
Voltage Noise vs Frequency



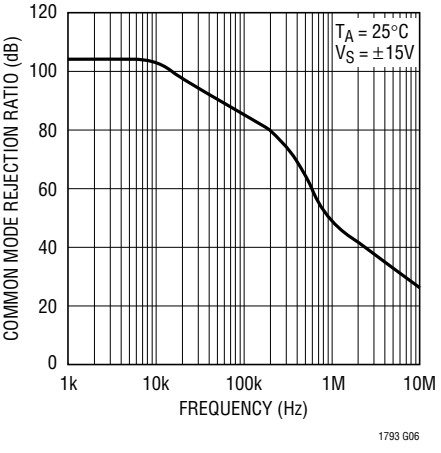
Voltage Noise vs Chip Temperature



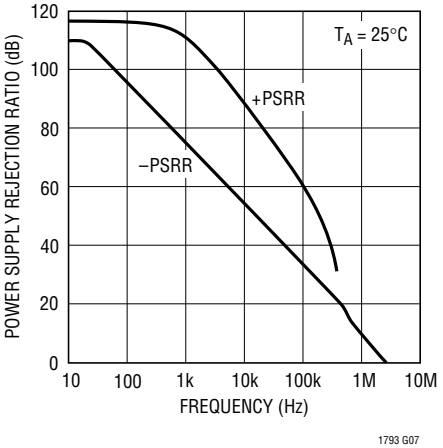
Common Mode Limit vs Temperature



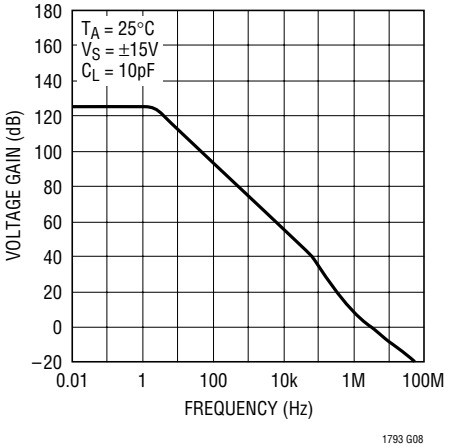
Common Mode Rejection Ratio vs Frequency



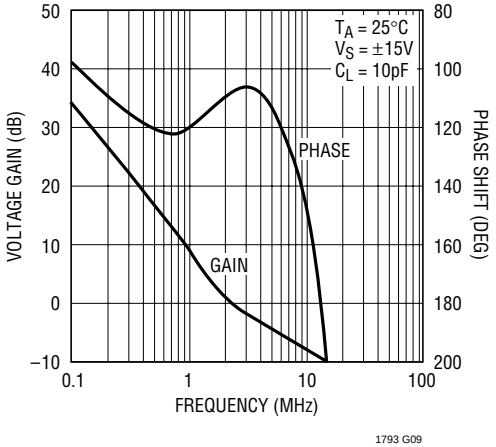
Power Supply Rejection Ratio vs Frequency



Voltage Gain vs Frequency

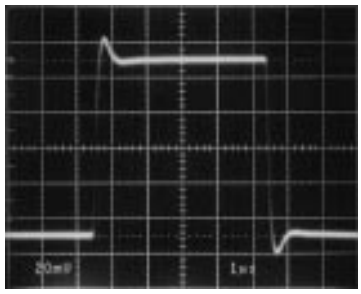


Gain and Phase Shift vs Frequency



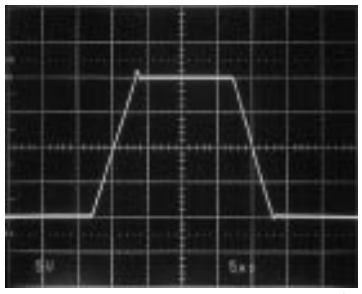
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response



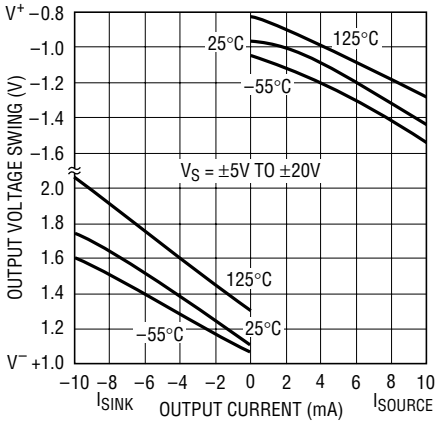
$A_V = 1$ 1µs/DIV
$C_L = 10pF$
$V_S = \pm15V, \pm5V$

Large-Signal Transient Response

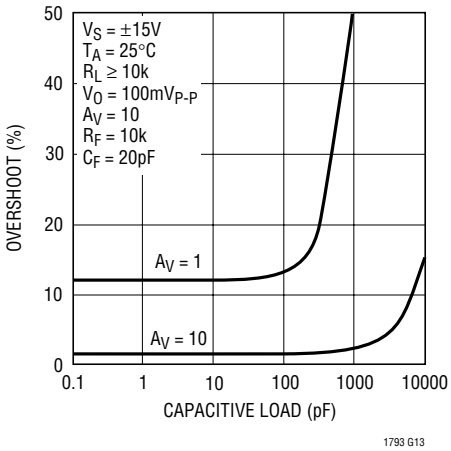


$A_V = 1$ 5µs/DIV
$C_L = 10pF$
$R_L = 2k$
$V_S = \pm15V$

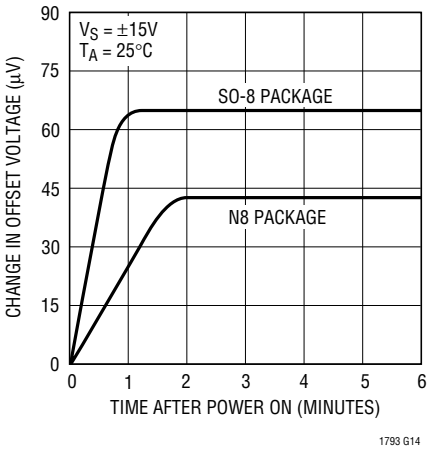
Output Voltage Swing vs Load Current



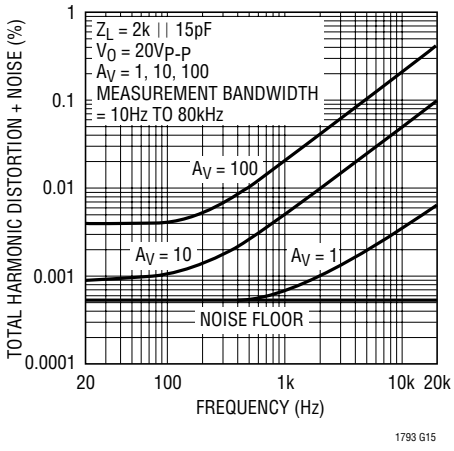
Capacitive Load Handling



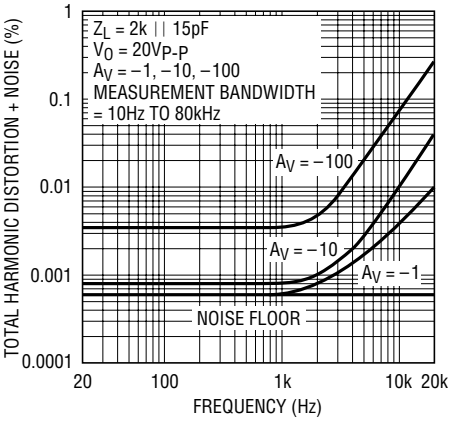
Warm-Up Drift



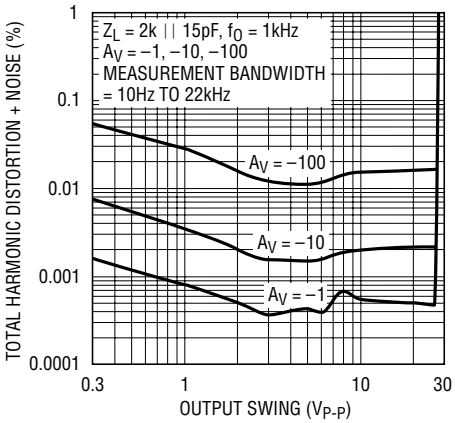
THD and Noise Frequency for Noninverting Gain



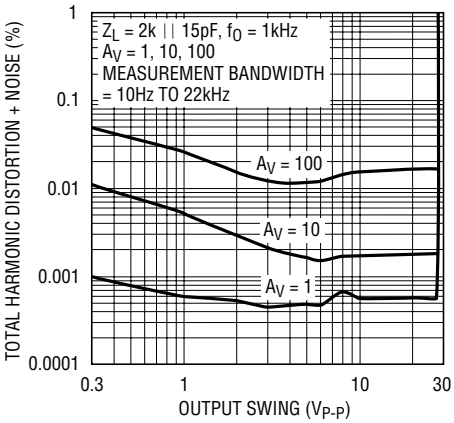
THD and Noise vs Frequency for Inverting Gain



THD and Noise vs Output Amplitude for Inverting Gain

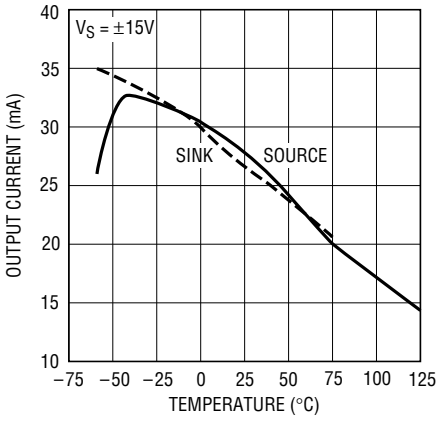


THD and Noise vs Output Amplitude for Noninverting Gain



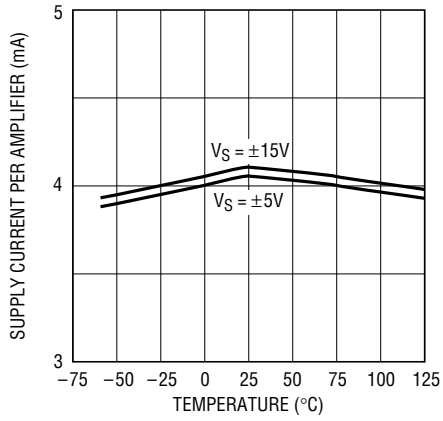
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Output Current vs Temperature



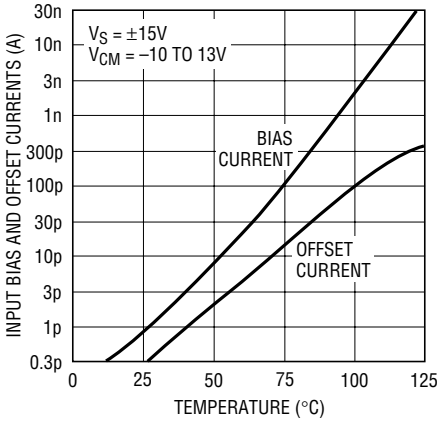
1793 G19

Supply Current vs Temperature



1793 G20

Input Bias and Offset Currents vs Chip Temperature

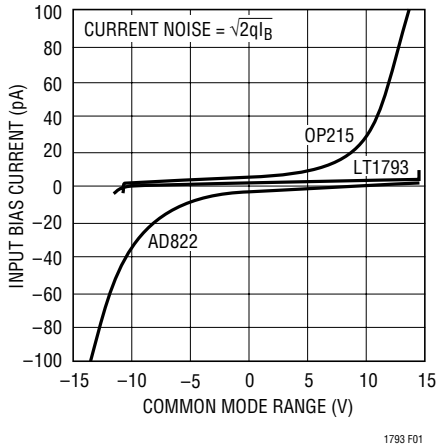


1793 G21

APPLICATIONS INFORMATION

LT1793 vs the Competition

With improved noise performance, the LT1793 in the PDIP directly replaces such JFET op amps as the OPA111 and the AD645. The combination of low current and voltage noise of the LT1793 allows it to surpass most dual and single JFET op amps. The LT1793 can replace many of the lowest noise bipolar amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps (with higher current noise) will eventually lose out to the LT1793 when transducer impedance increases.

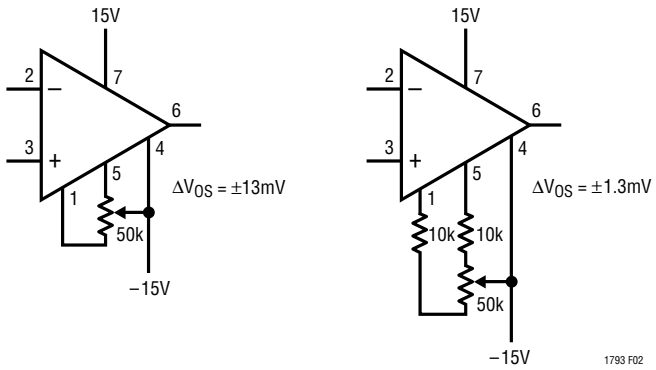


1793 F01

Figure 1. Comparison of LT1793, OP215, and AD822 Input Bias Current vs Common Mode Range

The extremely high input impedance ($10^{13}\Omega$) assures that the input bias current is almost constant over the entire common mode range. Figure 1 shows how the LT1793 stands up to the competition. Unlike the competition, as the input voltage is swept across the entire common mode range the input bias current of the LT1793 hardly changes. As a result the current noise does not degrade. This makes the LT1793 the best choice in applications where an amplifier has to buffer signals from a high impedance transducer.

Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the negative supply (Figure 2a). No appreciable change in offset voltage drift



1793 F02

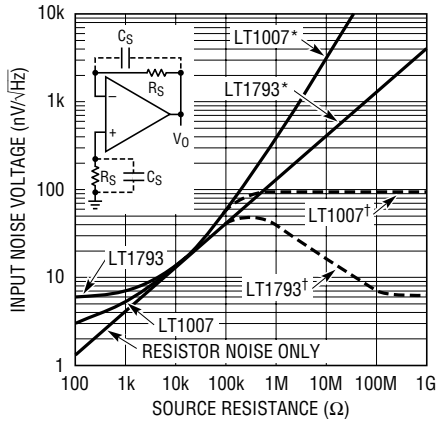
Figure 2

APPLICATIONS INFORMATION

with temperature will occur when the device is nulled with a potentiometer ranging from 10k to 200k. Finer adjustments can be made with resistors in series with the potentiometer (Figure 2b).

Amplifying Signals from High Impedance Transducers

The low voltage and current noise offered by the LT1793 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers and photodiodes. The total output noise in such a system is the gain times the RMS sum of the op amp's input referred voltage noise, the thermal noise of the transducer, and the op amp's input bias current noise times the transducer impedance. Figure 3 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1793 is superior to most JFET op amps. Only the lowest noise bipolar op amps have the advantage at low source resistances. As the source resistance increases from 5k to 50k, the LT1793 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_BR^2$) will eventually dominate the total noise. At these high source resistances, the LT1793 will out perform the lowest noise bipolar op amps due to the inherently low current noise of FET input op amps. Clearly, the LT1793 will extend the range of high impedance transducers that can be used for high signal-to-noise ratios. This makes the LT1793 the best choice for high impedance, capacitive transducers.



SOURCE RESISTANCE = $2R_S = R$
* PLUS RESISTOR
† PLUS RESISTOR || 1000pF CAPACITOR

$$V_n = A_V\sqrt{V_n^2{}_{(OP\ AMP)} + 4kTR + 2qI_BR^2}$$

Figure 3. Comparison of LT1793 and LT1007 Total Output 1kHz Voltage Noise vs Source Resistance

Optimization Techniques for Charge Amplifiers

The high input impedance JFET front end makes the LT1793 suitable in applications where very high charge sensitivity is required. Figure 4 illustrates the LT1793 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; the gain depends on the principal of charge conservation at the input of the LT1793. The charge across the transducer capacitance C_S is transferred to the feedback capacitor C_F

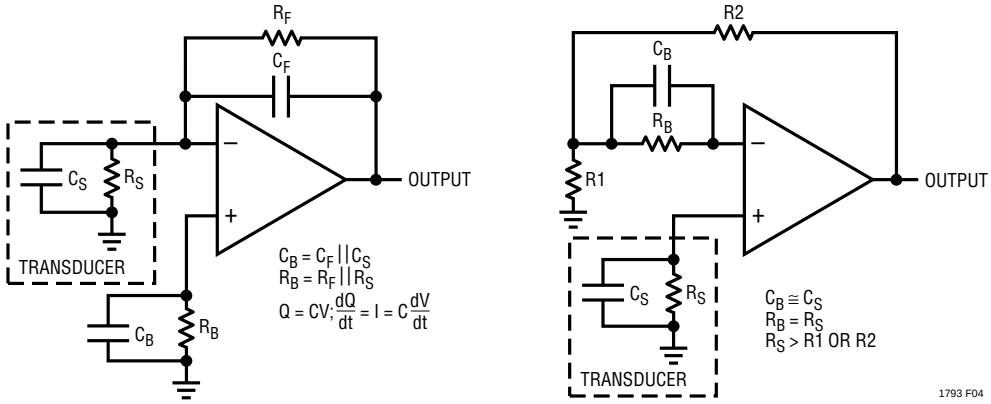


Figure 4. Inverting and Noninverting Gain Configurations

APPLICATIONS INFORMATION

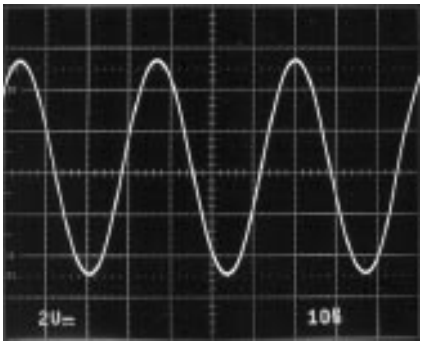
resulting in a change in voltage dV, which is equal to dQ/C_F. The gain therefore is C_F/C_S. For unity-gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1793 and R_F should equal R_S.

In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance, C_S. This voltage is then buffered by the LT1793 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors at higher temperature, especially with transducer resistances of up to 1000M or more. The optimum value for R_B is determined by equating the thermal noise ($4kTR_S$) to the current noise ($2qI_B$) times R_S^2. Solving for R_S results in $R_B = R_S = 2V_T/I_B$ (V_T = 26mV at 25°C). A parallel capacitor C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

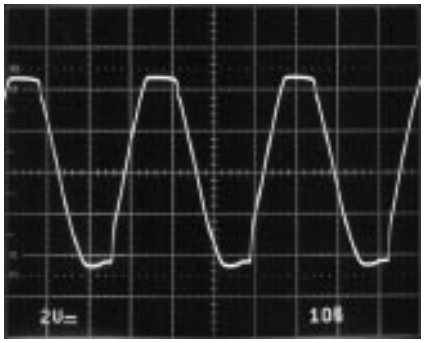
To take full advantage of a wide input common mode range, the LT1793 was designed to eliminate phase reversal. Referring to the photographs in Figure 5, the LT1793 is shown operating in the follower mode (A_V = 1) at ±5V supplies with the input swinging ±5.2V. The output of the LT1793 clips cleanly and recovers with no phase reversal. This has the benefit of preventing lockup in servo systems and minimizing distortion components.

Input: ±5.2V Sine Wave



LT1793 F05a

LT1793 Output



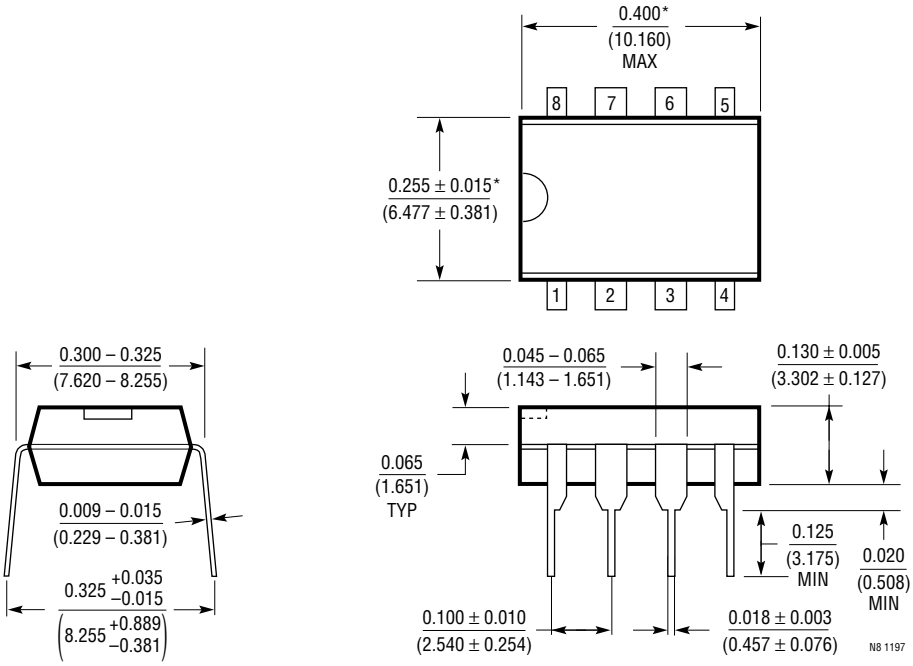
LT1793 F05b

Figure 5. Voltage Follower with Input Exceeding the Common Mode Range (V_S = ±5V)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

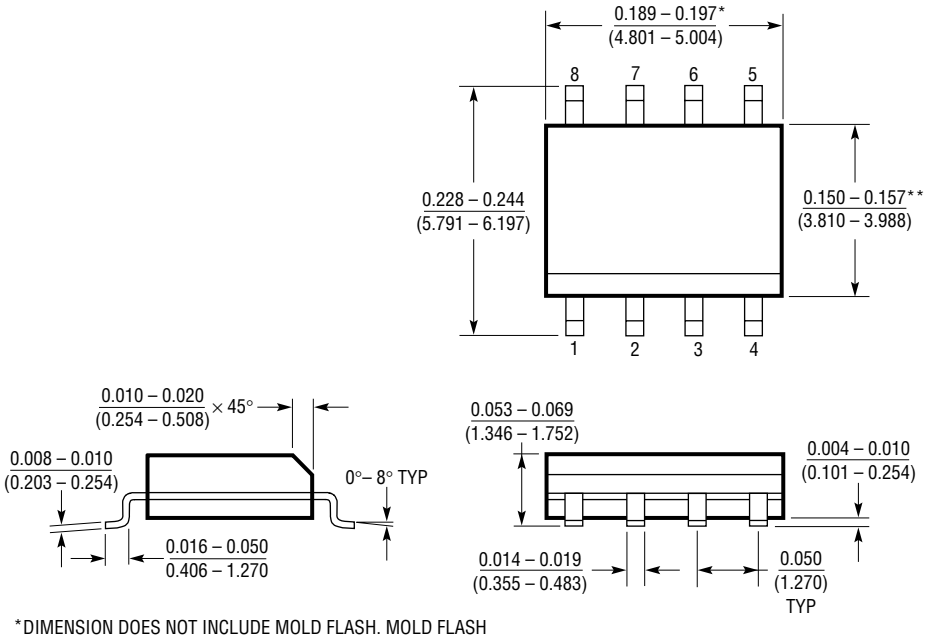


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

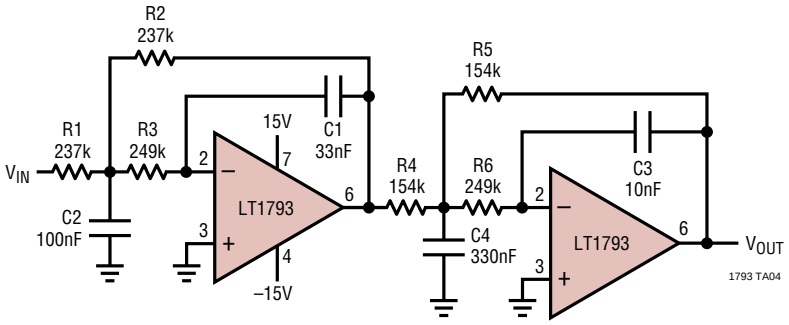
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

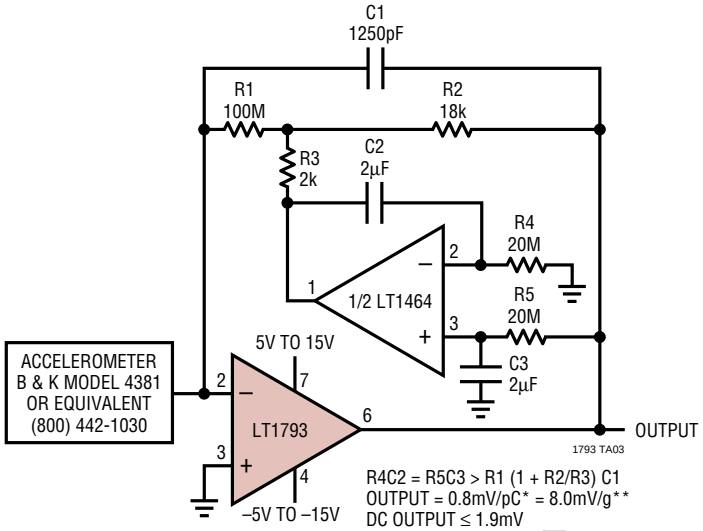
TYPICAL APPLICATIONS

10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)



TYPICAL OFFSET ≈ 0.8mV
1% TOLERANCES
FOR V_{IN} = 10V_{P-P}, V_{OUT} = –121dB AT f > 330Hz
= – 6dB AT f = 16.3Hz
LOWER RESISTOR VALUES WILL RESULT IN LOWER THERMAL NOISE AND LARGER CAPACITORS

Accelerometer Amplifier with DC Servo



R4C2 = R5C3 > R1 (1 + R2/R3) C1
OUTPUT = 0.8mV/pC* = 8.0mV/g**
DC OUTPUT ≤ 1.9mV
OUTPUT NOISE = 8nV/√Hz AT 1kHz

*PICOCOULOMBS
**g = EARTH'S GRAVITATIONAL CONSTANT

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1113	Low Noise, Dual JFET Op Amp	Dual Version of LT1792, V_{NOISE} = 4.5nV/√Hz
LT1169	Low Noise, Dual JFET Op Amp	Dual Version of LT1793, V_{NOISE} = 6nV/√Hz, I_B = 10pA
LT1467	Micropower Dual JFET Op Amp	1MHz, 2pA Max I_B, 200µA Max I_S
LT1792	Low Noise, Single JFET Op Amp	Lower V_{NOISE} Version of LT1793, V_{NOISE} = 4.2nV/√Hz

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