Datasheet Explanation Update

for Infineon's Automotive MOSFETs

About this document

Scope and purpose

The latest datasheets for Infineon's mid-voltage (from 40V up to 100V) Automotive MOSFETs are generated with a new template. Along with the datasheet template update, some parameters are specified with a new format. This application note explains the definition of parameters and related plots in the datasheet. Together with published application notes listed in the reference section, this will help engineers who design automotive applications read and understand the datasheet properly to select the right product for their applications.

Intended audience

Design engineers for automotive applications

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1 Introduction

Power MOSFETs are widely used for a variety of automotive applications. Infineon offers a broad portfolio of high power automotive MOSFETs. Application designers can select the device which best meets the application's requirements by using product datasheets. The datasheet is one of the most important resources to help the designer because of the detailed technical product information it contains about the MOSFET. However, sometimes, the datasheet is deemed to be too complicated because of the great amount of information it contains in such a condensed format. This application note will help overcome that perception by providing general guidance to help read and understand the datasheet and its contents. Each datasheet specification parameter and diagram is explained in detail.

The goal of this application note is to help improve the reader's comprehension of the parameters and diagrams in the datasheet. This will result in a more thorough understanding of MOSFETs and their behavior by application designers and help them better determine operational limits of these devices. This will also help application designers more effectively compare different MOSFETs and select the best one for their application.

Infineon's website contains several other application notes on a variety of topics, including design guidelines for MOSFETs. [1]

2 Datasheet Parameters in New Datasheet Template

MOSFET datasheet consists of specifications of electric parameters in table format as well as specific characteristics in diagrams. In this chapter, each parameter with related plots is explained separately. Format of the parameters described in this chapter is based on the latest datasheet template. For existing datasheets with legacy template, please refer to the appropriate application note available on Infineon web site. [2]

2.1 Power Dissipation

This parameter expresses the maximum allowable power dissipation over the case temperature and it can be calculated by the following equation.

$$(1)\quad P_{tot}(T_C) = \frac{T_J - T_C}{R_{thJC}}$$

The power dissipation P_{tot} is related to junction-to-case thermal resistance R_{thJC} which is material and dimension dependent. With increasing case temperature, the maximum allowable power dissipation decreases as illustrated in the diagram in the datasheet.

Power dissipation	P_{tot}	T_C=25 °C	71	W

Figure 1 Maximum rating for P_{tot}

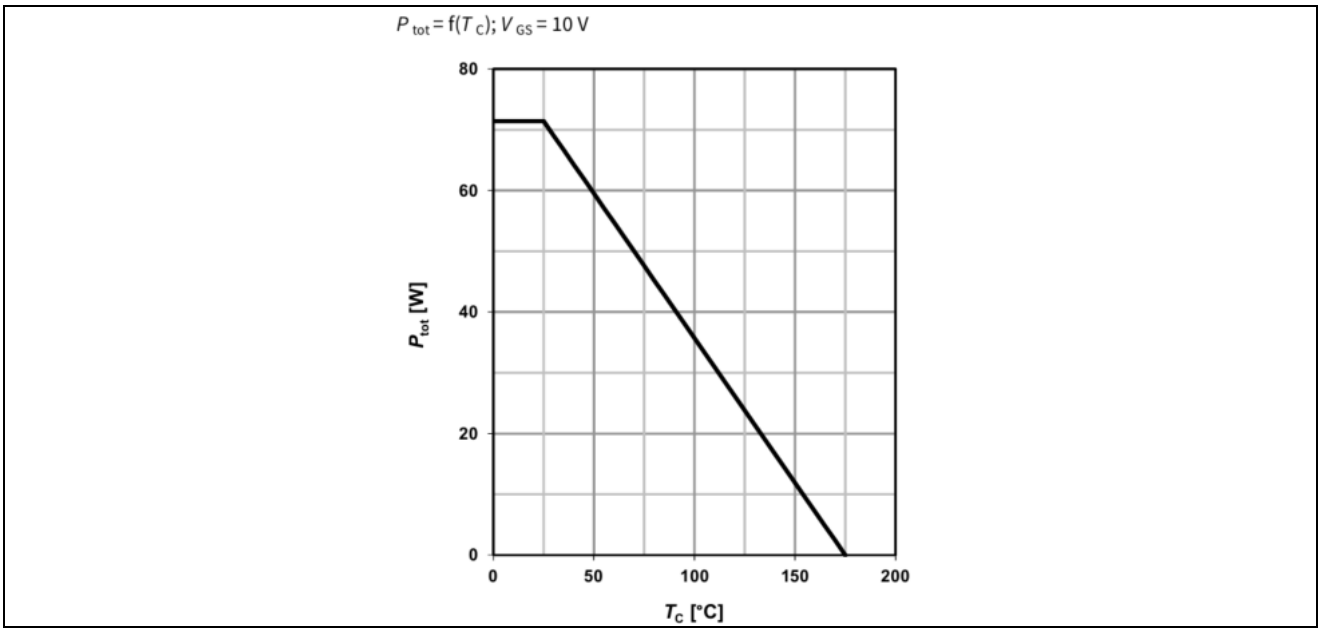


Figure 2 Maximum power dissipation P_{tot}=f(T_C)

2.2 Drain Current

The continuous Drain current I_D is the maximum current which can flow via the device without exceeding any thermal boundary conditions. There are two limitations for the I_D rating – one is maximum allowed junction temperature and the other is the package current limit coming from Source contact to substrate material or interconnect. The maximum drain current at a given case temperature can be calculated by the following formula under the function of T_J (junction temperature), T_C (case temperature), R_{thJC} (junction-to-case thermal resistance) and $R_{DS(on)_TJ(max)}$ (maximum on-state resistance at maximum junction temperature):

$$(2)\quad I_D(T_C) = \sqrt{\frac{\frac{T_J - T_C}{R_{thJC}}}{R_{DS(on)_TJ(max)}}}$$

In the latest MOSFET datasheet with new template, maximum Drain current I_D is specified under three different conditions as shown in Figure 3.

Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1,2]	90	A
		V_{GS}=10V, DC current[3]	40	
		T_a=85 °C, V_{GS}=10 V, R_{thJA} on 2s2p[2,4]	12	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	252	

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

[2] The parameter is not subject to production testing – specified by design.

[3] Current is limited by the package.

[4] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Figure 3 Maximum Drain current (I_D and $I_{D,pulse}$)

First rating is the chip limited current, which is the calculated theoretical maximum rating as described by equation (2) above. The current is limited by maximum junction temperature at given case temperature (25°C unless otherwise specified) based on the thermal impedance from junction to case and the maximum $R_{DS(on)}$ at $T_{J(max)}$. This would be useful to show device performance of combined on-state resistance $R_{DS(on)}$ and R_{thJC} as figure of merit, however, it is not practical rating because case temperature T_C will not stay constant based on conditions in the actual applications.

The second rating is the DC current rating which represents the maximum tested current during manufacturing. This limitation comes from testing process in production, Source contact to substrate due to electromigration or interconnect such as bond wire or copper clip on Source as described in the beginning. The corresponding footnote explains which type of limit is relevant for the specific product. It should be noted that if the limit is related to test capability, then the actual limit in the application can be calculated by equation (2) above, as long as it is lower than the chip limitation. If the chip limited current rating is lower than this DC current rating, then the DC current limit will be same as the chip limited current.

The third rating is the called application based current rating based on a standard R_{thJA} from a JEDEC reference PCB. This suggests more practical rating under the described conditions, however, the R_{thJA} depends on external environment such as layout design, substrate material, thermal interface material, heatsink design, etc., and the R_{thJA} in a particular can be lower that the JEDEC standard PCB resulting in a higher current capability. As stated above, the maximum current in an application can be determined from equation (2). The application current rating stated in the datasheet is provided as an indication. It is recommended to check the rating conditions especially when comparing different devices from different suppliers.

The pulsed Drain current limit $I_{D,pulse}$, is relevant at pulse width t_p which is specified in addition to case temperature T_C. Therefore, the rating can be calculated using equation (2) above by applying thermal impedance Z_{thJC} extracted from thermal impedance plot on datasheet instead of R_{thJA}. Since thermal impact to case temperature T_C under a short period of time (typically below 1ms) is minimal, T_C can be considered constant for $I_{D,pulse}$.

The plot for I_D over T_C in the latest datasheet also follows the new I_D rating format as seen in the Figure 4 below.

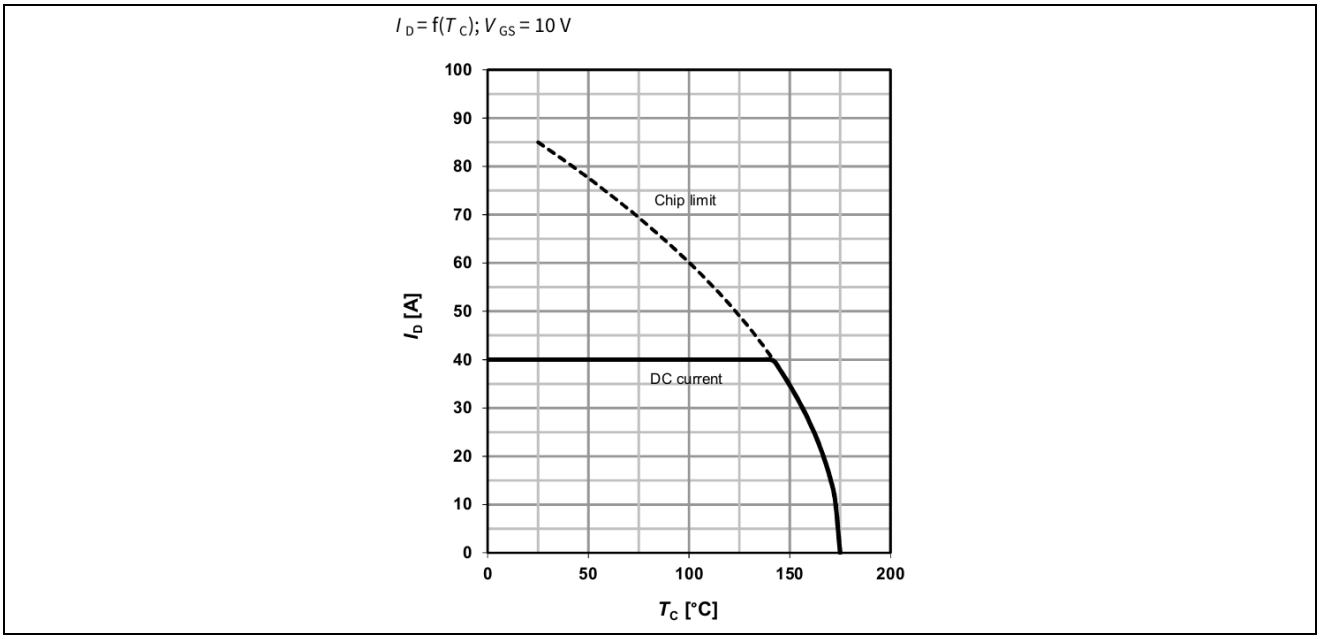


Figure 4 Maximum Drain current $I_D = f(T_C)$

2.3 Safe Operating Area

Figure 5 shows the maximum allowable Drain current I_D as a function of the Drain-Source voltage V_{DS} with different pulse widths. There are several limitations in the diagram as follows:

a) Top line is defined by a maximum pulsed Drain current $I_{D,pulse}$.

b) This area is limited by maximum on-state resistance $R_{DS(On)}$ at maximum junction temperature

c) At fixed T_C, the device is limited by the constant power line in this region. Depending on the applied power pulse width, maximum allowable power loss changes are related to thermal impedance. For a given pulse width, the thermal impedance Z_{thJC} can be obtained from maximum transient thermal impedance diagram, which will be described in section 2.4

$$(3)\quad I_D(V_{DS}) = \frac{T_J - T_C}{V_{DS} * Z_{thJC}}$$

d) In linear mode operation there is a risk of forming hot spots at low Gate-Source voltage due to the potential for thermal runaway. This effect is becoming more critical on the latest MOSFET technologies which have high current densities in the region where the zero temperature coefficient point of the transfer characteristic is shifted to higher Drain current. In order to consider the hot spot effect for higher V_{DS} and longer pulse width, derating is applied to the SOA diagram in this region.
Please refer to additional application note available on Infineon web site that discusses this topic in detail. [3]

e) The maximum breakdown voltage $V_{(BR)DSS}$ of the MOSFET defines the max V_{DS} limit in the SOA diagram

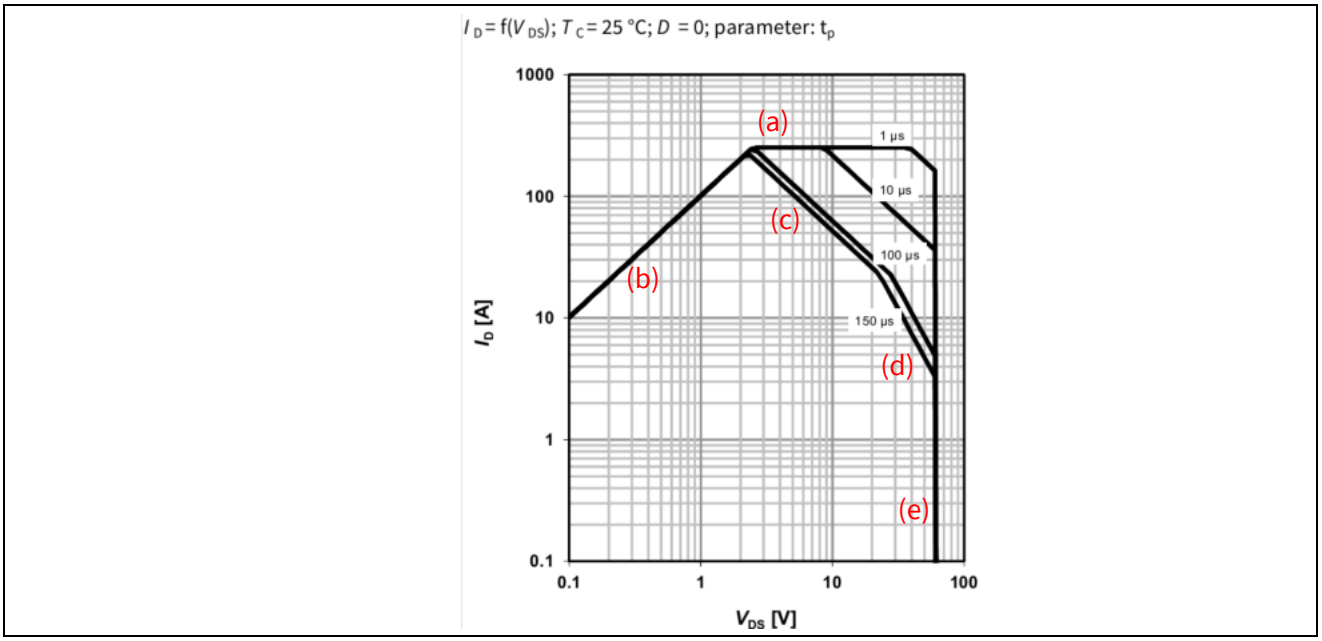


Figure 5 Safe Operating Area $I_D = f(V_{DS})$

2.4 Thermal characteristics

The R_{thJC} is the thermal resistance from the junction of the chip to the outside of the device, normally exposed pad unless otherwise specified. This is defined by the MOSFET itself (chip, package, and internal interconnects). The R_{thJA} is the application dependent thermal resistance from junction to the ambient. The R_{thJA} consists of the R_{thJC} mentioned above and thermal resistance between MOSFET case to ambient which includes all external components and the environment. Under normal operation, heat is generated by the power loss in the device and thermal resistance R_{thJC} and R_{thJA} describe how efficiently heat in the MOSFET die is transferred to the ambient temperature.

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	2.1	K/W
Thermal resistance, junction - ambient[4)]	R_{thJA}	–	–	61.8	–	

[2)] The parameter is not subject to production testing – specified by design.

[4)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Figure 6 Thermal characteristics R_{thJC} and R_{thJA}

In the latest MOSFET datasheet template, R_{thJA} is revised from the legacy 6cm² cooling area-based specification. Since the R_{thJA} conditions as stated in footnote is closer to actual use case, it suggests better idea on thermal performance of the device in the applications when compared to the legacy specification. It should be noted that the JEDEC PCB is a 4 layer PCB with two 2oz. layers and two 1oz. layers. A well designed PCB for a given application can achieve a much lower R_{thJA}, but as every design is different it cannot be specified here.

The transient junction-to-case thermal impedance Z_{thJC} takes the heat capacity C_{thJC} of the device into account. It can be used to estimate temperature raise caused by transient power losses. Depending on the pulse width t_P and the duty cycle $D = t_P/T$, thermal resistance varies over a wide range and its behavior is specified as a diagram in the datasheet as seen in Figure 7. The junction temperature increase can be calculated by the following equation (4). $T_{J,start}$ is equal to T_C at thermal equilibrium before the power pulse is applied.

$$(4)\quad T_J = T_{J,start} + P_{tot} * Z_{thJC}(t_P, D)$$

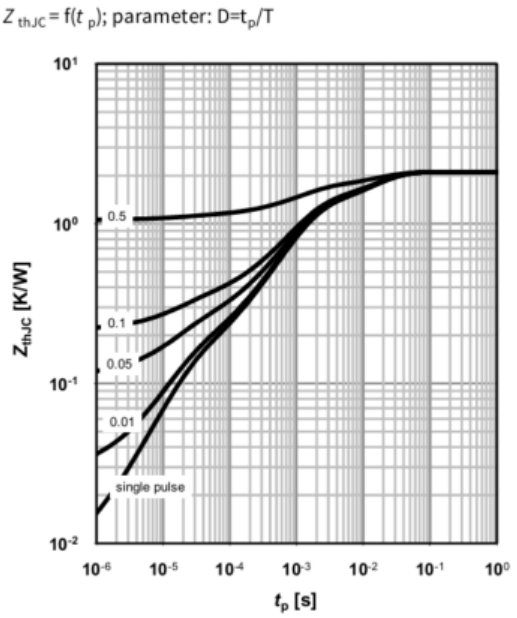


Figure 7 Maximum transient thermal impedance $Z_{thJC}=f(t_p)$

2.5 Typical Output Characteristics and Maximum Gate-Source Voltage

The typical output characteristic is illustrated by the Drain current I_D as a function of the Drain-Source voltage V_{DS} at given Gate-Source voltages V_{GS} under specified device junction temperature.
The device should be operated in the ohmic region to consider efficiency. There is a region that the drain current I_D saturates beyond the ohmic region at any given V_{GS}. As the operating point goes into the saturation region, any further I_D increase requires a massive V_{DS} rise, which will lead to conduction loss increase. In this case, the device may fail if the power dissipation is not limited.
As seen in the diagram, V_{GS} determines the output characteristic of the device. The maximum allowable range for V_{GS} is also specified.

Gate source voltage	V_{GS}	–	±16	V

Figure 8 Maximum Rating for V_{GS}

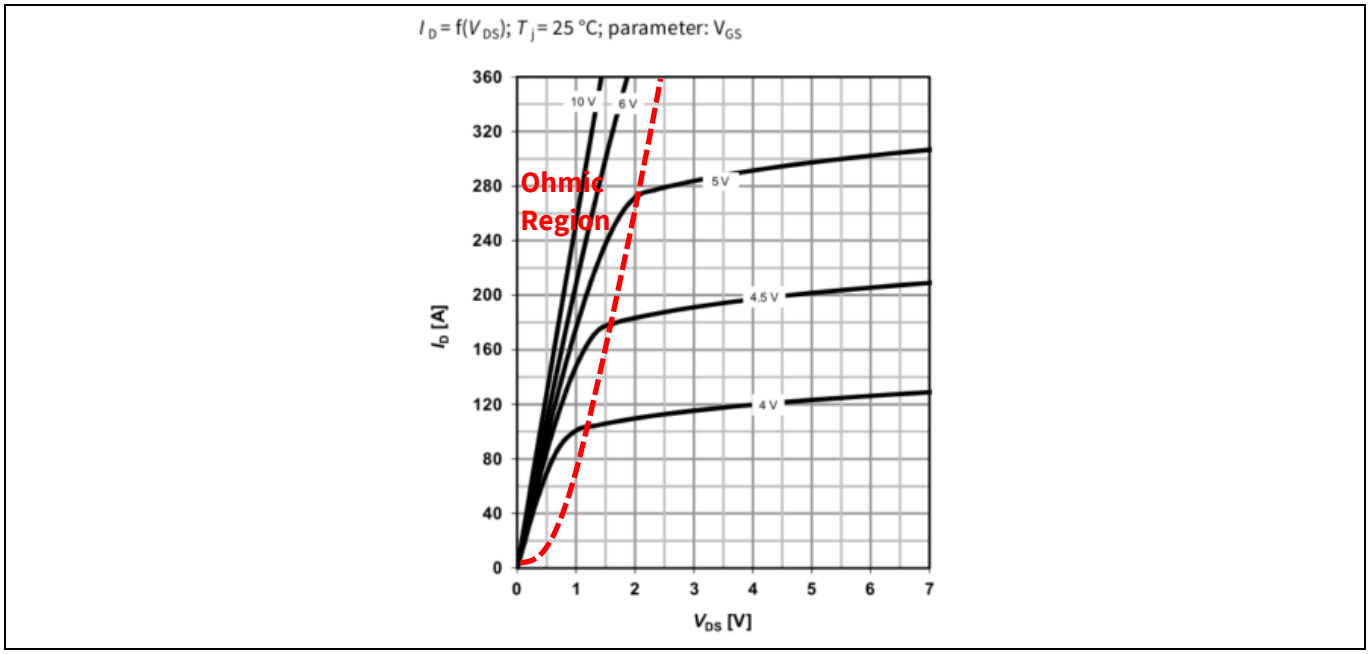


Figure 9 Typical Output Characteristics $I_D=f(V_{DS})$

2.6 Drain-Source ON-state Resistance as a function of Drain Current

The Drain-Source ON-state resistance $R_{DS(on)}$ over Drain current I_D at given Gate-Source voltage V_{GS} can be calculated from typical output characteristic diagram shown in Figure 9 using Ohm's Law.

$$(5)\quad R_{DS(on)}(I_D) = \frac{V_{DS}}{I_D}$$

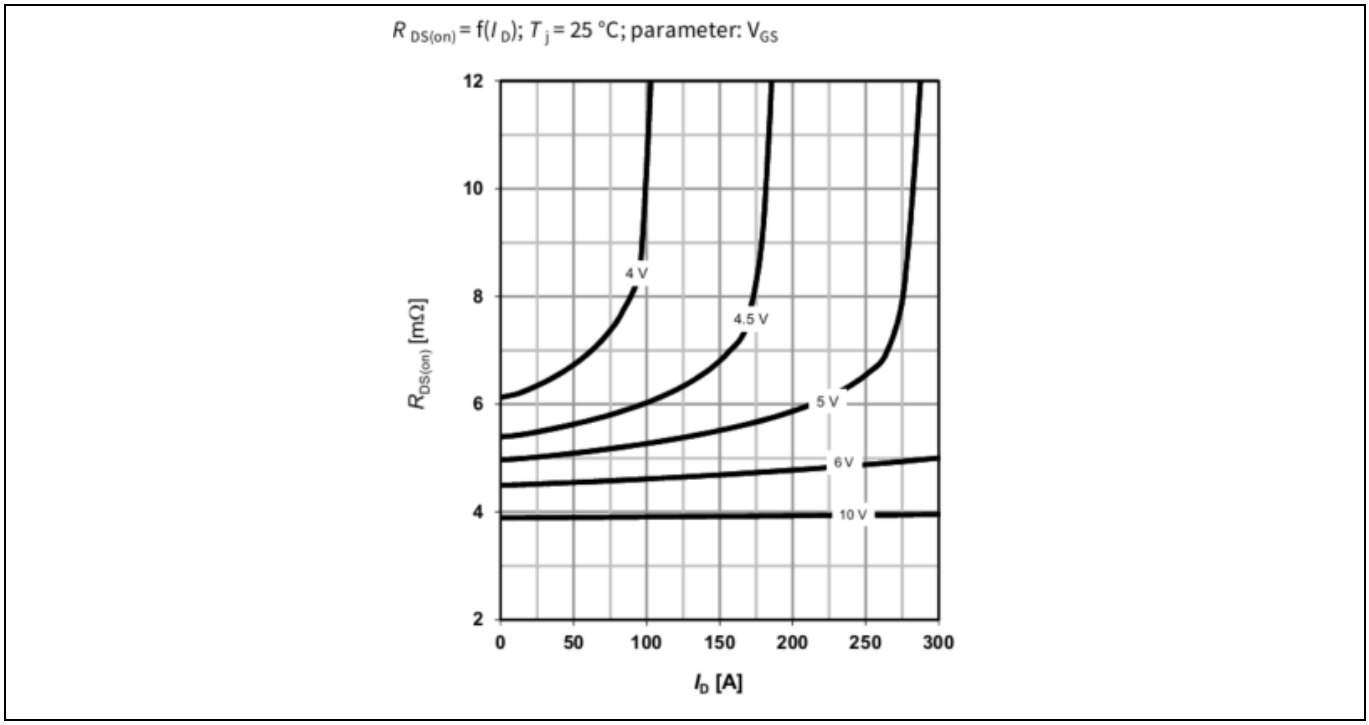


Figure 10 Typical Drain-Source ON-sate Resistance $R_{DS(on)}=f(I_D)$

2.7 Transfer Characteristics

The typical transfer characteristic of the device is illustrated by the diagram with the Drain current I_D as a function of Gate-Source voltage V_{GS} under the given junction temperature conditions and Drain-Source voltage V_{DS}. It is observed that all the curves are intersecting at one point, which is called the temperature stable operating point.

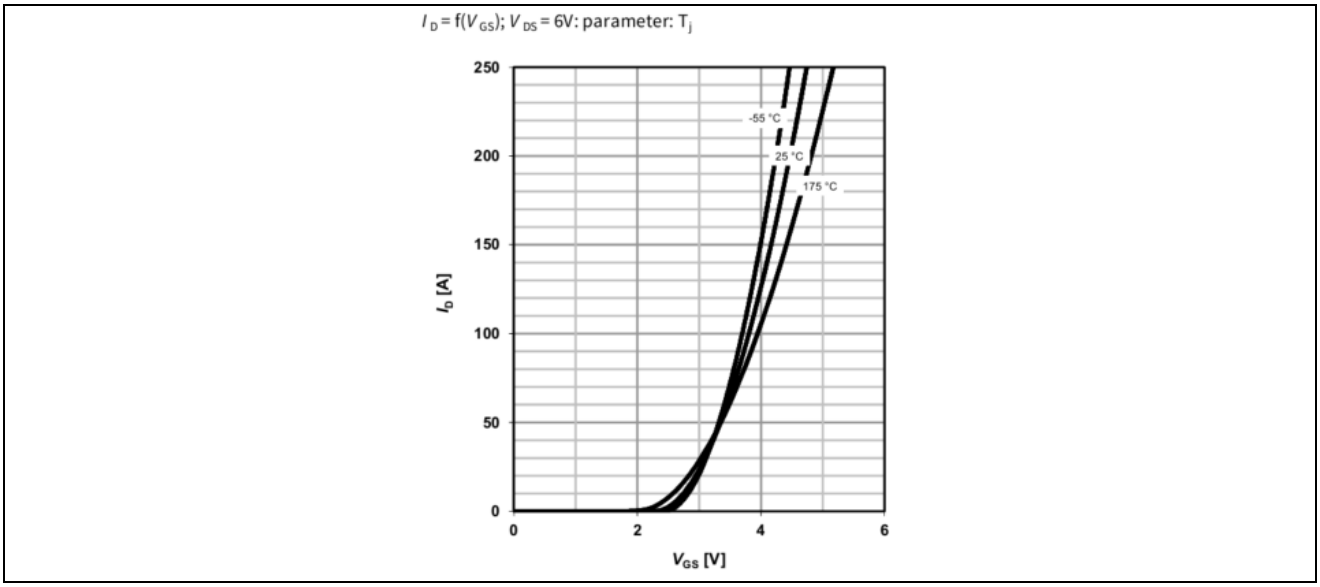


Figure 11 Typical Transfer Characteristics $I_D = f(V_{GS})$

The device will operate with a positive temperature coefficient until V_{GS} reaches the temperature stable operating point, which means that I_D increases as the junction temperature T_J increases. Extended MOSFET operation within this region should be avoided because there is potential to fail due to thermal runaway. Once V_{GS} exceeds the temperature stable operating point, the device will operate with a negative temperature coefficient. In this region, the device is stable since I_D decreases as T_J increases. Operating a MOSFET within this region is generally recommended as long as T_J is within the maximum allowable temperature.
Minimum or maximum rating of this characteristic can be estimated by shifting the plots in parallel according to Gate threshold voltage window.

2.8 Drain-Source ON-state Resistance

The Drain-Source ON-state resistance $R_{DS(on)}$ is one of the key parameters for the MOSFET. It specifies the resistance of the MOSFET when the part is turned on at a defined Gate-Source voltage V_{GS}, Drain current I_D and junction temperature T_J. This parameter is 100% tested in production under the specified conditions.

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=7V, I_D=100A	-	0.54	0.70	mΩ
		V_{GS}=10V, I_D=100A	-	0.47	0.64	

Figure 12 Drain to Source on-state resistance $R_{DS(ON)}$

In addition to the table, the data sheet contains a diagram of $R_{DS(on)}$ as a function of T_J. As can be seen in figure 13, the $R_{DS(on)}$ has a positive temperature coefficient and therefore increases with T_J. It is important that this effect is considered in any power loss calculation.
To calculate the dependency of the junction temperature, the equation (6) below can be used. The parameter α is a technology related constant which can be approximated as 0.4 for mid voltage Power MOSFETs.

$$(6)\quad R_{DSon}(T_J) = R_{DS(on),25℃} \cdot (1 + \frac{\alpha}{100})^{T_J - 25℃}$$

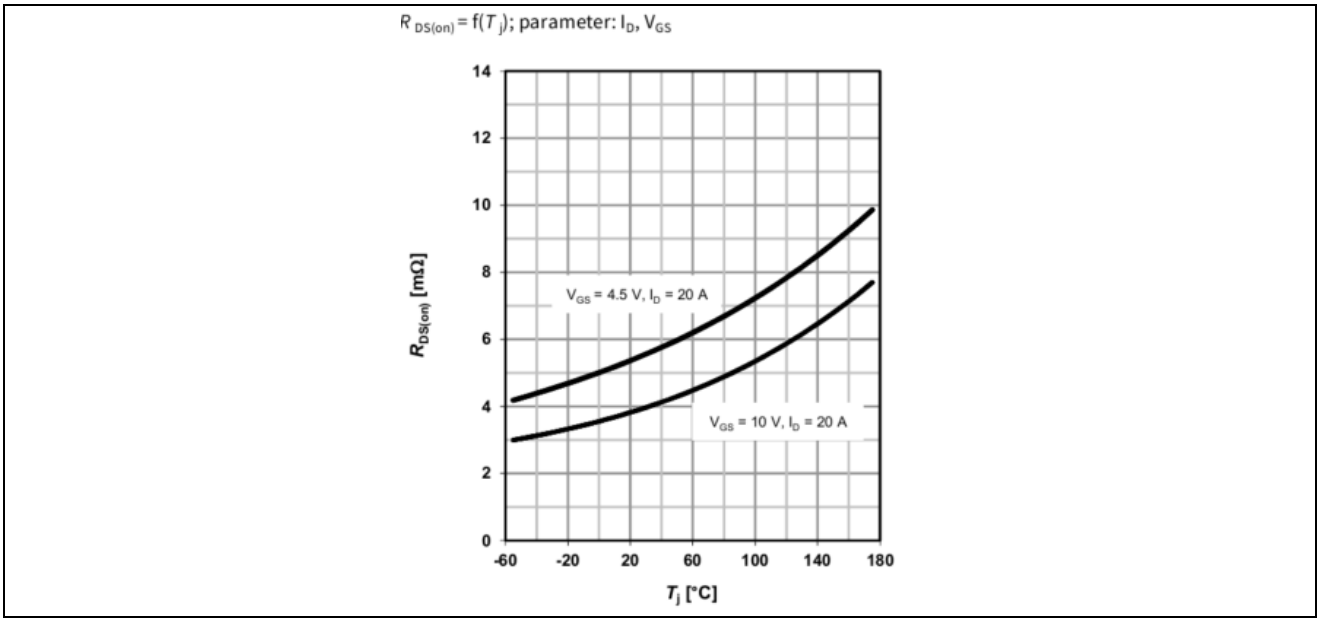


Figure 13 Typical Drain-Source ON-state Resistance Characteristics $R_{DS(on)}=f(T_j)$

2.9 Gate Threshold Voltage

The Gate-Source threshold voltage $V_{GS(th)}$ defines the required Gate-Source voltage at the specified Drain current I_D under given junction temperature T_J. This parameter is 100% tested in production under the given conditions and specified as minimum, typical and maximum ratings.

Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, I_D=29 µA	1.2	1.7	2.2	V

Figure 14 Gate Threshold Voltage $V_{GS(th)}$

This parameter has a negative temperature coefficient and its typical behavior is illustrated in a diagram as a function of T_J at given I_D. Two curves are generally provided in this plot, one is plotted with I_D specified in the table and the other one is with 10 times higher I_D because Drain-Source leakage current may reach specified current at T_J.

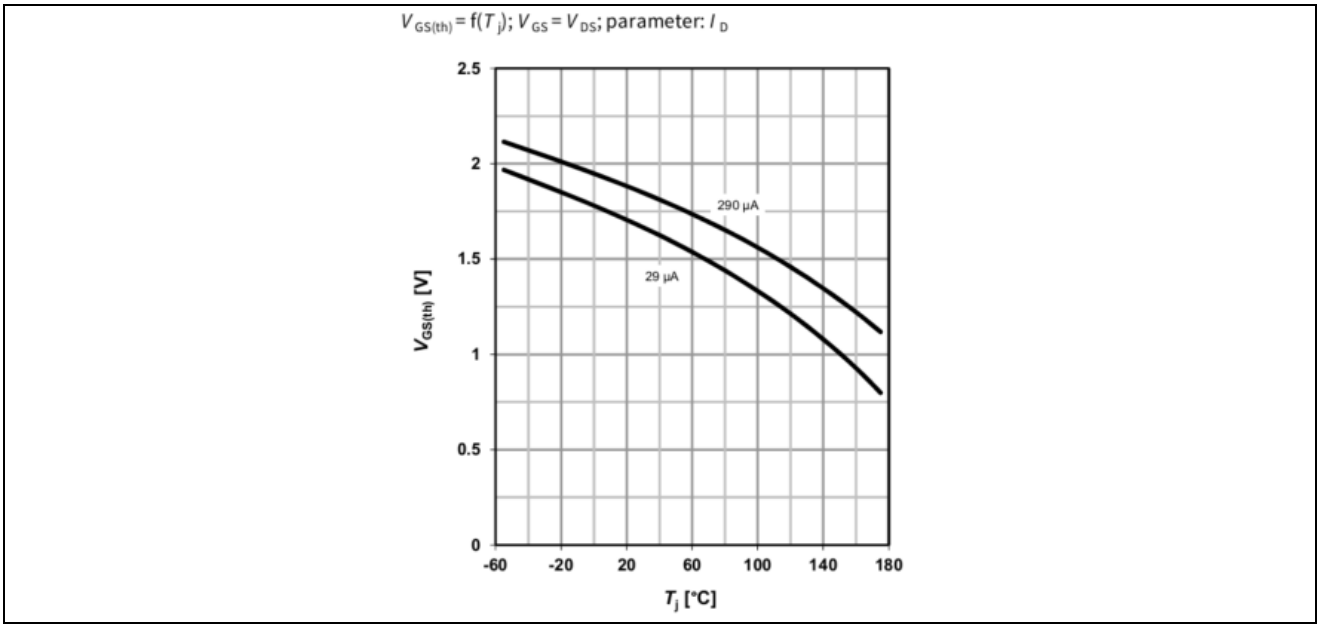


Figure 15 Typical Gate Threshold Voltage Characteristics $V_{GS(th)} = f(T_J)$

2.10 Capacitances

The parasitic capacitances of the MOSFET are specified with typical and maximum rating under given conditions, and they are defined by design during development. The capacitances between each terminal can't be directly measured, however, they can be calculated using input, output and reverse transfer capacitances. Following equations describe the relationship among them.

$$(7) \quad C_{iss} = C_{GS} + C_{GD}$$
$$C_{oss} = C_{DS} + C_{GD}$$
$$C_{rss} = C_{GD}$$

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz	–	1923	2500	pF
Output capacitance	C_{oss}		–	356	463	
Reverse transfer capacitance	C_{rss}		–	18	27	

Figure 16 Specifications of Capacitances

Their typical behavior is illustrated as a function of Drain-Source voltage V_{DS}. Wide voltage dependencies are observed on C_{oss} and C_{rss} due to the change in the space region during the switching transition of the device.

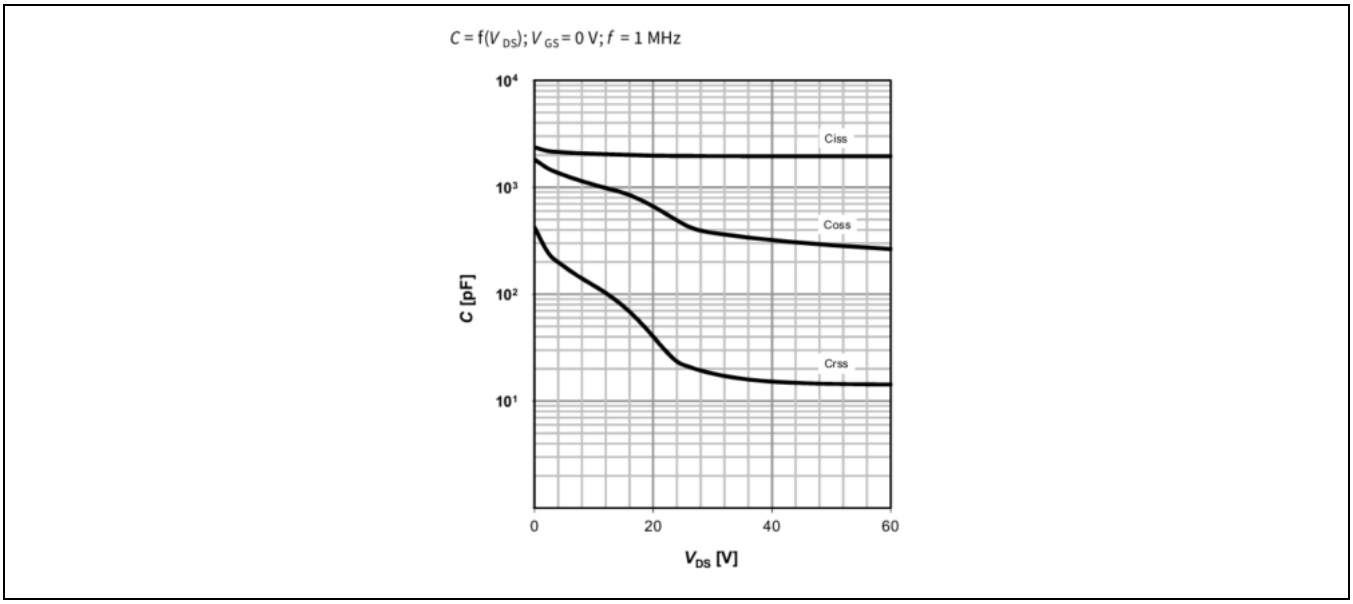


Figure 17 Typical Characteristics of Capacitances C=f(V_{DS})

2.11 Reverse Diode Characteristics

The characteristics of body diode in the MOSFET are defined under specified conditions. The following bullets explains each parameter in detail:

- Diode continuous forward current I_S: this parameter determines maximum allowable DC forward current flowing into body diode under specified conditions and it is normally identical to continuous Drain current
- Diode pulse current $I_{S,pulse}$: this parameter defines maximum allowable pulsed current flowing into body diode under specified conditions and it is normally identical to pulsed Drain current
- Diode forward voltage V_{SD}: this parameter specifies a voltage drop between Source and Drain at diode ON-state under given conditions and it is 100% tested in production.
- Reverse recovery time t_{rr}: this parameter defines the time until reverse recovery charge is removed. Typical and maximum rating are specified by design during development.
- Reverse recovery charge Q_{rr}: this parameter specifies the charge that accumulates in the PN junction of a MOSFET's body diode when the diode is forward biased under given conditions. Typical and maximum rating are specified by design during development.

Diode continous forward current[2)]	I_S	T_C=25 °C	–	–	40	A
Diode pulse current[2)]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	–	–	252	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	–	0.8	1.1	V
Reverse recovery time[2)]	t_{rr}	V_R=30 V, I_F=40 A, di_F/dt =100 A/µs	–	33	–	ns
Reverse recovery charge[2)]	Q_{rr}		–	23	–	nC

Figure 18 Reverse Diode Specifications

Figure 19 illustrates generalized reverse recovery waveforms. Diode forward current I_F flows when body diode of the MOSFET is in the forward conducting state. Once the body diode is switched to the reverse bias condition, I_F continues decreasing with a slope of di_F/dt which is determined by external circuit conditions. The

body diode conducts in the reverse direction, from Drain to Source in this case, for a short period of time. After the carriers have been swept out and the body diode enters reverse blocking mode, the current flow drops to the leakage level. Reverse recovery time t_{rr} is this short period of time when the body diode conducts in a reverse direction and reverse recovery charge Q_{rr} is the released charge during t_{rr}.

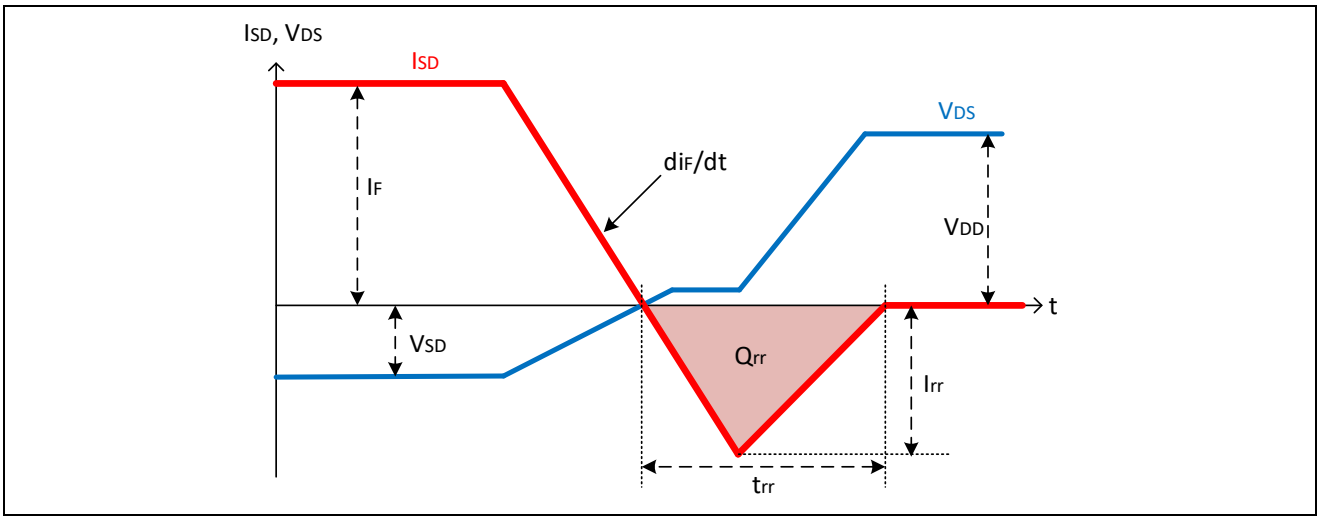


Figure 19 Generalized Reverse Recovery Waveforms

The typical characteristics of the diode forward current I_F is also illustrated in a diagram as a function of Source-Drain voltage V_{SD} with given junction temperatures.

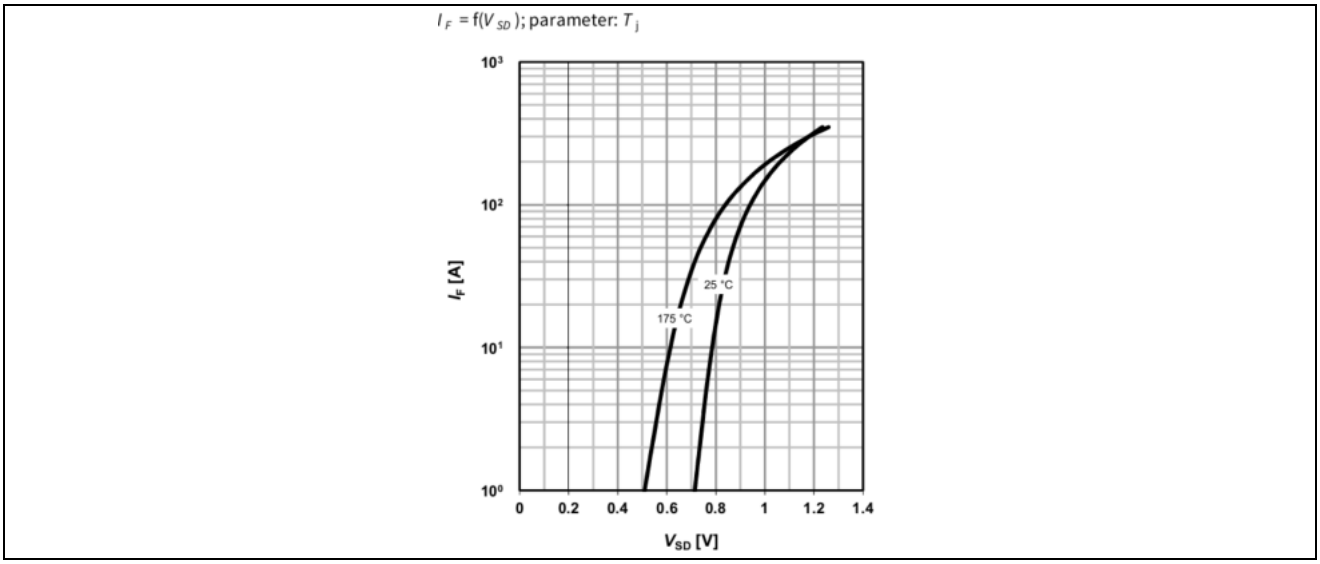


Figure 20 Typical Forward Diode Characteristics $I_F = f(V_{SD})$

2.12 Avalanche Ratings and Characteristics

The MOSFET datasheet specifies the maximum allowable avalanche energy E_{AS} under given avalanche current I_D and the maximum capability of avalanche current I_{AS}. The I_{AS} is normally the same as Drain DC current I_D unless limited by technology. These rating are not intended to be used in repetitive mode; only a single pulse is allowed.

Avalanche energy, single pulse[2)]	E_{AS}	I_D=20 A	115	mJ
Avalanche current, single pulse	I_{AS}	–	40	A

Figure 21 Avalanche Energy E_{AS} and Current I_{AS}

Avalanche characteristics are illustrated with two diagrams. One diagram presents the dependence of the pulsed avalanche current I_{AS} over the time in avalanche mode t_{AV}. The device allows avalanche operation inside the curve in terms of maximum junction temperature. This characteristic is bounded by the total energy of a pulse. The longer t_{AV}, the lower I_{AV}. The avalanche energy can be calculated by the following equation:

$$(8)\quad E_{AS} = \frac{1}{2} \cdot V_{DS} \cdot I_{AV} \cdot t_{AV}$$

The second diagram shows the maximum single pulse avalanche energy E_{AS} as a function of junction temperature T_J at given I_{AS}. As a rule of thumb, allowable E_{AS} is inversely proportional to I_{AS}. The E_{AS} decreases as T_J increases, and can be calculated with equation (9).

$$(9)\quad E_{AS}(T_J) = \left(\frac{T_{J_max} - T_J}{T_{J_max} - 25°C}\right)^2 \cdot E_{AS_25°C}$$

Please refer to two application notes available on the Infineon website that describes avalanche characteristics in detail. [4] [5]

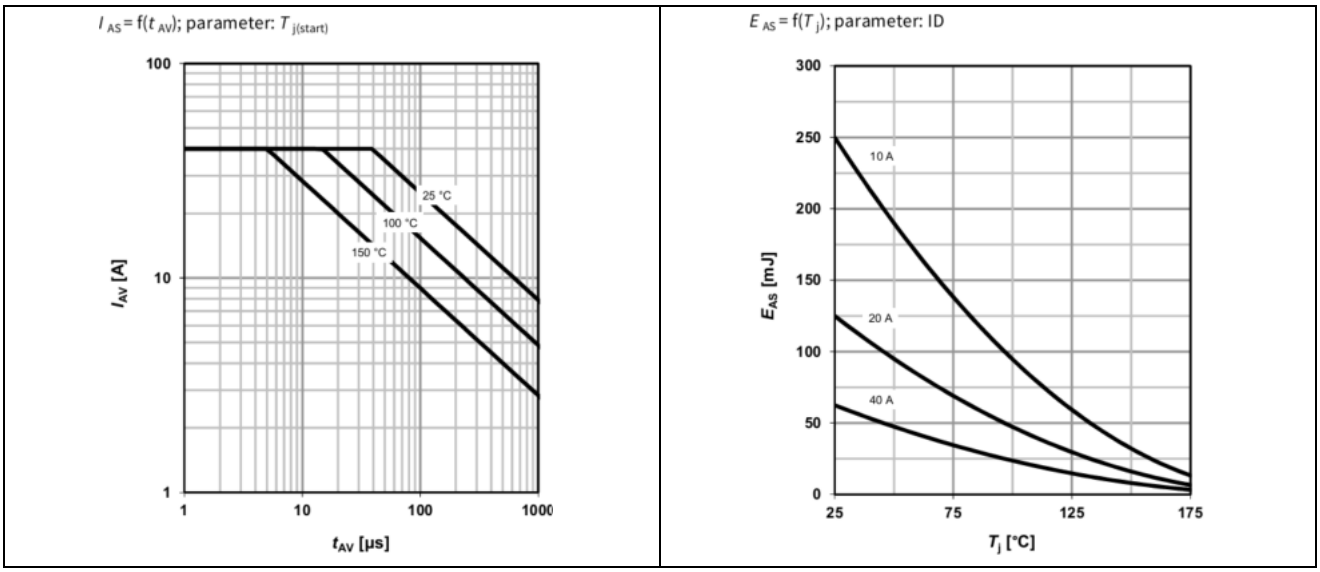


Figure 22 Typical Avalanche Characteristics, Current $I_{AV} = f(t_{AV})$ (Left) and Energy $E_{AS} = f(T_J)$ (Right)

2.13 Drain-Source Breakdown Voltage

The Drain-Source breakdown voltage $V_{(BR)DSS}$ is defined as the minimum voltage value at a given Drain current I_D and Gate-Source voltage V_{GS}. This parameter is 100% tested in production.

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60	–	–	V

Figure 23 Drain-source breakdown voltage $V_{BR(DSS)}$

The breakdown voltage $V_{(BR)DSS}$ of a MOSFET is temperature dependent with a positive temperature coefficient. A diagram is provided in the datasheet to exhibit the characteristic.

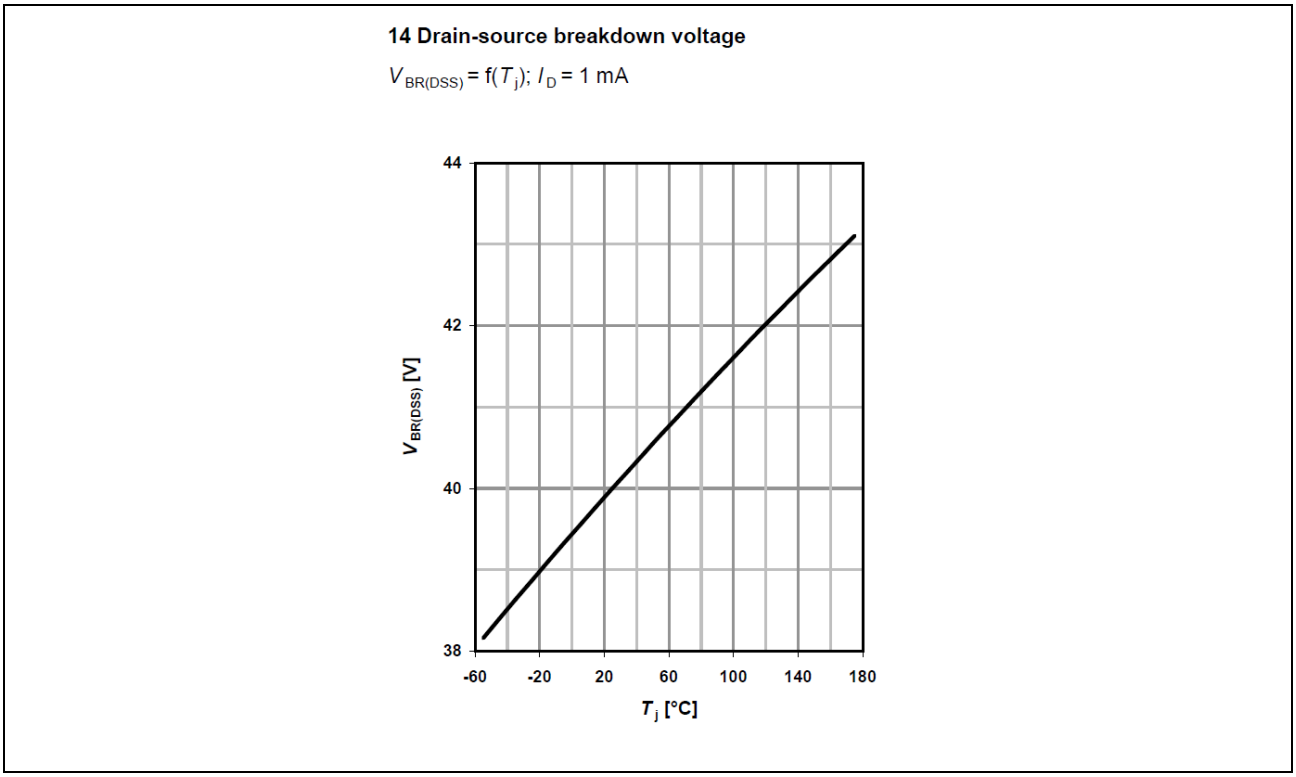


Figure 24 Drain-source breakdown voltage $V_{(BR)DSS}$=f(T_j)

2.14 Gate Charge Characteristics

The gate charge Q_G consists of the Gate-Source charge Q_{GS}, the charge between Drain and Gate Q_{GD} and over-drive charge on Q_{GS} to reach to the desired Gate-Source voltage V_{GS} from the plateau voltage $V_{plateau}$. The Q_{GS} represents the charge to charge Gate-Source capacitance C_{GS} up to $V_{plateau}$. During this period, Dain current I_D rises up to the load value after Gate-Source voltage V_{GS} reaches threshold voltage. The behavior of Drain-Source voltage V_{DS} depends on load condition. The V_{DS} falls simultaneously with the rise of I_D when switching a resistive load, or V_{DS} starts falling after I_D reaches load level when switching an inductive load. The Gate-Drain capacitance C_{GD}, also known as the miller capacitance, has to be discharged before the V_{DS} falls to its ON-state value. (V_{DS}=$R_{DS(on)}$ * I_D) This charge component is defined as Gate-Drain Charge Q_{GD}. The combined charge Q_{GS}+Q_{GD} is not enough to fully turn on the MOSFET because Drain-Source ON-state resistance $R_{DS(on)}$ is not minimized yet at this V_{GS} level. To optimize conduction loss, V_{GS} needs to be pulled up to typically V_{GS}=10V, until the devices reaches full ON state. Total gate charge Q_G is defined as the charge to reach V_{GS}=10V.

Gate charge characteristics are defined with typical and maximum ratings under the given conditions. The parameters are specified by design during development at the conditions specified. Two diagrams are provided in the datasheet as seen in figure 26 below. The diagram on the left illustrates the variation of requisite typical gate charge at given Gate-Source voltage V_{GS} under the specified Drain current I_D and Drain-Source supply voltage V_{DD}. The diagram on the right is the generalized gate charge waveform which graphically explain the definition of each of the gate charge parameters.

Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=20 A, V_{GS}=0 to 10 V	–	5.6	7.3	nC
Gate to drain charge	Q_{gd}		–	4.3	6.5	
Gate charge total	Q_g		–	28.2	36.7	
Gate plateau voltage	$V_{plateau}$		–	3.0	–	V

Figure 25 Gate Charge Specifications

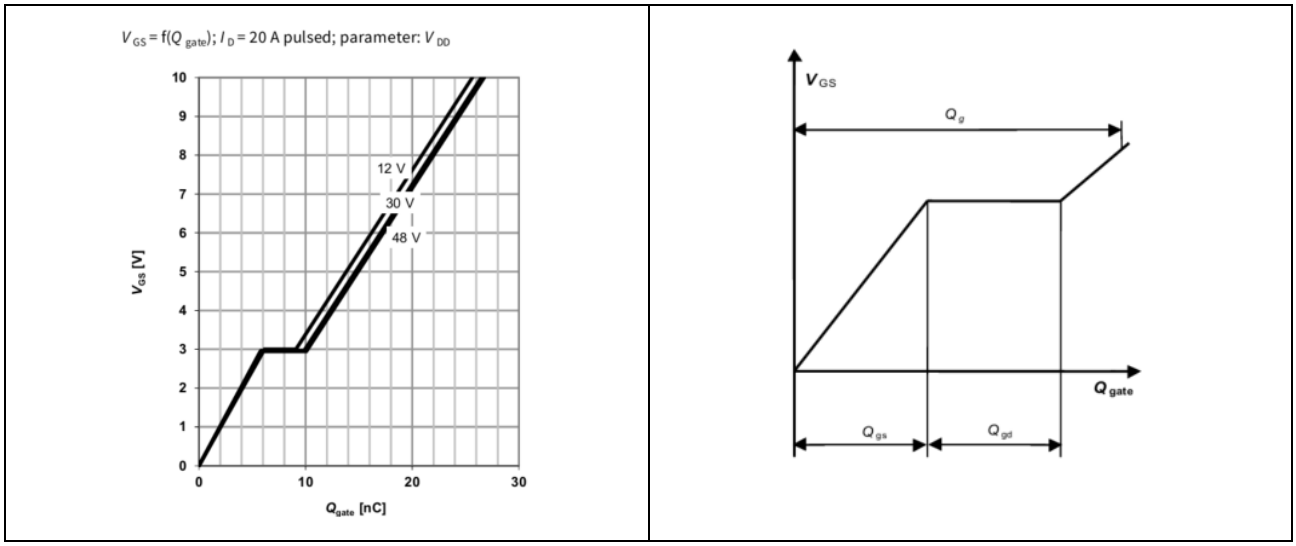


Figure 26 Typical Gate Charge V_{GS}=f(Q_{Gate}) (Left) and Generalized Gate Charge Waveform (Right)

2.15 Leakage Current

Two types of leakage current are specified in the datasheet.

- Drain-Source leakage current I_{DSS} is defined under given conditions. I_{DSS} at T_J=25°C is 100% tested in production. Maximum rating of I_{DSS} comes by design during development.
- Gate-Source leakage current I_{GSS} is defined under given conditions. This parameter is 100% tested in production. Maximum rating of I_{GSS} comes by design during development.

Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C	–	–	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=100 °C[2)]	–	–	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	–	–	100	nA

Figure 27 Leakage Current I_{DSS} and I_{GSS}

2.16 Switching Times

The datasheet includes a table that suggests typical rating for switching time related parameters under the given conditions. Each bullet explains the definition of reach parameter followed by generalized switching waveforms for graphical support.

- Turn-on delay time $t_{d(on)}$: it is measured between 10% value of rising edge on Gate Source voltage V_{GS} and 90% value of falling edge on Drain-Source voltage V_{DS}.
- Rise time t_r: it is measured at falling edge of V_{DS} between 90% value and 10% value
- Turn-off delay time $t_{d(off)}$: it is measured between 90% value of falling edge on V_{GS} and 10% value of rising edge on V_{DS}.
- Fall time t_f: it is measured at rising edge of V_{DS} between 10% value and 90% value

Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=20 A, R_G=3.5 Ω	–	3.3	–	ns
Rise time	t_r		–	0.9	–	
Turn-off delay time	$t_{d(off)}$		–	14.6	–	
Fall time	t_f		–	8.0	–	

Figure 28 Switching Time Characteristics

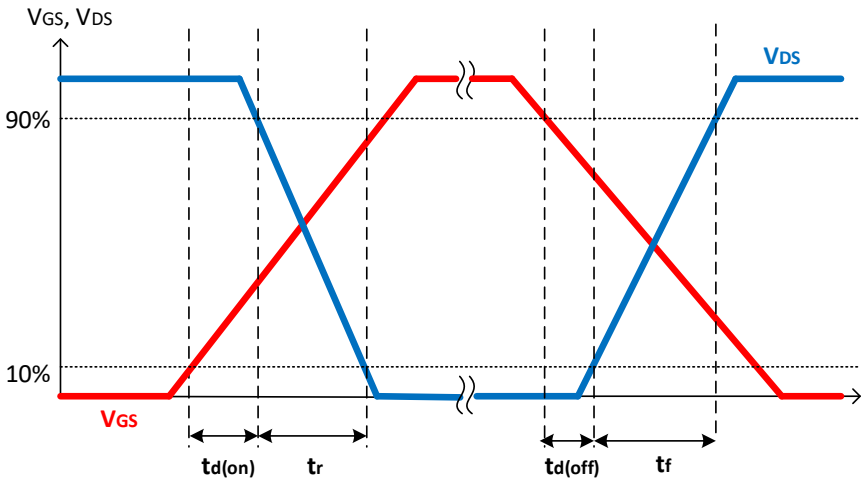


Figure 29 Generalized Switching Waveforms

2.17 T_J – Operating temperature

The maximum junction temperature specifies the absolute thermal limit in the operation of power MOSFET. It is one of the most critical limiting factors. For automotive MOSFETs, the limit is typically at 175°C. The junction temperature is qualified according to AEC-Q101 up to 1000h. It must not be exceeded under any kind of circumstances; otherwise the lifetime of the device might be considerably reduced and the proper operation of the device is not guaranteed. The negative temperature limit is typically at -55°C for automotive power MOSFETs.

Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Figure 30 Maximum junction temperature

2.18 Gate Resistance

The latest MOSFET datasheet template provides typical rating of internal gate resistance R_G. R_G is specified based upon design during development.

Gate resistance[2)]	R_G	–	–	1.35	–	Ω

Figure 31 Gate Resistance R_G

2.19 Packaging Information

The latest MOSFET datasheet template provides package information which includes package outline, recommended footprint design and packing with tape and reel. Infineon website also provides the latest package information, thus it is encouraged to check it periodically.

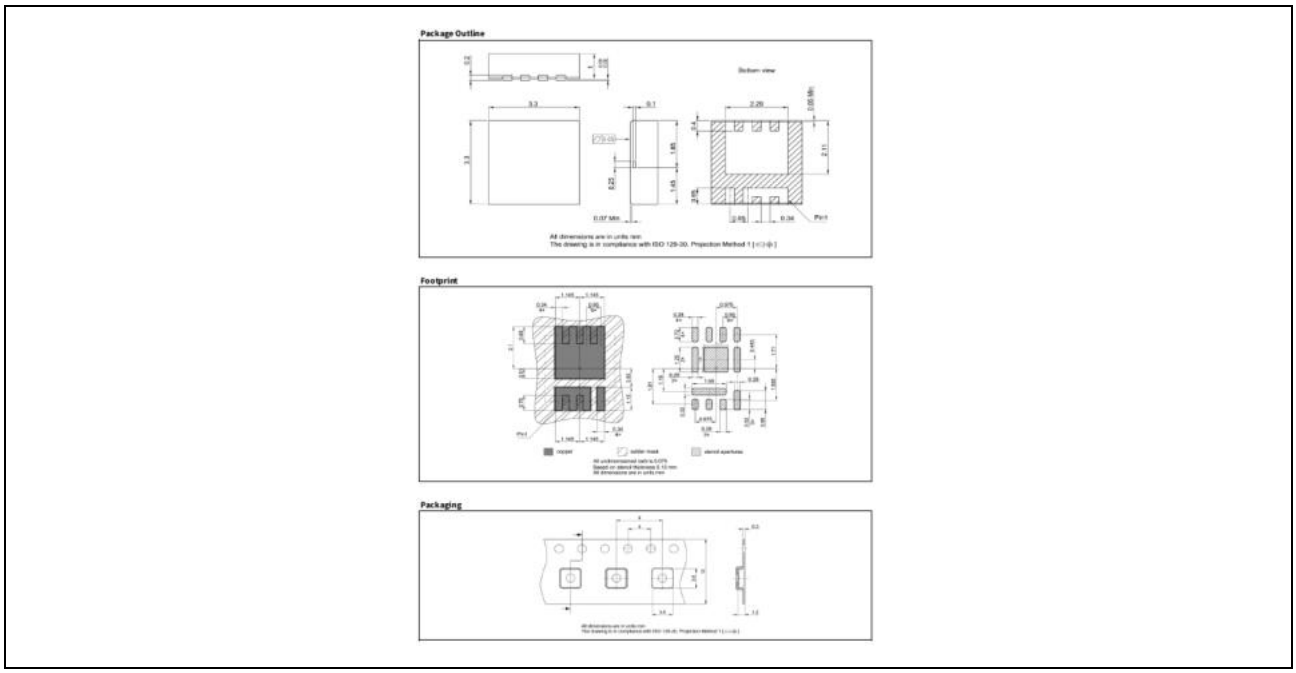


Figure 32 Package information

3 Summary

The parameters and diagrams described on the datasheet are explained in this document. It is very important for design engineers to read and understand the datasheet contests properly for finding the right product for their applications.

4 References

[1] Infineon automotive MOSFET web site
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/#!documents

[2] Application note "Automotive MOSFETs Datasheet Explanation"
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[3] Application note "MOSFET linear mode operation and SOA power MOSFETs"
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[4] Application note "Repetitive Avalanche of Automotive MOSFETs"
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[5] Application note "MOSFET some key facts about avalanche"
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5 Revision History

Document version	Date of release	Description of changes
1.0	November 18, 2021	Initial release
1.1	November 29, 2021	Diagram size adjusted

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