M61140FP

Tuner Single Chip

REJ03F0023-0130
Rev.1.3
Jun 14, 2004

Description

The M61140FP is a semiconductor integrated circuit consisting of Tuner signal processing for NTSC color TV and VCRs.

The circuit includes Mixer circuit in Tuning system, Oscillator circuit, PLL frequency synthesizer and VIF/SIF, which permits a smaller tuner system.

Features

- VIF/SIF
  Inter carrier type for NTSC
  Coil-less VCO
  Adjustment free AFT
  High-speed IF AGC
- PLL
  Low phase noise and High-speed lock-up
  Built-in band switch driver (4 port)
  I2C bus control
  Available for both XO and external reference
- Mixer/Oscillator
  Built-in U&V Oscillator and mixer
  Built-in IF Amplifier (Unbalanced Output)

Application

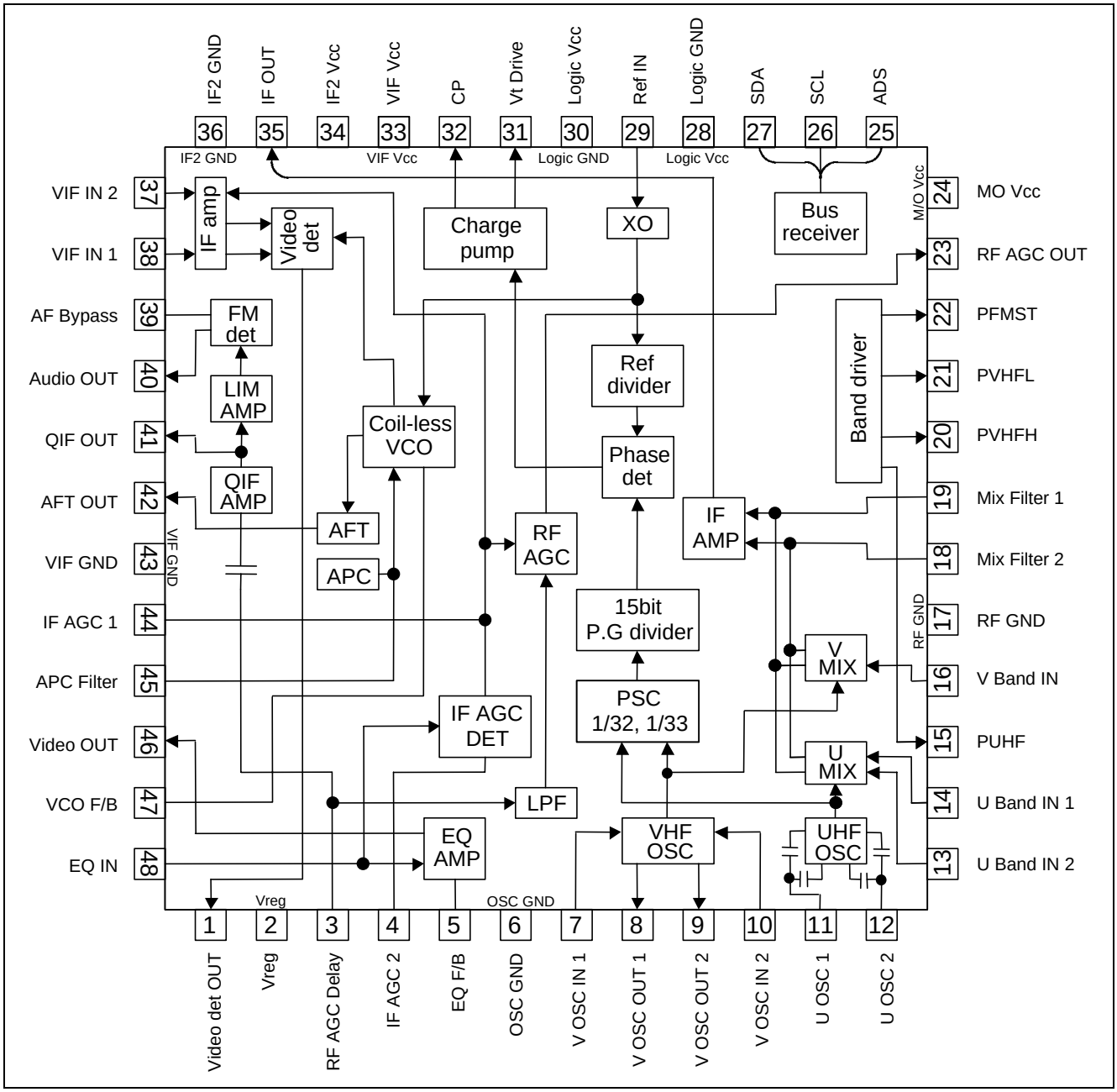
TV, VCR

Recommended Operating Conditions

Supply voltage range --- 4.75 to 5.25V

Recommended supply voltage --- 5.0V

Pin Configuration and Block Diagram



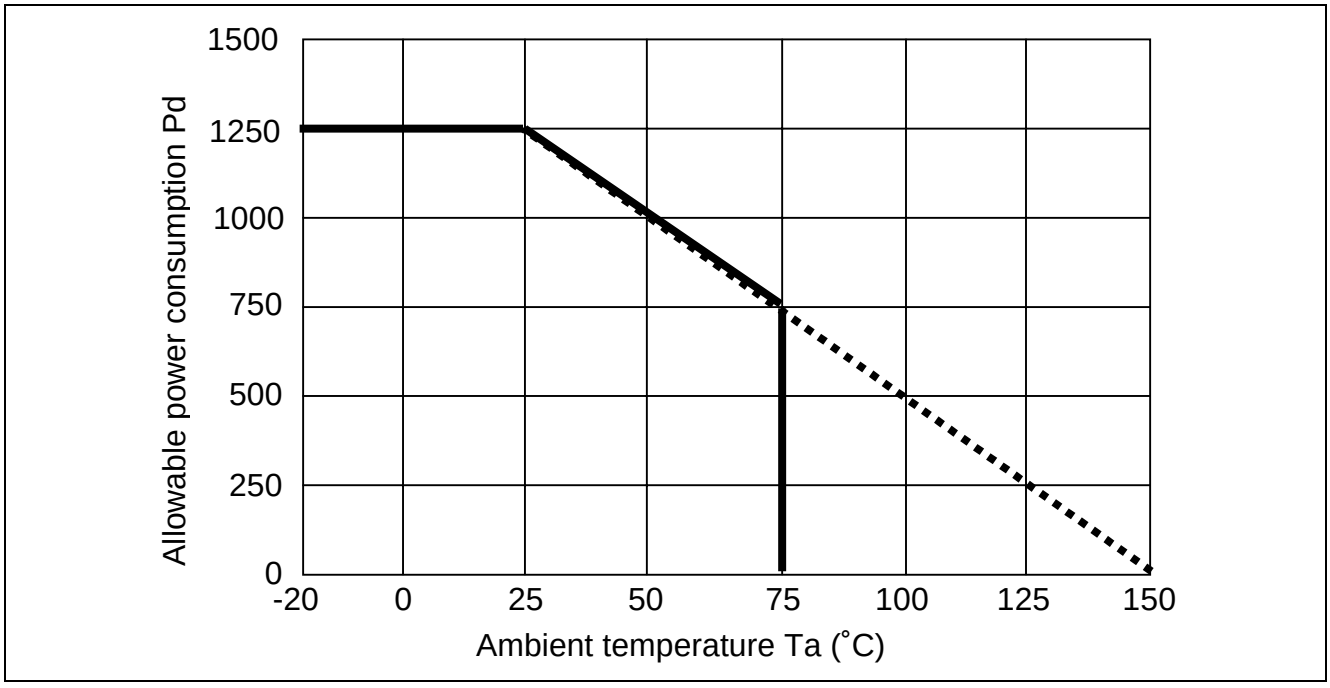
Absolute Maximum Ratings

(Ta=25ºC, unless otherwise noted)

Parameter		Symbol	Ratings	Unit	Note
Supply Voltage		Vcc	6	V	
MO Block	Maximum Allowable Input	Vin	126	dBμV	
PLL Block	Input Voltage	Vimax	6	V	Pin25 to 27
	Port Output Voltage	Vo	6	V	Pin20 to 22,15
	Port Output Current (1)	Iopmax1	26	mA	Pin20, 21
	Port Output Current (2)	Iopmax2	7	mA	Pin15, 22
	Port Output Current (3)	Iopmax3	33	mA	2 circuits are on at same time
	SDA Output Current	Iosdamax	10	mA	
Power Consumption		Pd	750	mW	Recommended circuit board. When Cu occupancy area is 50%.
Operating Temperature		Topr	–20 to +75	°C	
Storage Temperature		Tstg	–40 to +150	°C	

Temperature Characteristics (maximum ratings)

Mounting in standard circuit board (70mm × 70mm × 1.6mmt Epoxy board of one side copper)

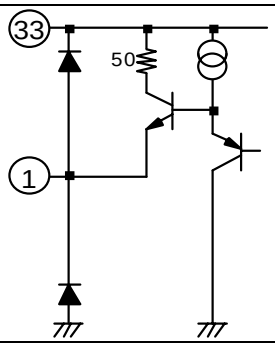
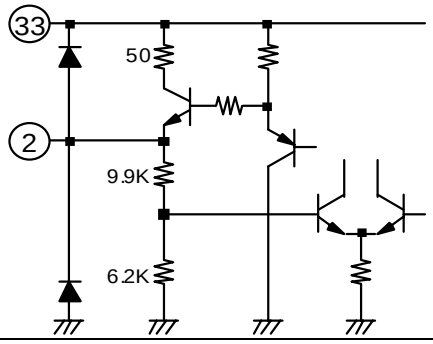
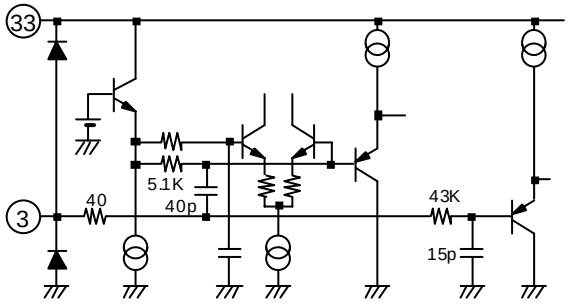
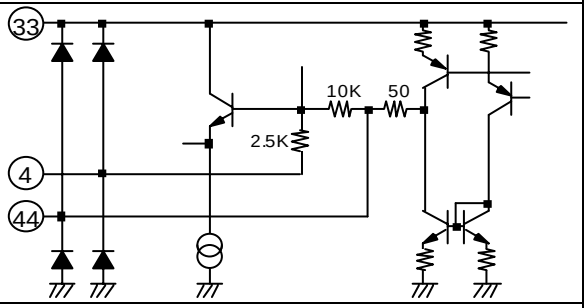
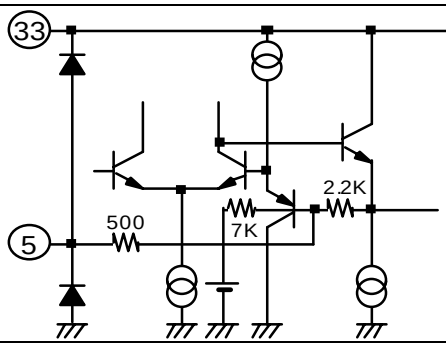


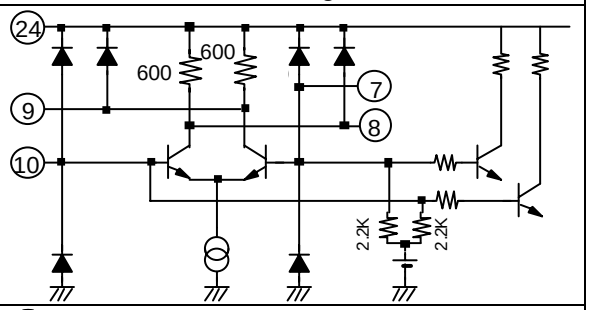
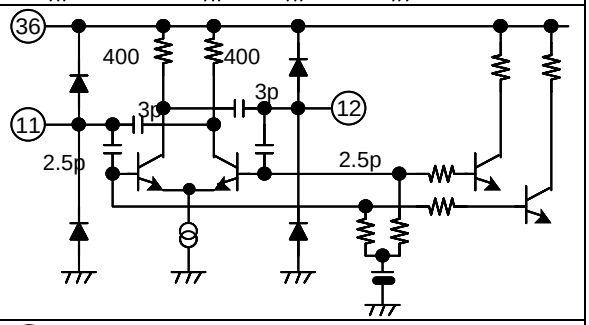
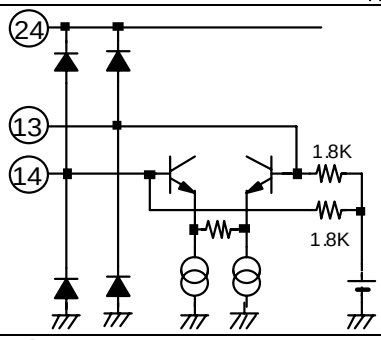
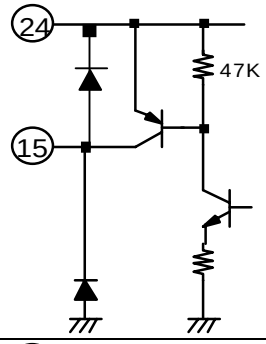
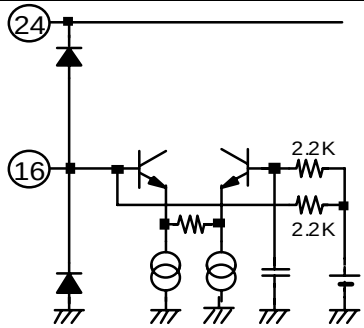
Recommended Operating Condition

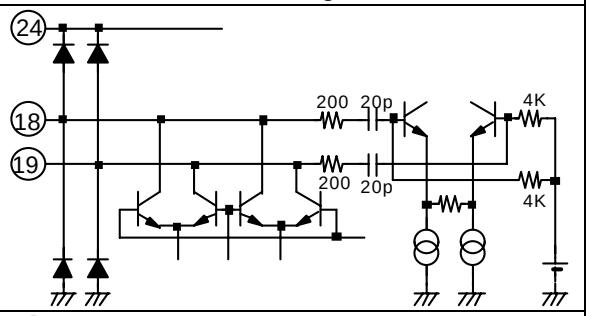
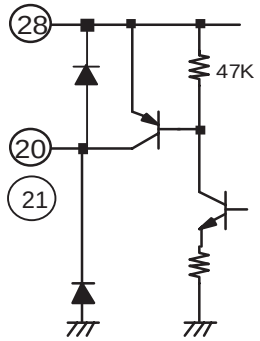
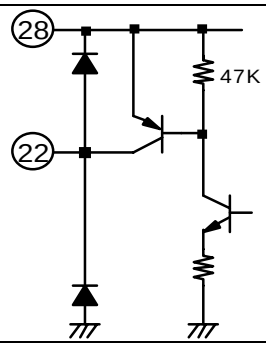
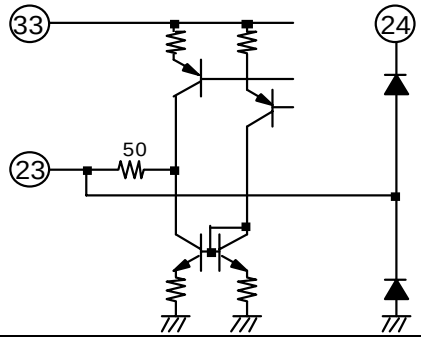
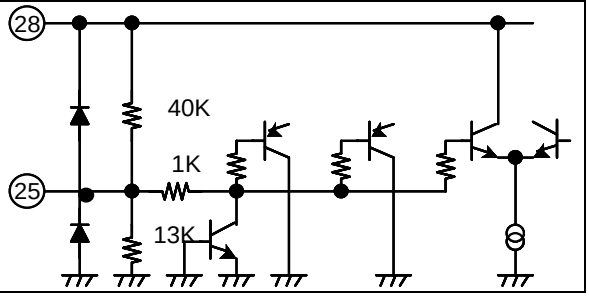
(Ta=25ºC, unless otherwise noted)

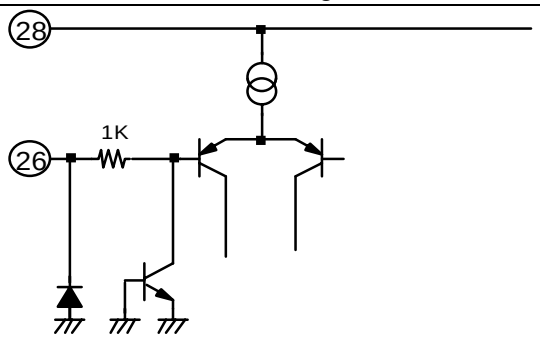
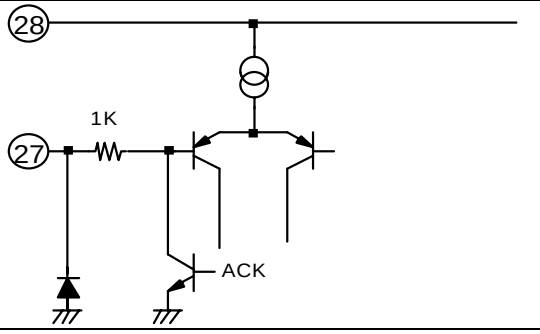
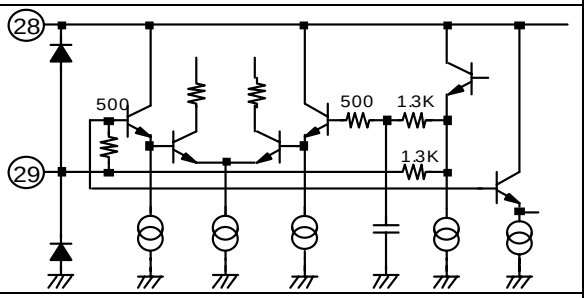
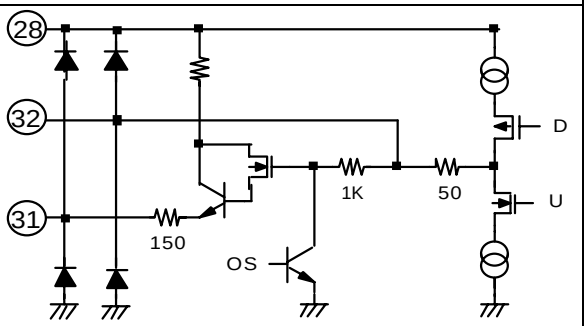
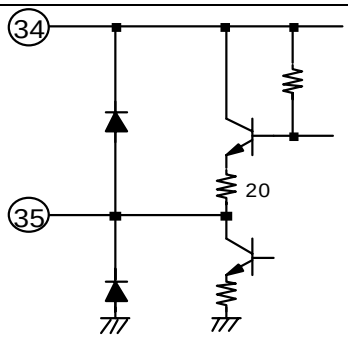
Parameter	Symbol	Ratings	Unit	Note
Guarantee Operating Voltage	Vcc	4.5~5.3	V	Refer to Data
Supply Voltage Range	Vcc	4.75~5.25	V	
Operating frequency of Crystal oscillator	fopr	4.0	MHz	
Port output current (1)	Ioprt1	0~25	mA	Pin 20,21
Port output current (2)	Ioprt2	0~5	mA	Pin 15,22

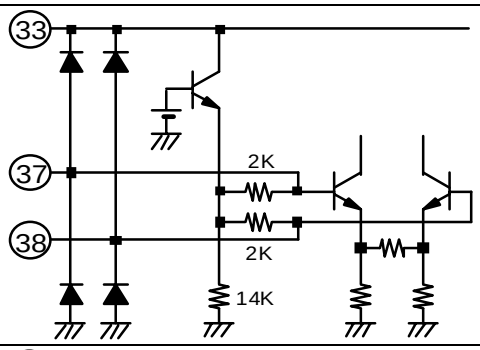
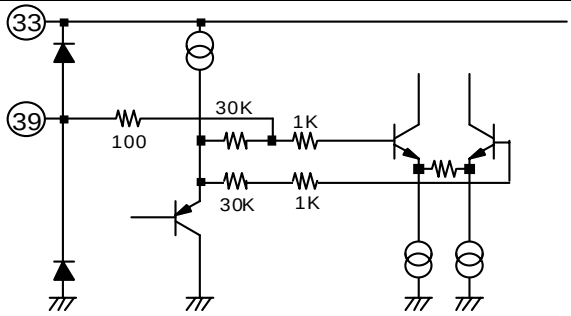
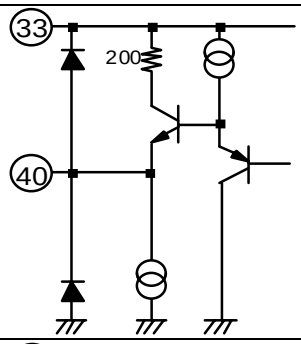
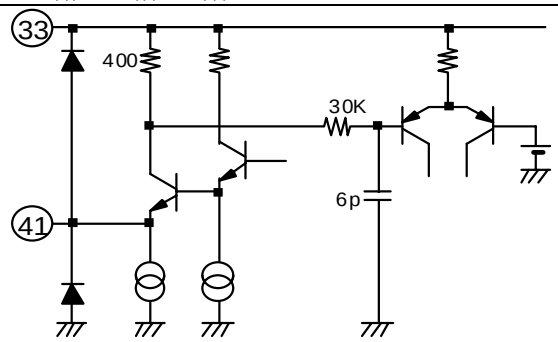
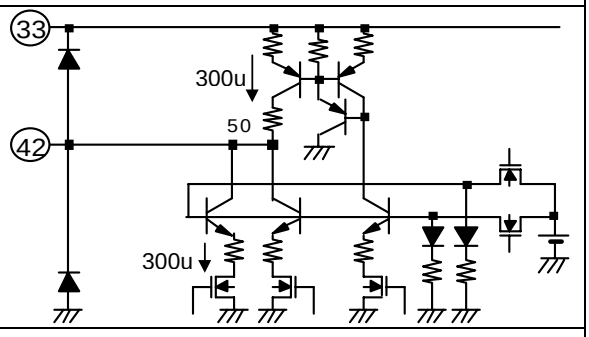
Pin Description

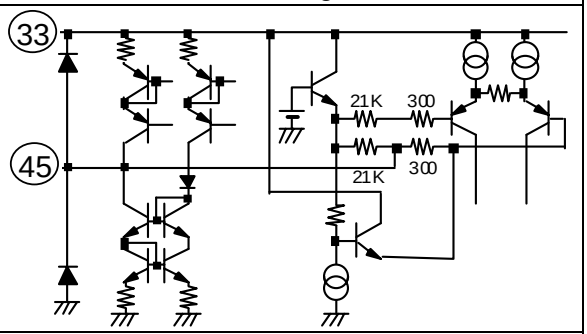
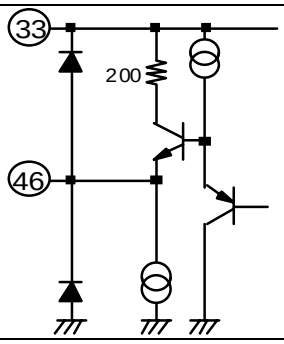
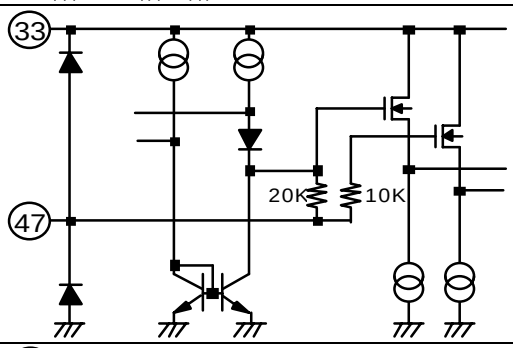
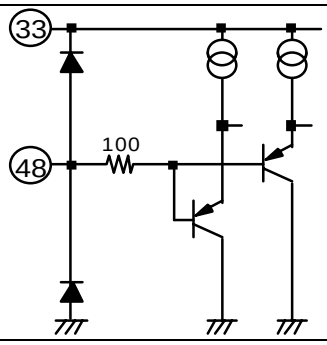
Pin No.	Pin name	Function	Circuit Diagram
1	VIDEO DET OUT	Video detected output terminal. SIF trap and SIF B.P.F. are connected to this terminal. Because of open emitter configuration, an externally connected drive resistor is necessary.	
2	Vreg	Regulated voltage output. Approximately 3V output.	
3	RF AGC DELAY	RF AGC terminal. This terminal combine 4.5MHz SIF signal input with set up the RF AGC delay point. The RF AGC delay point is set up by the DC component of input signal. AC component is FM detection threw the limiter amplifier.	
4	IF AGC 2	IF AGC 2 terminal	
44	IF AGC 1	IF AGC 2 terminal. External capacitor effects AGC speed. When this terminal is grounded, the effect of VIF amp gain becomes minimum.	
5	EQ F/B	Equalizer feedback terminal. It is possible to change the frequency characteristic of the video signal by attaching L,C,R to this terminal.	
6	OSC GND	OSC ground terminal.	

Pin No.	Pin name	Function	Circuit Diagram
7	V OSC IN 1	VHF oscillator circuit is connected externally. When band byte bit PUHF is set "1", bias current of oscillator transistor turns OFF.	
8	V OSC OUT 1		
9	V OSC OUT 2		
10	V OSC IN 2		
11	U OSC 1	UHF oscillator circuit is connected externally. When band byte bit PUHF is set "1", bias current of oscillator transistor turns ON.	
12	U OSC 2		
13	U BAND IN 1	UHF RF input terminal. Input type is balance input. In the case of unbalance input, grounding of either pin 13 or 14 with capacitor is required, while input to the other pin.	
14	U BAND IN 2		
15	PUHF	Band change drive terminal. Output configuration is PNP open collector. When band selection bit PUHF is set "1", current is output.	
16	V BAND IN	VHF RF input terminal. Input type is unbalance.	
17	RF GND	RF (Mixer) GND terminal.	

Pin No.	Pin name	Function	Circuit Diagram
18	MIX FILTER 1	Mixer output terminal. The output terminal is open collector type, single-tuned filter is connected. This pin is pull-up through power supply in order for voltage to be above 4.2V.	
19	MIX FILTER 2		
20	PVHFH	Band change drive terminal. Output configuration is PNP open collector. When band selection bit PVHFL or PVHFH is set "1", current is output.	
21	PVHFL		
22	PFMST	Band change drive terminal. Output configuration is PNP open collector. When band selection bit PFMST is set "1", current is output. Reference frequency or divided frequency of local are output by test mode condition.	
23	RF AGC OUT	RF AGC output terminal. It is current drive type.	
24	MO Vcc	Mixer and oscillator block power supply.	
25	ADS	Address setting input terminal. Address bit "MA1","MA2" is selected by the potential at this terminal.	

Pin No.	Pin name	Function	Circuit Diagram
26	SCL	SCL input terminal.	
27	SDA	SDA input terminal. Reading and writing of data confirm to I^2C bus of Philips.	
28	Logic Vcc	Logic block power supply.	
29	REF IN	Reference frequency input terminal. Connect crystal oscillator at this terminal, or external signal (Sine wave).In this case of using external sine wave signal, pull down this terminal with 1.5k to 3.3kΩ.	
30	Logic GND	Logic block power supply.	
31	VT DRIVE	Filter transistor drive terminal. As for drive output, control bit "OS" controls it On or OFF	
32	CP	Charge pump output terminal. When the phase of the divide frequency of local is lead compared with the reference frequency, the "source" current state becomes active. If it is lag, the "sink" current becomes active. If the phase are the same, the high impedance state becomes active.	
33	VIF Vcc	VIF block power supply.	
34	IF2 Vcc	Power supply terminal exclusively for IF amp output (pin 34) circuit.	
35	IF OUT	IF amp output terminal. This terminal is a low impedance and output IF frequency.	

Pin No.	Pin name	Function	Circuit Diagram
36	IF2 GND	IF2 grand terminal. This grand is exclusively used by circuit of IF amplifier	
37 38	VIF IN 1 VIF IN 2	IF signal thew SAW filter is input. It is a balance type input.	
39	AF BYPASS	AF bypass terminal. It is connected to one of the input of a differential amplifier, external capacitor provides AC filtering. When resistor is connected in series with capacitor, it is possible to lows the amplitude of the audio output. When audio output terminal is not used, please connect pin 22 to GND.	
40	AUDIO OUT	Sound output terminal. De-emphasis is achieved by external components.	
41	QIF OUT	QIF output terminal. FM signal which is converted to 4.5MHz is output. Additionally, this pin has dual function of being VIF VCO type selection. Connected to GND via 1.2kΩ	
42	AFT OUT	AFT output terminal. Because of pulse-like signal output, a smoothing capacitor is connected externally. In addition, AFT detection sensitivity is set by external resistor.	
43	VIF GND	VIF GND terminal.	

Pin No.	Pin name	Function	Circuit Diagram
45	APC FILTER	APC filter terminal. It is the loop filter terminal which a VIF signal is made to lock VCO and keeps frequency constant.	
46	VIDEO OUT	Video output terminal. The signal inputted into the EQI terminal is outputted.	
47	VCO F/B	VCO feedback terminal. The feedback is to keep the free-running frequency of the built-in VCO.	
48	EQ IN	The video signal threw the SIF trap is input to this terminal. DC impression from pin 1 is required for the input to 48 pins.	

Setting Data

M61140FP's bus format is based on Philips's I^2C-bus.

Bidirectional bus communication control can be performed. It consists of WRITE mode which receives various data, and READ mode which transmits data. Recognition in WRITE mode and READ mode is performed by specification of the last bit on Address Byte (R/W bit). When the setup of a R/W bit is "0", it is set as WRITE mode and, in the case of "1", is set as READ mode. Furthermore, it has the address in which four programs are possible.

It enables this to use two or more devices on the same I^2C bus.

Moreover, four programmable addresses are possible. Therefore, two or more devices become usable on I^2C bus.

A setup of an address is chosen by the voltage impressed to an address setting terminal (ADS:25 pin).

If the address Byte in agreement is received, a data line will be set to "L" between knowledge, and at the time of WRITE mode, if Data Byte is received, SDA line between knowledge will be set to "L."

It shows a definition of bus protocol admitted in the following.

Mode_1 STA CA DB1 DB2 CB1 CB2 STO

Mode_2 STA CA CB1 CB2 DB1 DB2 STO

Mode_3 STA CA DB1 DB2 STO

Mode_4 STA CA CB1 CB2 STO

STA : Start condition

STO : Stop condition

CA : Chip address

DB1 : Divider data byte 1

DB2 : Divider data byte 2

CB1 : Control data byte 1

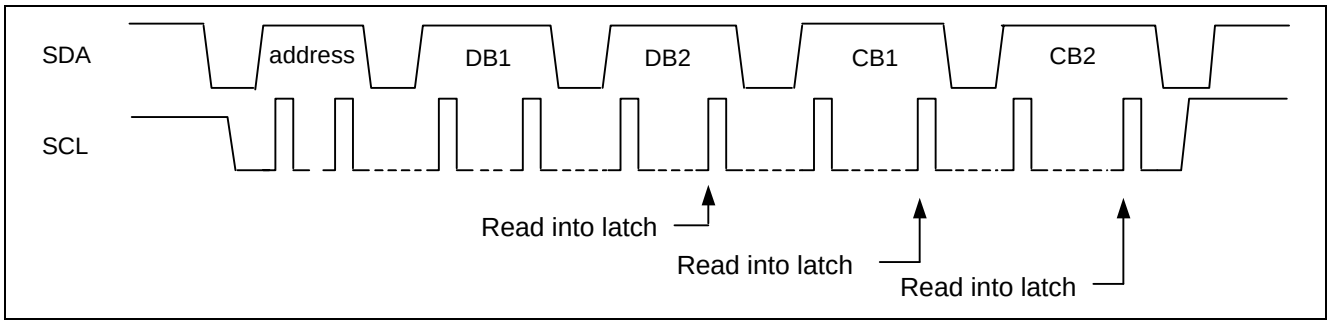
CB2 : Band data byte 2

(1) WRITE mode

The information of 5 bytes required for circuit operational chip address, control data and band SW data of 2 bytes and divider data of 2 bytes. after the chip address input, 2 or 4 bytes can be received. Function bit is contained in the first and the third data byte to distinguish between divider and 'control data/band SW data', with "0" going ahead of divider data, and "1" going ahead of 'control data/band SWdata'.

The timing of Writing data for bus protocol Mode is shown in the figure below. Divider data uses 15 bits and is read in at the rise of the eighth clock bit of the second byte divider data (DB2). Control data (CB1) and band SW-data (BB) are each read in at the rise of their eighth clock bit.

Timing Chart



Write mode data format

Byte	MSB							LSB	
Address Byte (CA)	1	1	0	0	0	MA1	MA0	R/W=0	A
Divider Byte1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider Byte2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte (CB1)	1	CP	T2	T1	T0	Rsa	Rsb	OS	A
Band Byte (CB2)	X	X	X	X	PUHF	PFMST	PVHFH	PVHFL	A

Programmable Address Bit

Address input voltage applied to ADS [V]	MA1	MA0
0 to 0.1xVcc	0	0
Open or 0.2 to 0.3xVcc	0	1
0.4xVcc to 0.6xVcc	1	0
0.9xVcc to Vcc	1	1

N14 to N0 : Set up for division ratio of the programmable divider

Frequency of VCO fvco: fvco=fref x N

Division ratio N: N=N14(2^14)+N13(2^13)+ --- +N0(2^0)

Range of division ratio N: N=1,024 to 32,767

fref: Reference frequency of phase comparator

CP: Set up the charge pump current

CP	Charge pump current *
0	70µA
1	300µA

Note:* Current of charge pump is typ current

In the case of setting current 270µA,when PLL is locked, charge pump current is automatically switched to CP=O (70µA).

T2, T1, T0 : Set up for test mode

CP	T2	T1	T0	Charge pump	Test output	Test SW	Mode
0	0	0	X	CP switched off	-	OFF	Normal mode
1	0	0	X	CP switched on	-	OFF	Normal mode
X	0	1	X	High impedance	-	OFF	Test mode
X	1	1	0	Sink	-	OFF	Test mode
X	1	1	1	Source	-	OFF	Test mode
0	1	0	0	High impedance	fREF	OFF	Test mode
1	1	0	X	CP switched on	-	ON	TV test mode
0	1	0	1	High impedance	f1/N	OFF	Test mode

Note : fREF and f1/N is available on pin PFMST(pin 22). Test SW is for the mix filter damping switch

Rsa : Set up tuning step

Rsa	Rsb	Division ratio	tuning step frequency @4MHz X'tal
0	1	1/128	31.25kHz
1	1	1/64	62.5kHz
X	0	1/80	50.0kHz

OS : Set up drive output

OS	Drive output	Mode
0	ON	Normal mode
1	OFF("L")level	Test mode

PFMST, PUHF , PVHFL,PVHFH : PORT setting

PFMST,PUHF,PVHFL,PVHFH	Output
0	OFF
1	ON

PNP open collector output. When PUHF is "OFF", Mixer and Oscillator active VHF mode.

(2) READ mode data format

At the time of READ mode, a power-on reset state, a phase comparison machine lock detector output state, and the state of the charge pump current change SW are outputted to a master device.

Read mode data format

Byte	MSB								LSB
Address Byte	1	1	0	0	0	MA1	MA0	R/W=1	A
Status Byte	POR	FL	ACPS	X	X	X	X	X	A

X: 0 or 1 Don't care

POR: Power on reset flag. Output is "1" at power-on
Set to "1" when the time of a power supply voltage injection or power supply voltage falls in about 3V or less.
Reset by "0", if a Request to Send is carried out in READ mode and a flag is returned.
Power supply voltage is about 3v or more, Reset by "0", after returning a flag in READ mode.

FL: Lock detector flag. Output is "1" at locked, output is "0" at unlocked.

ACPS: Automatic charge pump current flag. Output is "0" at charge pump current automatically switched mode, output is "1" at other mode.

(3) Power on reset

The initial status is shown as below when supply voltage is turned on. If supply voltage becomes less than about 3.0V, the initial status is set.

Byte	MSB							LSB
Divider Byte1 (DB1)	0	X	X	X	X	X	X	X
Divider Byte2 (DB2)	X	X	X	X	X	X	X	X
Control Byte (CB1)	1	1	0	1	X	1	1	1
Band Byte (CB2)	X	X	X	X	0	0	0	0

(4) Data format example

Ex1.US-TV-ch2 (fRF=55.25MHz,fosc=101MHz),CP sw=ON, Reference Frequency=4MHz,31.25kHzstep, PUHF="ON"

Byte	MSB							LSB	
Address Byte	1	1	0	0	0	MA1	MA0	R/W=0	A
Divider Byte1 (DB1)	0	0	0	0	1	1	0	0	A
Divider Byte2 (DB2)	1	0	1	0	0	0	0	0	A
Control Byte (CB1)	1	1	0	0	0	0	1	0	A
Band Byte (CB2)	X	X	X	X	0	0	0	1	A

Divide ratio $N = 101*10^6/31.25*10^3$

$= 3232$

$= 2^{11}+2^{10}+2^7+2^5$

Purchase of Renesas Technology electric corporation's I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips

Electrical Characteristics

DC characteristics

(Ta=25°C, Vcc=5.0V otherwise noted.)

Item	Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
					min	typ	max		
IF Vcc current	IccIF	33	-	SW33=2	40	53	66	mA	
IF2 Vcc current	IccIF2	34	-	SW34=2	14	19	24	mA	
M/O Vcc current	IccRF	24	-	SW24=2	14	18	23	mA	
Logic Vcc current(1)	IccLo1	28	-	SW28=2 Port OFF	11	14	18	mA	
Logic Vcc current(2)	IccLo2	28	-	SW28=2, Io(PVHFL) or Io(PVHFH)=20mA	27	37	46	mA	
Logic Vcc current(3)	IccLo3	28	-	SW28=2, Io(PFMST) or Io(PUHF)=5mA	15	20	25	mA	

Mixer and OSC Block

(Ta=25°C, Vcc=5.0V otherwise noted.)

Item		Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
						min	typ	max		
VHF	Conversion gain1	GvcV1	35,16	-	fRF=55.25MHz, CW	20	23	26	dB	
	Conversion gain2	GvcV2	35,16	-	fRF=361.25MHz, CW	20	23	26	dB	
	NF1	NFV1	35	-	fRF=55.25MHz, CW	-	16.5	18	dB	
	NF2	NFV2	35	-	fRF=361.25MHz, CW	-	17.5	20	dB	
	Cross modulation1	CMV1	35	-	fd=55.25MHz, CW fud=fd6MHz, AM100kHz, 30%	-28	-25	-	dBm	
	Cross modulation2	CMV2	35	-	fd=361.25MHz, CW fud=fd6MHz, AM100kHz, 30%	-28	-25	-	dBm	
	CS beat1	CS1	35	-	fp=241.25MHz, fs=245.75MHz fc=244.83MHz, AM100kHz, 30%	55	60	-	dBc	
	CS beat1	CS2	35	-	fp=241.25MHz, fs=245.75MHz fc=244.83MHz, AM100kHz,30%	55	60	-	dBc	
UHF	Conversion gain3	GvcU3	35	-	fRF=367.25MHz, CW	27	30	33	dB	
	Conversion gain4	GvcU4	35	-	fRF=801.25MHz, CW	27	30	33	dB	
	NF1	NFU1	35	-	fRF=367.25MHz, CW	-	11.5	13	dB	
	NF2	NFU2	35	-	fRF=801.25MHz, CW	-	13	15	dB	
	cross modulation1(-)	CMU1(-)	35	-	fd=367.25MHz, CW fud=fd-6MHz, AM100kHz, 30%	-31	-28	-	dBm	
	cross modulation1(+)	CMU1(+)	35	-	fd=367.25MHz, CW fud=fd+6MHz, AM100kHz, 30%	-37	-34	-	dBm	
	cross modulation2(-)	CMU2(-)	35	-	fd=801.25MHz, CW fud=fd-6MHz, AM100kHz, 30%	-31	-28	-	dBm	
	cross modulation2(+)	CMU2(+)	35	-	fd=801.25MHz, CW fud=fd+6MHz, AM100kHz, 30%	-37	-34	-	dBm	
	CS beat3	CS3	35	-	fp=615.25MHz, fs=627.75MHz fc=618.83MHz, VoIF=-10dBm	55	60	-	dBc	

Mixer and OSC Block

(Ta=25°C,Vcc=5.0V otherwise noted.)

Item		Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
						min	typ	max		
Beat	6ch beat	INT6ch	35	-	fp=83.25MHz, fs=87.75MHz VoIF=-10dBm	55	60	-	dBc	
	A5ch beat	INTA5ch	35	-	fp=91.25MHz, VoIF=-10dBm	60	65	-	dBc	
	5ch beat	INT5ch	35	-	fp1=83.25MHz, fp=77.25MHz VoIF=-10dBm	60	65	-	dBc	
	PSC beat1	PSC183	35	-	fosc=183MHz	-	-	-85	dBm	
	PSC beat2	PSC366	35	-	fosc=366MHz	-	-	-85	dBm	
	PSC beat3	PSC732	35	-	fosc=732MHz	-	-	-85	dBm	
OSC	VHF OSC Power supply shift	Δfosc_v	35	-	ΔVcc=10%	-	-	±500	kHz	
	VHF OSC Swon Drift	Δfoscv_t	35	-	VccOn 3sec to 5min	-	-	±500	kHz	
	VHF OSC C/N1	C/N(V1)	35	-	fp=83.25MHz, VoIF=-10dBm +/-50kHz offset	65	-	-	dBc	
	VHF OSC C/N2	C/N(V2)	35	-	fp=241.25MHz, VoIF=-10dBm +/-50kHz offset	65	-	-	dBc	
	UHF OSC Power supply shift	Δfosc_u	35	-	ΔVcc =10%	-	-	±500	kHz	
	UHF OSC Swon Drift	Δfoscu_t	35	-	VccOn 3sec to 5min	55	-	-	kHz	
	UHF OSC C/N	C/N(U)	35	-	fp=615.25MHz, VoIF=-10dBm +/-50kHz offset	65	-	-	dBc	

PLL Block

(Ta=25°C,Vcc=5.0V otherwise noted.)

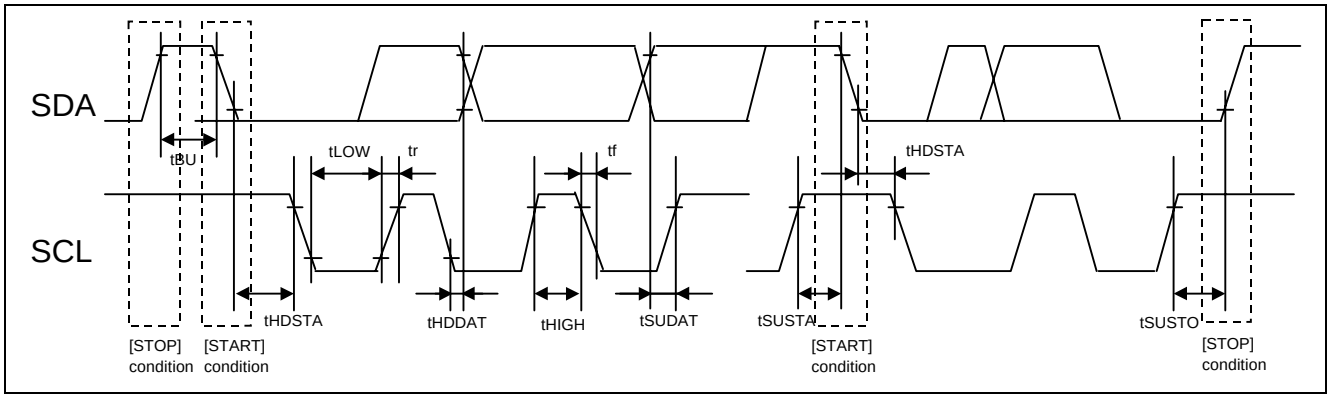
Item		Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
						min	typ	max		
SDA/SCL	High input voltage	ViH	26,27	-	SW26,27=2	2.3	-	Vcc	V	
	Low input voltage	ViL	26,27	-	SW26,27=2	-	-	1.0	V	
	High input current	IiH	26,27	-	SW25A,26,27=2 Vi=4.0V	-	-	10	µA	
	Low input current	IiL	26,27	-	SW25A,26,27=2 Vi=0.4V	-	-1	-10	µA	
SDA	Low output voltage	VoSL	27	-	SW25A,27=2 Io=3mA	-	-	0.4	V	
	Leakage current	IoSLK	27	-	SW25A,27=2 Vo=5.0V	-	-	10	µA	
ADS	High input current	ViAH	25	-	SW25,25A=2 Vi=5.0V	-	-	600	µA	
	Low input current	IiAL	25	-	SW25,25A=2 Vi=0.4V	-	-	-200	µA	
PORT	Output voltage1	Vop1	20,21	-	SW20,21=2 Io=-25mA	4.6	4.8	-	V	
	Output voltage2	Vop2	15,22	-	SW15,22=2 Io=-5mA	4.6	4.8	-	V	
	Leakage current	IopLK	15 20~22	-	SW15,20,21,22=2 output "OFF"	-	-	10	µA	
CP	High output current	IcpH	32	-	SW32=2 Vo=2.5V	±170	±300	±400	µA	
	Low output current	IcpL	32	-	SW32=2 Vo=2.5V	±55	±75	±115	µA	
	Leakage current	IcpLK	32	-	SW32=2 Vo=2.5V,output "OFF"	-	-	50	nA	
VT	Tuning drive output	Iovt	31	-	SW31=2 Vo=0.5V	-	-	2.0	mA	
Xin	Operational frequency of Crystal OSC	fxin	29	-		3.2	4.0	4.4	MHz	
	Absolute Value	Rxin	29	-		2.0	-	-	kΩ	
	Sensitivity of External signal	Vixin	29,22	SG17	SW29=2,Sine wave signal input Data(T2,T1,T0)="01X"	50	-	600	mVp-p	*14

Data input Block

(Ta=25°C,Vcc=5.0V otherwise noted.)

Item	Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
					min	typ	max		
Clock frequency	fSCL	26			0	100	400	kHz	
Bus free time	tBUF	27			1.3	-	-	µsec	
Data hold time	tHDSTA	27			0.6	-	-	µsec	
SCL LOW hold time	tLOW	26			1.3	-	-	µsec	
SCL HIGH hold time	tHIGH	26			0.6	-	-	µsec	
Set up time	tSUSTA	26,27			0.6	-	-	µsec	
Data hold time	tHDDAT	26,27			0	-	-	µsec	
Data set up time	tSUDAT	26,27			100	-	-	nsec	
Rise time	tR	26,27			-	-	300	nsec	
Fall time	tF	26,27			-	-	300	nsec	
Set up time	tSUSTO	26			0.6	-	-	µsec	

Timing chart



VIF Block1

(Ta=25°C, Vcc=5.0V otherwise noted.)

Item	Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
					min	typ	max		
Video output level	Vodet	46	SG1		0.85	1.15	1.35	Vp-p	
Sync tip voltage	VoSNK	46	SG2		1.1	1.3	1.5	V	
Video S/N	VideoS/N	46	SG2	5MHz LPF	48	50	-	dB	*1
Video out freq. response	BW	1	SG3		6	7	-	MHz	*2
Input sensitivity	VinMIN	1,37,38	SG4	Vo=-3dB point	-	45	52	dBμV	*3
Max. IF input	VinMAX	1,37,38	SG5	Vo=-3dB point	101	105	-	dBμV	*4
AGC range	GR	-		GR = VinMAX - Vin MIN	52	60	-	dB	*5
Capture range U	CR-U	46,37,38	SG9		0.6	0.8	-	MHz	*6
Capture range L	CR-L	46,37,38	SG9		1.1	1.5	-	MHz	*7
Inter modulation	IM	1	SG11		32	40	-	dB	*8
D/G	DG	1	SG12		-	3	5	%	
D/P	DP	1	SG12		-	3	5	deg	
Input impedance	Zin	37,38	-	DC	-	2k	-	Ω	
Input capacitance	Yin	37,38	-	40MHz	-	5	-	pF	
RF AGC max voltage	V23H	23	SG6		4	4.3	4.6	V	
RF AGC min voltage	V23L	23	SG7		0	0.3	0.6	V	
RFAGC Delay point	Vi23	23,37,38	SG8	@3pin open	82	85	88	dBμV	*9

VIF Block2

(Ta=25°C,Vcc=5.0V otherwise noted.)

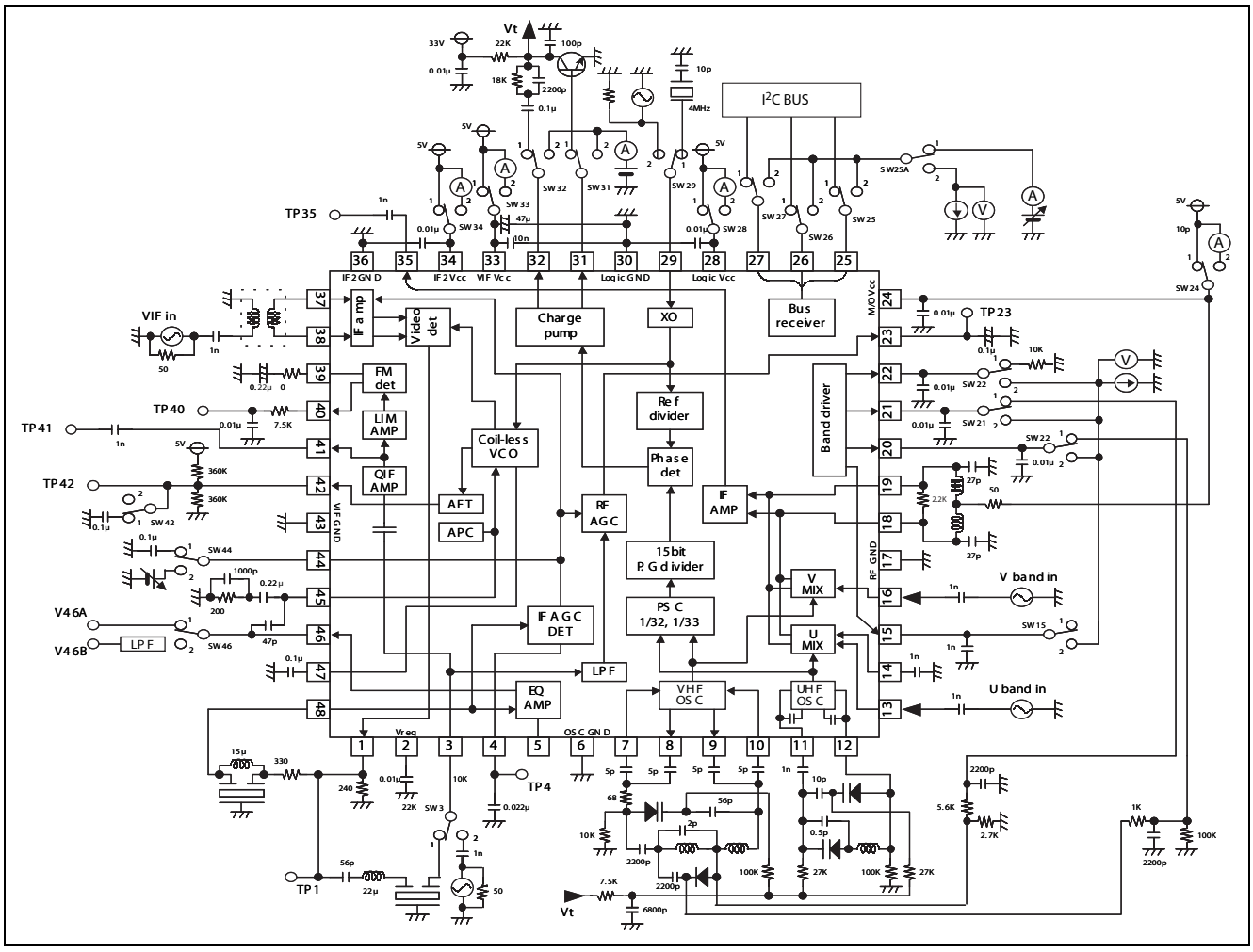
Item	Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
					min	typ	max		
Freerun frequency	fvco	42	SG17	SW42,29=2,44pin "GND" Data (T2,T1,T0="01X")	-500	-	500	kHz	*15
AFT Sensitivity	μ	42	SG10	@360k/360k 0.1μF	12	24	36	mV/kHz	*10
AFT high output voltage	V42H	42	SG10	4.3	4.7	5	V		
AFT Low output voltage	V42L	42	SG10	0	0.3	0.7	V		
AFT center voltage	V42C1	42	SG18	frequency=58.75MHz	2.4	2.5	2.6	V	
AFT center voltage	V42C2	42	SG2	frequency=45.75MHz	2.4	2.5	2.6	V	

SIF Block

(Ta=25°C,Vcc=5.0V otherwise noted.)

Item	Symbol	Measure point	Input SG	Condition switches set to position "1" unless otherwise noted	Limits			Unit	Note
					min	typ	max		
Audio out level	VoAF	40	SG13	SW3=2 @Pin39:0.22µF	500	770	1040	mVrms	
Audio out THD	THDAF	40	SG13	SW3=2 @Pin39:0.22µF	-	0.4	0.9	%	
AF S/N	AF S/N	40	SG16	SW3=2 @Pin39:0.22µF	51	56	-	dB	*11
Limiting sensitivity	LIM	3,40	SG14	SW3=2 S/N=30dB Point	-	50	55	dBµV	*12
AMR	AMR	40	SG15	SW3=2	44	50	-	dB	*13
QIF output	VoQIF	41	SG16	SW3=2	86	92	-	dBµV	

Measurement Diagram



Input Signal

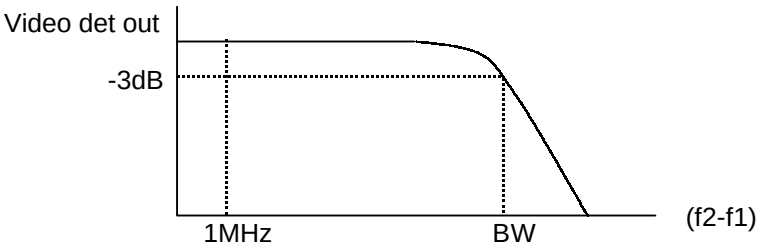
SG	50ohm termination			
1	f0=45.75MHz	Vi=90dBµV	fm=20kHz	AM=77.8%
2	f0=45.75MHz	Vi=90dBµV	CW	
3	f1=45.75MHz f2=Frequency Variable	Vi=90dBµV Vi=70dBµV	CW CW	} mixed signal
4	f0=45.75MHz	Level Variable	fm=20kHz	AM=77.8%
5	f0=45.75MHz	Level Variable	fm=20kHz	AM=14.0%
6	f0=45.75MHz	Vi=80dBµV	CW	
7	f0=45.75MHz	Vi=110dBµV	CW	
8	f0=45.75MHz	Level Variable	CW	
9	f0=Frequency Variable	Vi=90dBµV	fm=20kHz	AM=77.8%
10	f0=Frequency Variable	Vi=90dBµV	CW	
11	f1=45.75MHz f2=42.17MHz f3=41.25MHz	Vi=90dBµV Vi=80dBµV Vi=80dBµV	CW CW CW	} mixed signal
12	f0=45.75MHz	Sync Tip Level 90dBµ 10 stair-steps waveform	TV moduration=87.5%	
13	f0=4.5MHz	Vi=90dBµV	fm=1kHz	+/- 25kHz dev
14	f0=4.5MHz	Level Variable	fm=1kHz	+/- 25kHz dev
15	f0=4.5MHz	Vi=90dBµV	fm=1kHz	AM=30%
16	f0=4.5MHz	Vi=90dBµV	CW	
17	f0=4.0MHz	Level Variable	CW	
18	f0=58.75MHz	Vi=90dBµV	CW	

Measurement of Electrical Characteristic Notes

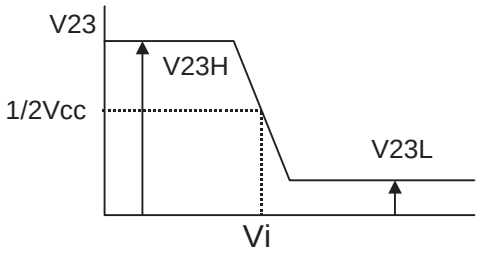
1. Video S/N
   Input SG2 to VIF IN and measure the video out (Pin 46) noise in r.m.s. at TP46B through a 5MHz (-3dB) L.P.F.

$$S/N=20\log\left(\frac{0.7\times Vodet}{NOISE}\right)\ (dB)$$

2. Video Band Width
   1. Measure the 1MHz component level of Video output TP1 with a spectrum analyzer when SG3 (f2=44.75MHz) is input to VIF IN. At that time, measure the voltage at TP44 with SW8, set to position 2, and then fix V8 at that voltage.
   2. Reduce f2and measure the value of (f2-f1) when the (f2-f1) component level reaches -3dB from the 1MHz component level as shown below.

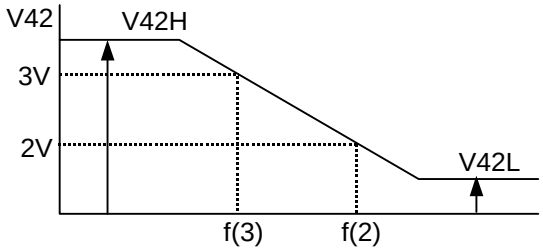


3. Input sensitivity
   Input SG4 (Vi=90dBμ) to VIF IN , and then gradually reduce Vi and measure the input level when the 20kHz component of Video output TP46A reaches -3dB from Vo det level.
4. Maximum Allowable Input
   1. Input SG5 (Vi=90dBμ) to VIF IN, and measure the level of the 20kHz component of Video output.
   2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.
5. AGC control Range
   GR=VinMAX-VinMIN (dB)
6. Capture range U
   1. Increase the frequency of SG9 until the VCO is out of locked-oscillation
   2. And decrease the frequency of SG9 and measure the frequency fU when the VCO is locked.
      CR-U=fU-45.75 (MHz)
7. Capture range L
   1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
   2. And increase the frequency of SG9 and measure the frequency fL when the VCO is locked.
      CR-L=45.75-fL (MHz)
8. Inter modulation
   1. Input SG11 to VIF IN, and measure video output TP9 with an oscilloscope.
   2. Adjust AGC filter voltage V44 so that the minimum DC level of the output waveform is 1.5V.
   3. At that time, measure TP1 with a spectrum analyzer The inter modulation is defined as a difference between 0.92MHz and3.58 MHz frequency components.
9. RF AGC Operating Voltage:
   Input SG8 to VIF IN and gradually reduce Vi and then measure the input level when RF AGC output reaches 1/2Vcc, as shown below.



10. AFT sensitivity, Maximum AFT voltage, Minimum AFT voltage
    1. Input SG10 to VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP42 is 3(V). This frequency is named f(3).
    2. Set the frequency of SG10 so that the AFT output voltage is 2(V). This frequency is named f(2).
    3. IN the graph shown below, maximum and minimum DC voltage are V42H and V42L, respectively.

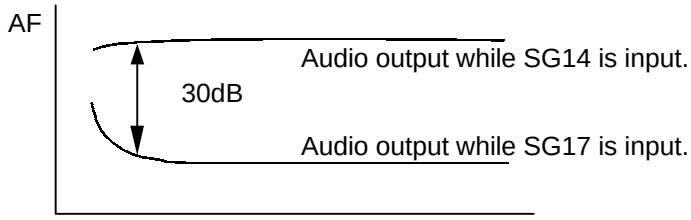
$$\mu = \frac{1000mV}{f(2)-f(3)\ (KHz)}\ (mV/KHz)$$



11. AF S/N
    1. Input SG19 to LIM IN, and measure the output noise level of Audio output (TP40). This level is named VN.

$$S/N = 20\log\left(\frac{VoAF}{VN}\right)\ (dB)$$

12. Limiting Sensitivity
    1. Input SG14 to LIM IN, and measure the 1kHz component level of AF output TP40.
    2. Input SG17 to LIM IN, and measure the noise level of AF output TP40 .
    3. The input limiting sensitivity is defined as the input level when the difference between each 1kHz components of audio output (TP40) is 30dB, as shown below.



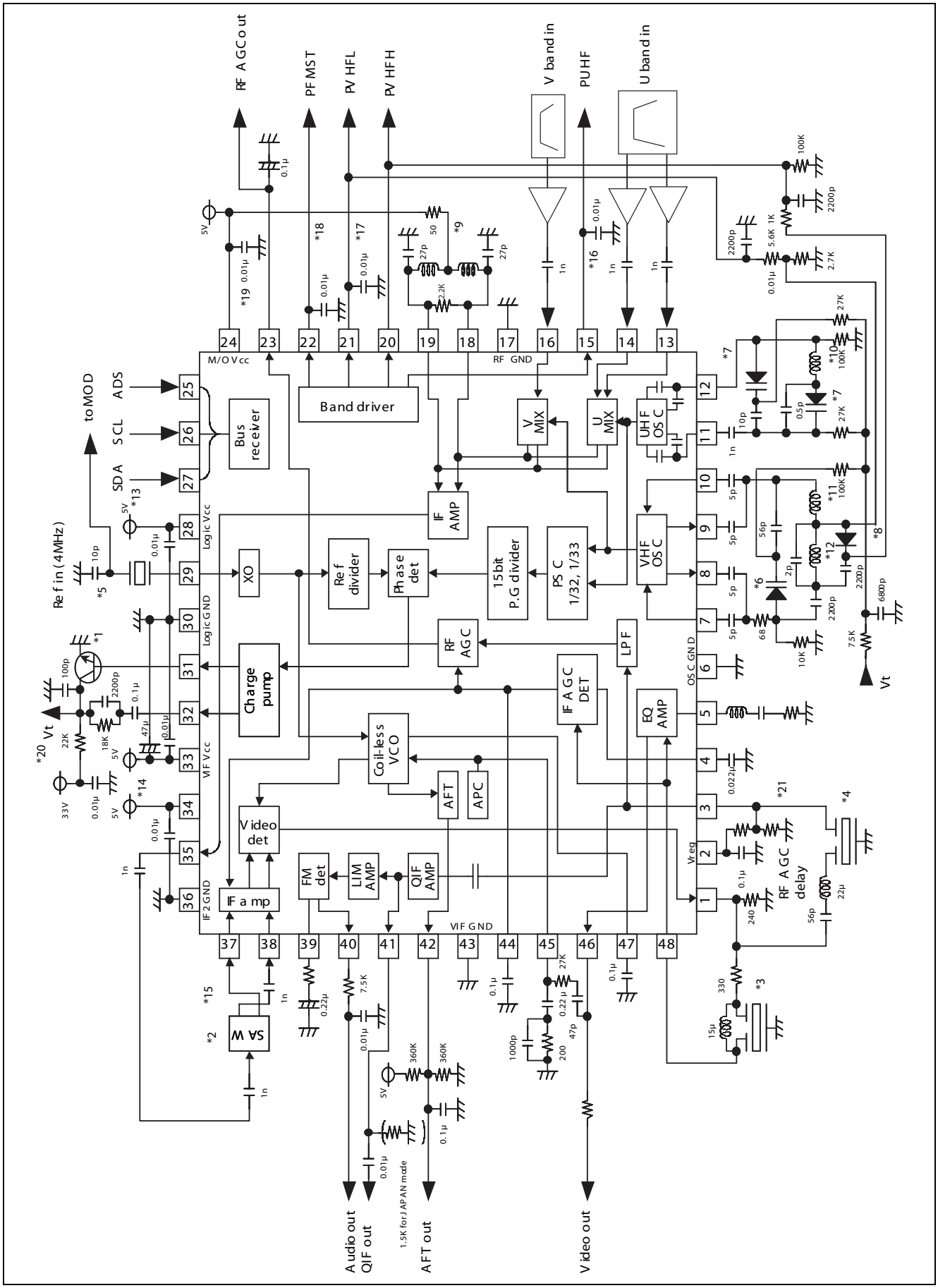
13. AM Rejection
    1. Input SG15 to LIM IN, and measure the output level of Audio output (TP40). This level is named VAM.
    2. AMR is

$$AMR = 20\mathrm{Log}\left(\frac{Vo\ \ AF\ \ (mVrms)}{VAM\ \ \ (mVrms)}\right)\ \ (dB)$$

14. Xin sensitivity of external signal
    1. Input data that Control byte data CP,T2,T1,T0 is "0100" and Rsa,Rsa is"01"
    2. The Reference frequency is output to Pin 22, measure the frequency with counter.
    3. Input sensitivity is defined as the input level when the frequency is less than plus-or-minus 1ppm of 31.25kHz.
15. Freerun frequency
    1. Input data that Control byte data CP,T2,T1,T0 is "01X".
    2. The Reference frequency is output to Pin 42, measure the frequency with counter. This frequency is named fmoni.

    Freerun frequency (foUS) is 52.9524[MHz] - fmoni x 9 [MHz]
    Freerun frequency (foJP) is 65.9512[MHz] - fmoni x 9 [MHz]

Application Example



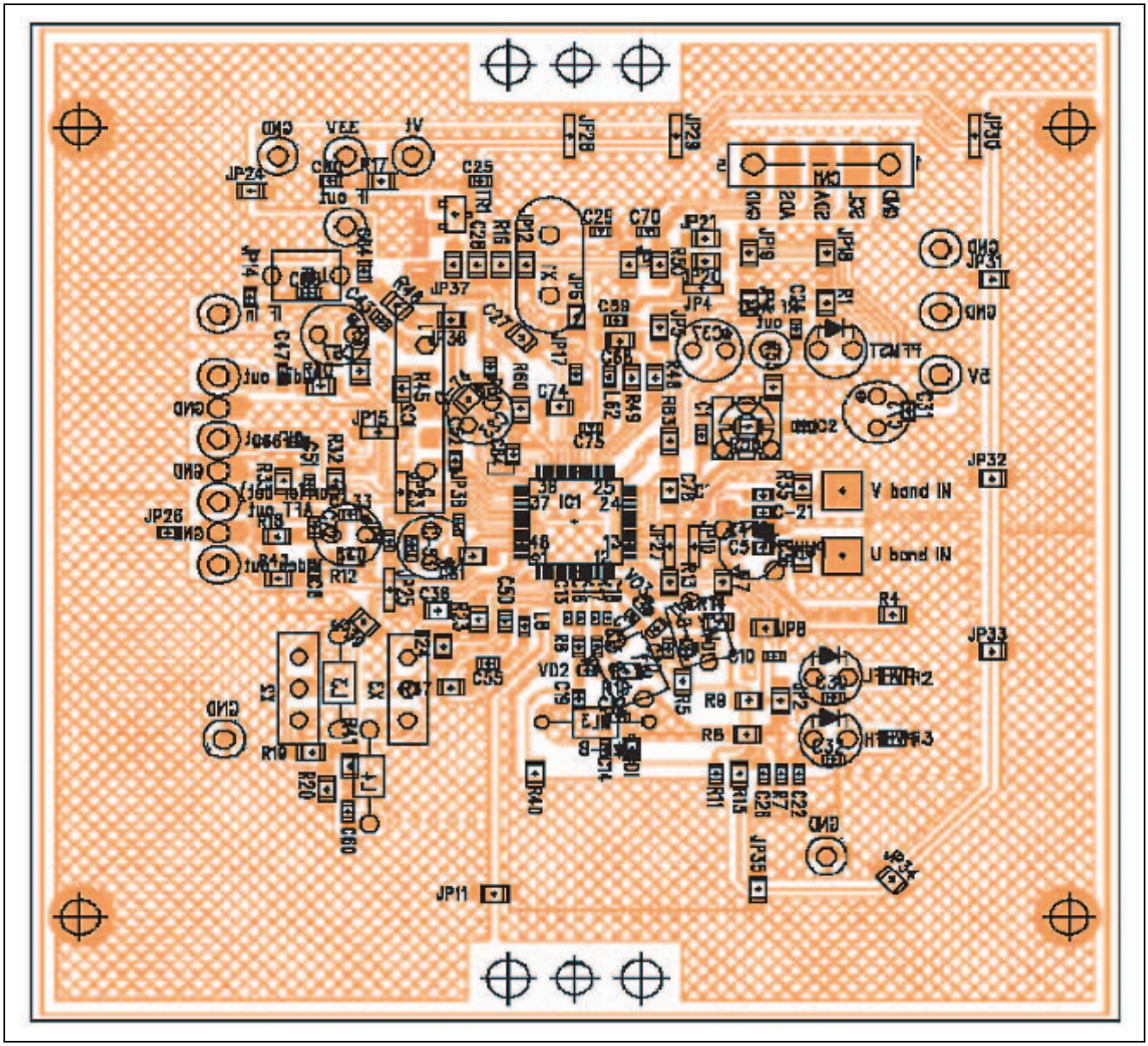
Application Note

*1 2SC2643 equivalent made by Renesas
*2 45.75MHz SAW Filter made by EPCOS
*3 4.5MHz Trap: TPSRA4M50B00 made by Murata
*4 4.5MHz B.P.F.: SFSRA4M50EF00 made by Murata
*5 HC-49/U equivalent made by Daishinku. Load capacitance=20pF,Motinal resistance: Less 300 Ω
*6,7 HVC306B, HVC306C equivalent made by Renesas
*8 HSC277 equivalent made by Renesas
*9 0.1mm 3mm ϕ 6t x2 P886ANS-0194VN made by TOKO
*10 0.5mm 2.4mm ϕ 1.5t
*11 0.5mm 2.4mm ϕ 2.5t
*12 0.5mm 2.4mm ϕ 8.5t
*13,14 The bypass capacitor of Vcc is arranged near the LogicGND pin.
*15 In order to mitigate the surroundings lump by the VIF input, the balanced connection from a SAW filter to the VIF input pin of 37.38 recommends a putter which serves as a 1t coil by Tip C or the jumper.
*16-19 In order to stop digital beat which goes via the port output from Logic Vcc, bypass capacitor arranged near the port output pin.
*21 It is high impedance. keep away from VideodetOUT and EQ F/B pin.

Notes about the handling of IC

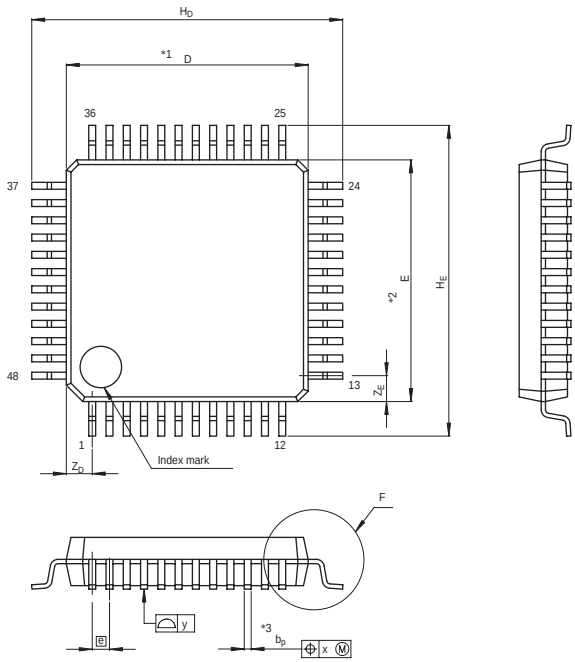
*20 The direct power supply impression to Vt terminal is forbidden. When power supply impression is required, please impress through the resistance for current restrictions. Depending on the case, it is drive current from 31 pin, and excessive collector current flows and breaks to an external transistor.
Because there is a possibility of also destroying IC by the destruction.
* Since this IC is using the detailed process, be careful of serge enough.
Especially careful 1,7,8,9,10,25,26,27,32,48 pins.

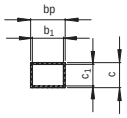
Application Board Example



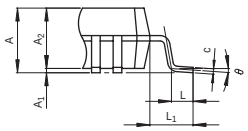
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	——	1.4	——
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	——	——	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	——	0.20	——
c	0.09	0.145	0.20
c_1	——	0.125	——
θ	0°	——	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.10
Z_D	——	0.75	——
Z_E	——	0.75	——
L	0.35	0.5	0.65
L_1	——	1.0	——

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