14-Line SCSI Bus Terminators

FEATURES

- Auto Selection of S/E or LVD SCSI Termination
- 2.7-V to 5.25-V TERMPWR Range
- Meets SCSI-1, SCSI-2, SPI-2 (ULTRA-2), SPI-3 (ULTRA-160) and SPI-4 (ULTRA-320) Standards
- Integrated SPI-3 Mode Change Delay Filter
- Bus Mode Status Pins
- Differential Failsafe Bias
- Thermal Package
- On-Chip Thermal Shutdown Circuit
- Active Negation
- Hot Swap Compatible
- Pin Compatible with UCC5628
- Lead (Pb)-Free SQFP-48 Package

APPLICATIONS

- Disk Array (RAID)
- Storage Area Networks (SAN)
- Network Attached Storage (NAS)
- SCSI Cable
- Server and Workstation
- Industrial Computers
- High-End Personal Computers

DESCRIPTION

The SiP5668 provides active bus termination suitable for all SCSI bus operational modes from SCSI-1 through SPI-4 (Ultra 320). The termination includes impedance matching of the SCSI bus to minimize signal reflections from the end of the bus, as well as required SCSI bus biasing for either S/E (single ended) or LVD (low voltage differential) operation.

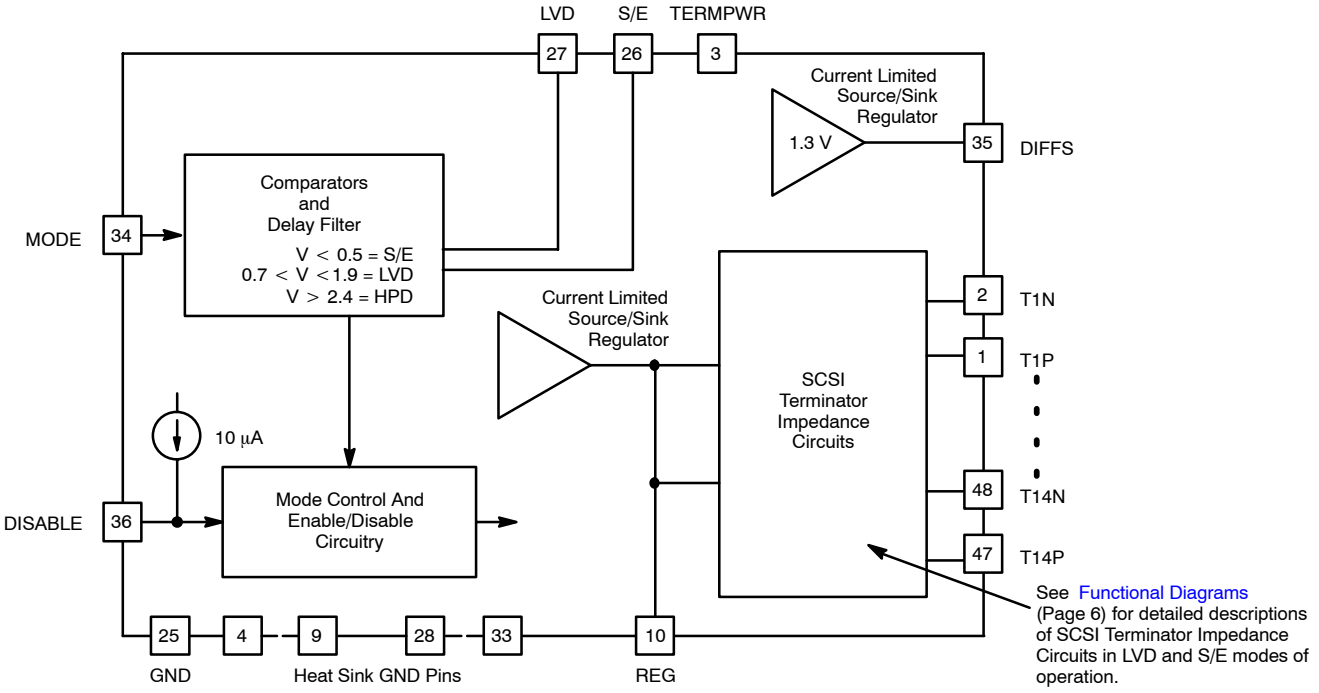
An integrated mode change delay filter in the SIP5668 eliminates the need for a bulky 4.7-µF low pass filter capacitor to be compliant with SPI-3 mode change timing requirements.

The SiP5668 has fourteen (14) output channels (T1–T14). Each output channel provides termination for one SCSI data signal, parity signal or control signal. Two SiP5668 ICs provide complete termination for a wide SCSI bus.

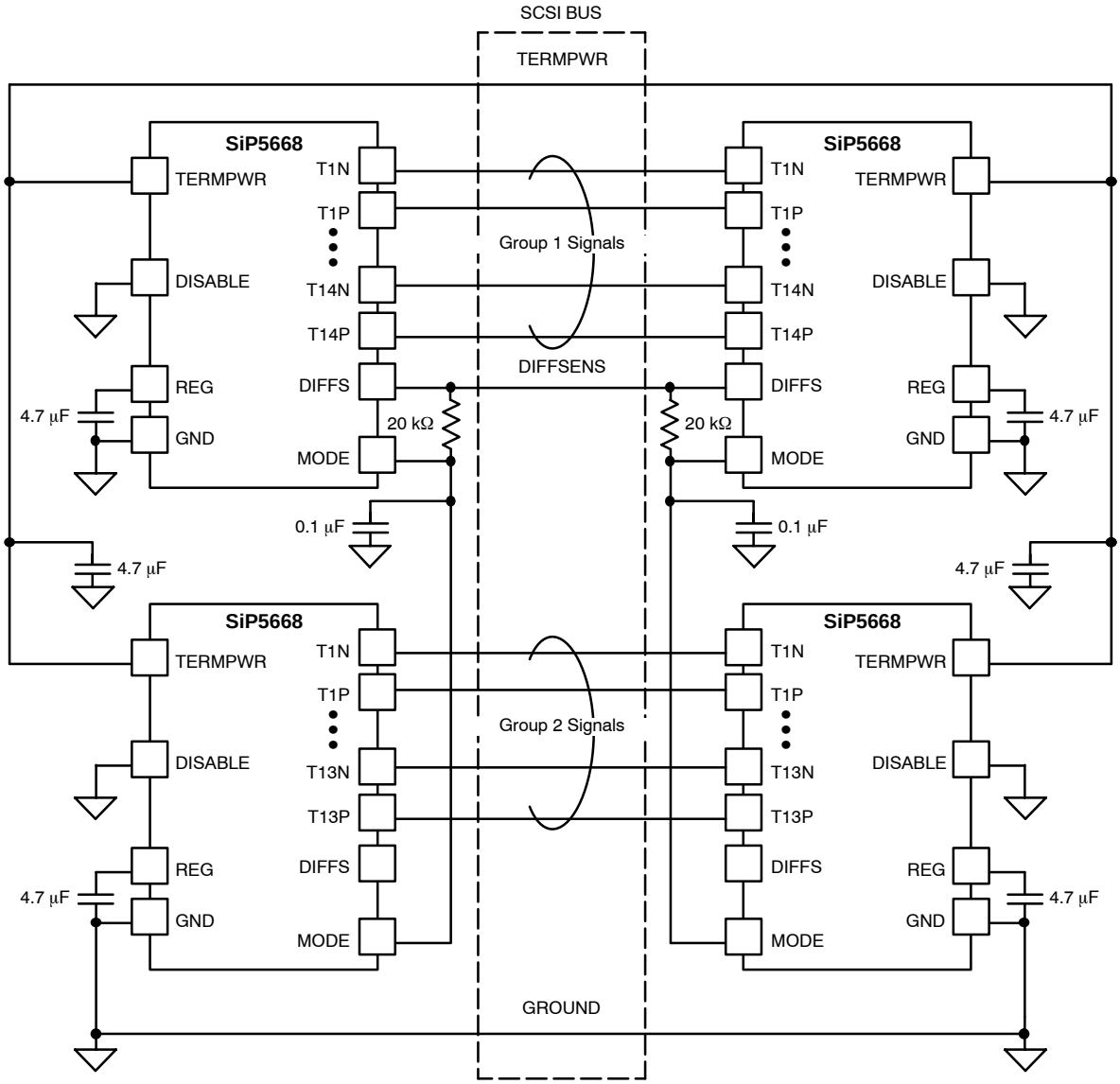
The SiP5668 senses the operational state of the SCSI bus via the DIFFSENS bus signal, and automatically switches to S/E or LVD operation as required. It cannot be used on an HPD (high power differential) SCSI bus, and goes into high impedance mode when the voltage on the DIFFSENS line indicates HPD operation. The SiP5668 also presents high impedance to the SCSI bus if the DISABLE pin is asserted, or if TERMPWR is removed from the IC.

The SiP5668 is available in a lead (Pb)-free SQFP-48 package for operation over the temperature range of 0 to 70 °C.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION DIAGRAM



Group 1 Signals:

DB(0), DB(1), DB(2), DB(3), DB(4), DB(5), DB(6), DB(7), DB(P), DB(12), DB(13), DB(14), DB(15), DB(P1)

Group 2 Signals:

ATN, BSY, ACK, RST, MSG, SEL, C/D, REQ, I/O, DB(8), DB(9), DB(10), DB(11)

ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

TERMPWR . . . . . 6 V
TXN, TXP . . . . . –0.3 to 6 V
MODE, DISABLE, M/S, STATUS . . . . . –0.3 to 6 V

Storage Temperature . . . . . –65 to 125 °C
Junction Temperature . . . . . 150 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

TERMPWR . . . . . 2.7 V to 5.25 V

Operating Temperature Range (T_A) . . . . . 0 to 70 °C

SPECIFICATIONS

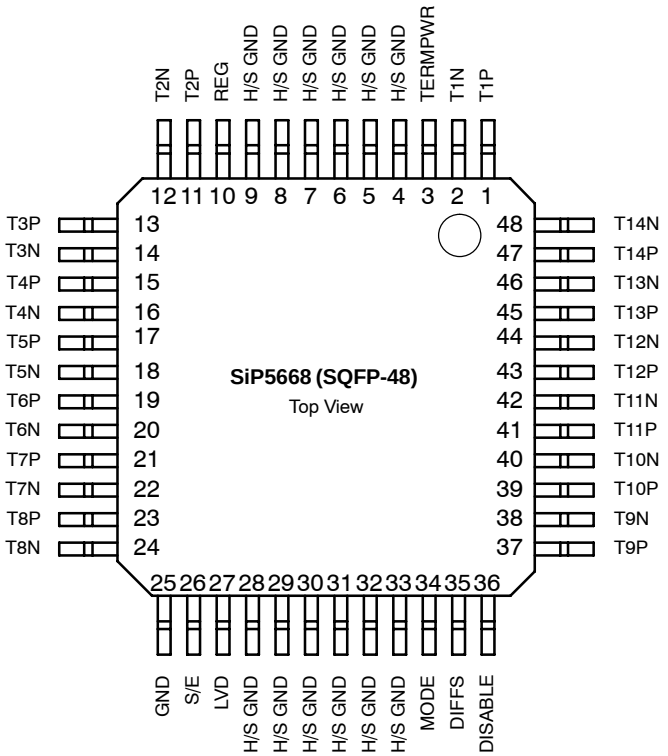
Parameter	Symbol	Test Conditions Unless Specified TERMPWR = 2.7 to 5.25 V, DISABLE = 0 V $T_A = T_J$ = 0 to 70 °C		Limits Min[a]	Typ[b]	Max[a]	Unit
SCSI Channels (T1 to T14), LVD Operation							
Differential Impedance	Z_{DIFF}	MODE = 1.3 V		100	105	110	Ω
Common Mode Impedance	Z_{CM}			120	140	160	
Differential Failsafe Bias	V_{DIFF}			100	112	125	mV
Common Mode Bias	V_{CM}			1.15	1.25	1.35	V
SCSI Channels (T1 to T14), S/E Operation							
Impedance	$Z_{S/E}$	MODE = 0 V		100	108	116	Ω
Bias Voltage	$V_{S/E}$			2.5	2.7	3.0	V
Output Current	$I_{S/E}$	MODE = 0 V	Channel Voltage = 0.2 V	–25.4	–23	–20.5	mA
			Channel Voltage = 0.5 V	–22.4			
GND Driver Impedance	Z_{GS}	MODE = 0 V, I_{TEST} = 10 mA			30	60	Ω
SCSI Channels (T1 to T14), Termination Disabled							
Channel Leakage[c]	I_L	Channel Voltage = 0 to 5 V		–500	0	500	nA
Channel Capacitance[c, d]	C_T	Referenced to GND			3		pF
SCSI Regulator, LVD Mode							
Output Voltage	$V_{REG(LVD)}$	0.5 V ≤ V_{CM} ≤ 2.0 V[e]		1.15	1.25	1.35	V
Source Current	$I_{SO(LVD)}$	V_{REG} = 0 V		–1000	–600	–400	mA
Sink Current	$I_{SI(LVD)}$	V_{REG} = 4 V		200	400	700	
DIFFSENS Regulator							
Output Voltage	V_{DIFFS}	–5 mA ≤ I_{DIFFS} ≤ 50 µA		1.2	1.3	1.4	V
Source Current	$I_{SO(DIFFS)}$	V_{DIFFS} = 0 V		–15	–8	–5	mA
Sink Current	$I_{SI(DIFFS)}$	V_{DIFFS} = 2.75 V		50	100	200	µA
SCSI Regulator, S/E Mode							
Output Voltage	$V_{REG(S/E)}$	0.2 V ≤ V_{CM} ≤ 4.0 V[f]		2.5	2.7	3.0	V
Source Current	$I_{SO(S/E)}$	V_{REG} = 0 V		–1000	–600	–400	mA
Sink Current	$I_{SI(S/E)}$	V_{REG} = 4 V		200	400	700	
DISABLE Input							
Input Threshold	$V_{TH(DIS)}$			0.8	1.0	1.2	V
Input Current	$I_{IN(DIS)}$	0 V ≤ $V_{DISABLE}$ ≤ 1.2 V		–30	–10	–3	µA
		$V_{DISABLE}$ > 1.2 V		–30	0	10	
MODE Input							

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified TERMPWR = 2.7 to 5.25 V, DISABLE = 0 V $T_A = T_J$ = 0 to 70 °C	Limits			Unit
			Min[a]	Typ[b]	Max[a]	
MODE Input						
S/E to LVD Threshold	$V_{TH(S/E)}$		0.5	0.6	0.7	V
LVD to HPD Threshold	$V_{TH(HPD)}$		1.9	2.1	2.4	
Input Current	$I_{IN(MODE)}$	0 V ≤ V_{MODE} ≤ 5.25 V	–1	0	1	µA
Mode Change Delay	t_{DEL}		100	200	400	ms
STATUS Output Pins (LVD, S/E)						
Source Current	$I_{SO(STAT)}$	TERMPWR = 2.7 V, V_{PIN} = 2.4 V		–10	–5	mA
Sink Current	$I_{SI(STAT)}$	V_{PIN} = 0.4 V	3	6		
THERMAL Shutdown						
Shutdown Temperature[d]	T_{OFF}	Rising Temperature		160		°C
Hysteresis[d]	T_{HYS}			10		
TERMPWR Supply						
LVD Mode	$I_{DD(LVD)}$	MODE = 1.3 V, Channels Unloaded		25	35	mA
S/E Mode	$I_{DD(S/E)}$	MODE = 0 V, Channels Unloaded		10	20	
HPD Mode	$I_{DD(HPD)}$	MODE = 3 V		10	20	
Disabled Mode	$I_{DD(DIS)}$	DISABLE = 3 V		500	1000	µA

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. MODE = 3 V and/or DISABLE = 3 V and/or TERMPWR = 0 V.
d. Guaranteed by design, not subject to production test.
e. V_{CM} applied simultaneously to Line PLUS and Line MINUS pins of all SCSI channels T1-T14.
f. V_{CM} applied simultaneously to Line MINUS pins of all SCSI channels T1-T14.

PIN CONFIGURATION AND ORDERING INFORMATION

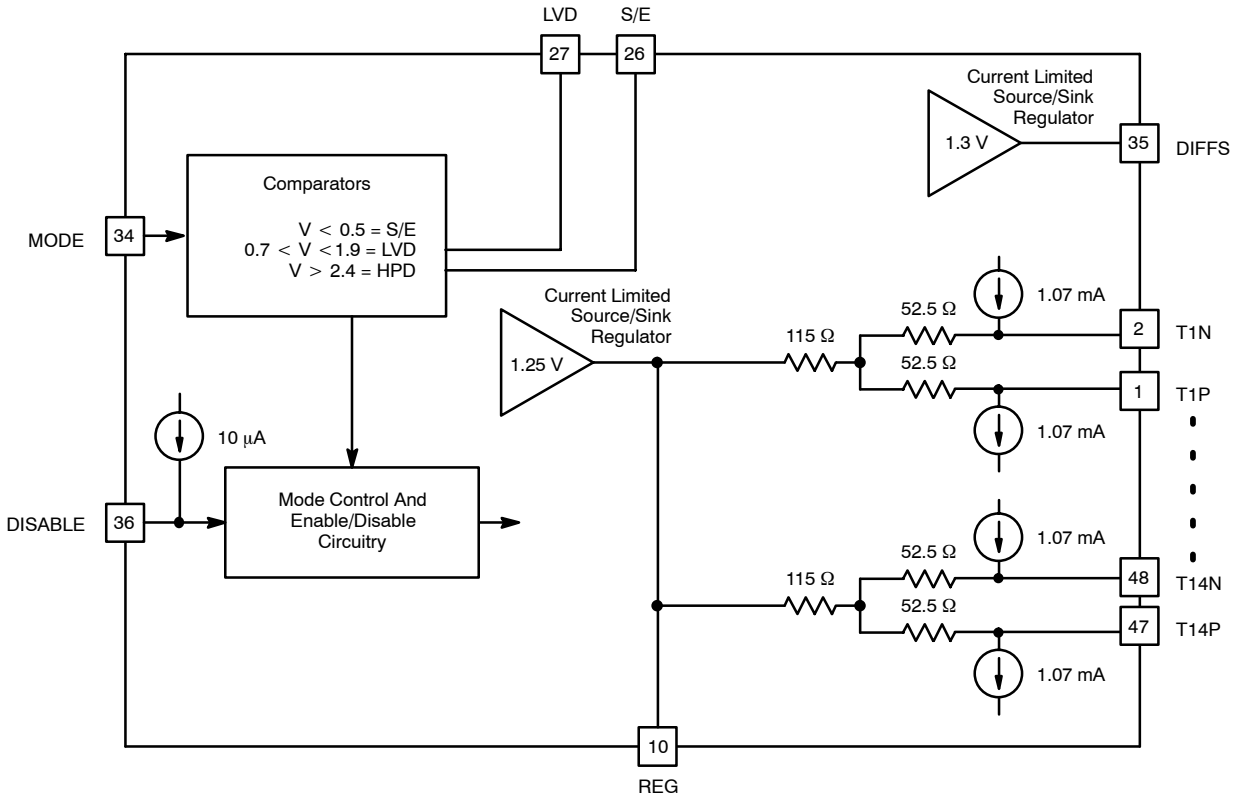


ORDERING INFORMATION		
Part Number	**Temperature Range**	**Marking**
SiP5668CS-TR—E3	0 to 70°C	SiP5668CS

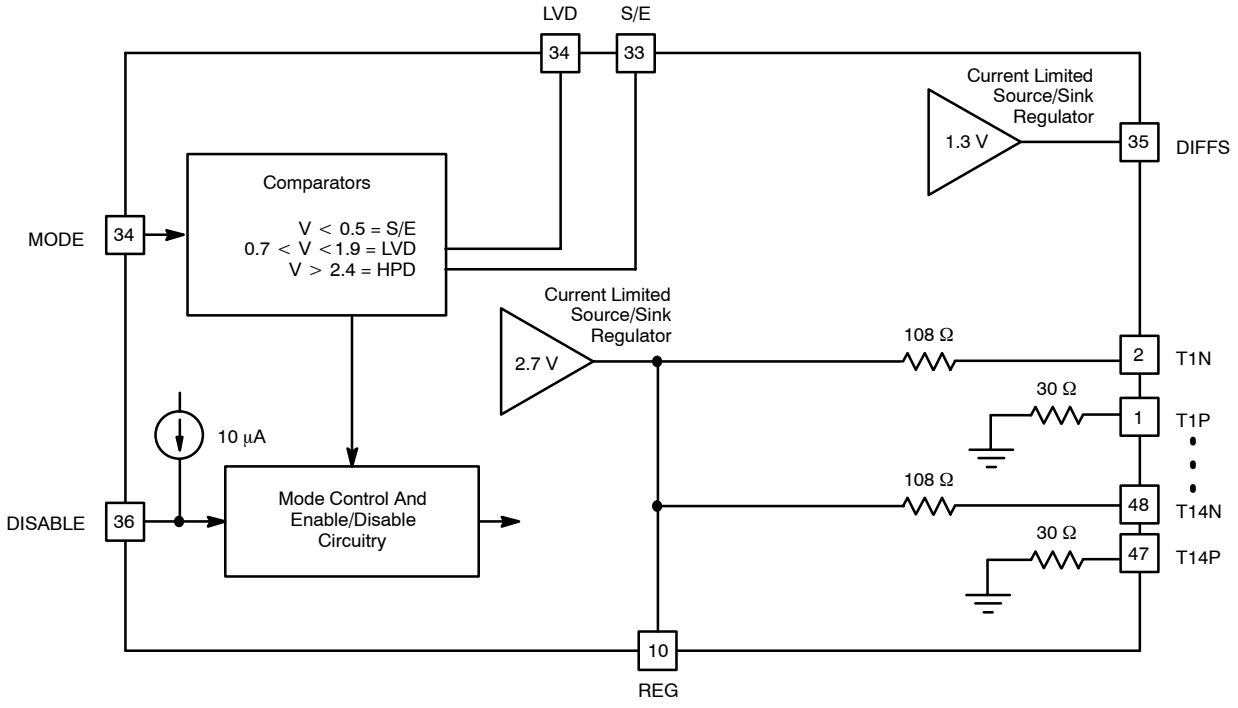
PIN DESCRIPTION

Pin	Name	Function
1, 11, 13, 15, 17, 19, 21, 23, 25, 37, 39, 41, 43, 45, 47	TXP; X = 1...14	Positive terminator channel pins. Provide positive signal line termination in LVD operation, and are connected to GND through low impedance in S/E operation. In HPD, DISABLE, or power off condition these pins present high impedance to the SCSI bus.
2, 12, 14, 16, 18, 20, 22, 24,26, 38, 40, 42, 44, 46, 48	TXN; X = 1...14	Negative terminator channel pins. Provide negative signal line termination in LVD operation, and line termination for S/E operation. In HPD, DISABLE, or power off condition these pins present high impedance to the SCSI bus.
3	TERMPWR	Power for the terminator IC. Connect to the TERMPWR lines on the SCSI bus and decouple with a 4.7-μF capacitor to GND at the IC.
4, 5, 6, 7, 8, 9, 28, 29, 30, 31, 32, 33	H/S GND	Heat sink ground. Should be connected to as large a grounded heat sink area on the PC board as is practical.
10	REG	SCSI regulator output. Connect a 4.7-μF bypass capacitor from this pin to GND.
25	GND	Electrical ground connection for the terminator IC. Connect to the ground lines of the SCSI Bus
26, 27	S/E, LVD	Status output pins. Respective pins are high when the terminator detects the corresponding mode of operation on the SCSI bus, and low otherwise.
34	MODE	SCSI MODE select pin. Connect to the DIFFSENS line of the SCSI bus to sense the present mode of operation on the bus. An internal time delay filter is provided but it is recommended to decouple MODE from the DIFFSENS signal with a 20-kΩ/0.1-μF anti-aliasing filter for reliable operation in noisy environments.
35	DIFFS	DIFFSENS regulator output. Connect to the DIFFSENS line of the SCSI bus to bias the mode selection function.
36	DISABLE	Chip disable. There is a small (nominal 10 μA) pull up current on this pin. Pull this pin to GND to enable bus termination. When this pin is left floating or pulled high all SCSI channel pins present high impedance to the SCSI bus, and the SCSI regulator and DIFFSENS regulator are both disabled.

FUNCTIONAL BLOCK DIAGRAM—LVD OPERATION

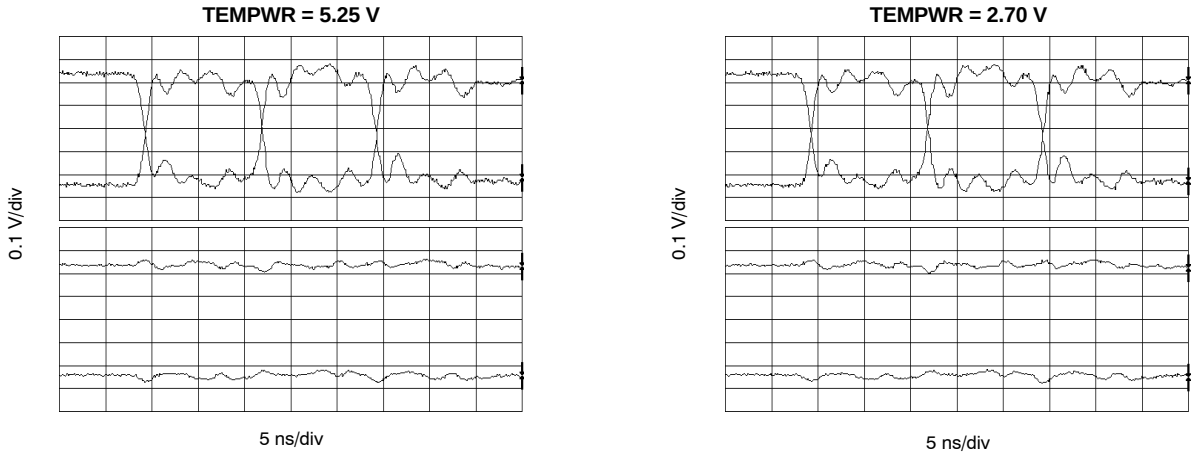


FUNCTIONAL BLOCK DIAGRAM—S/E OPERATION



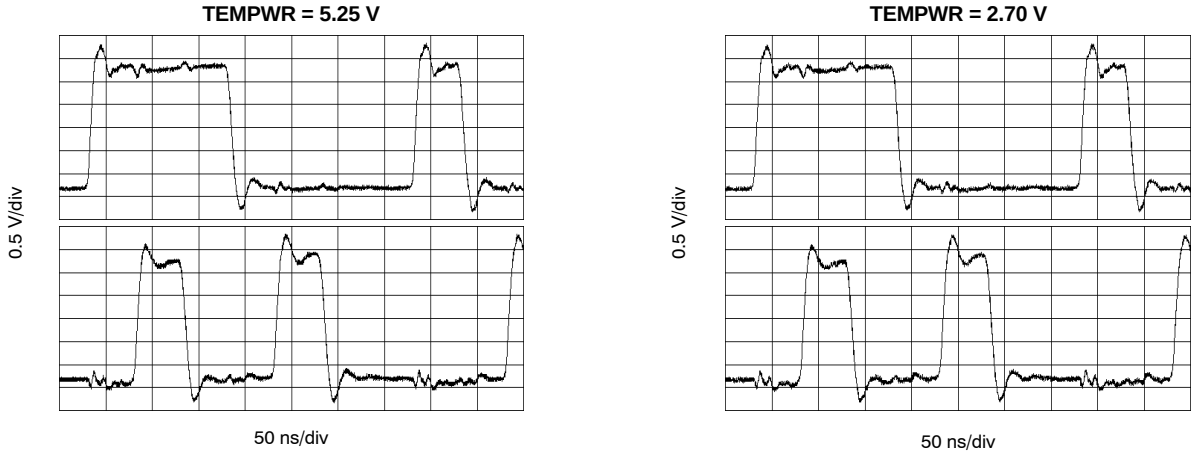
LVD WAVEFORMS

160 Mbyte/sec data transfer. Top panel DB10 T- and T+ signals. Bottom panel DB9 T− and T+ signals. All bits except DB9 toggling at maximum data rate.



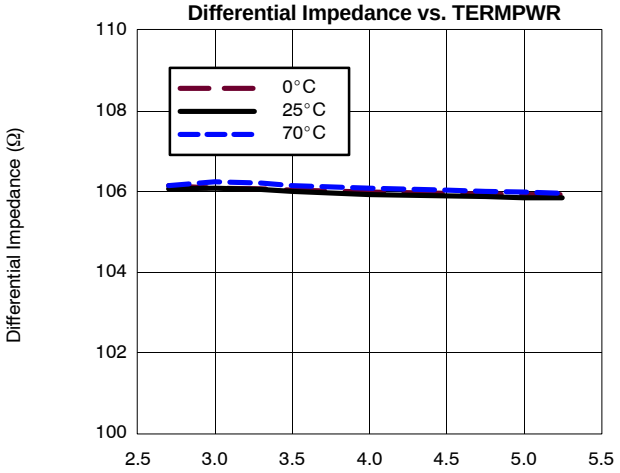
S/E WAVEFORMS

40 Mbyte/sec data transfer. Top panel DB10 T- signals. Bottom panel DB9 T− signals.

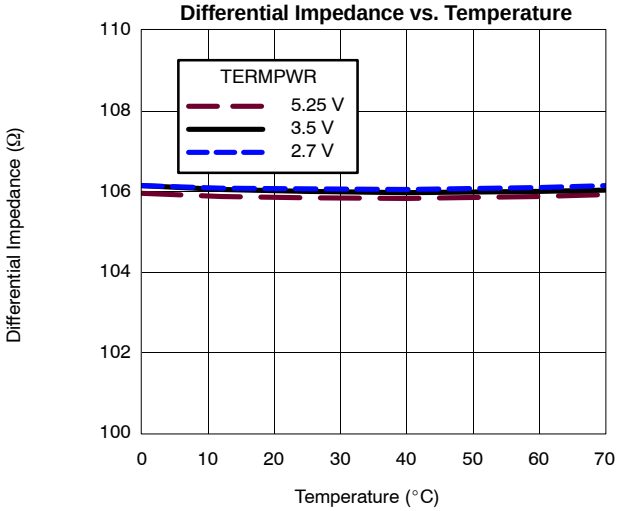


LVD TYPICAL CHARACTERISTICS

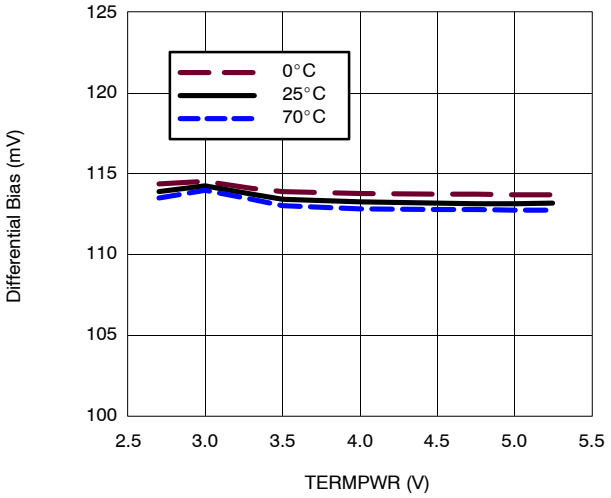
Differential Impedance vs. TERMPWR



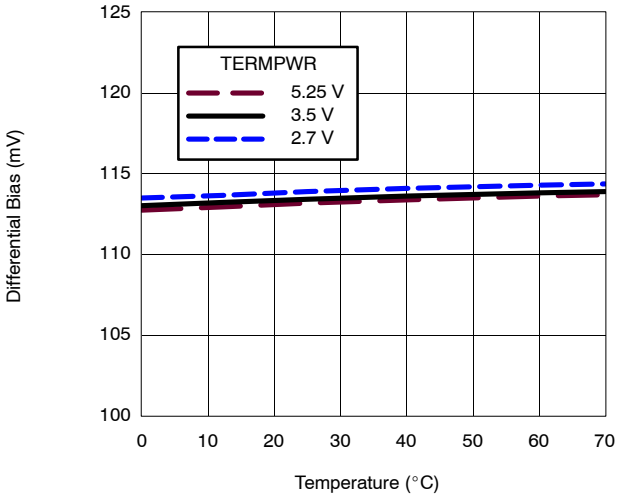
Differential Impedance vs. Temperature



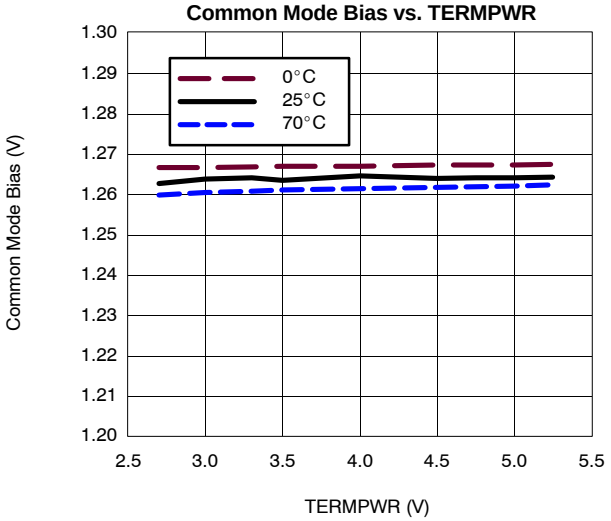
Differential Fail-Safe Bias vs. TERMPWR



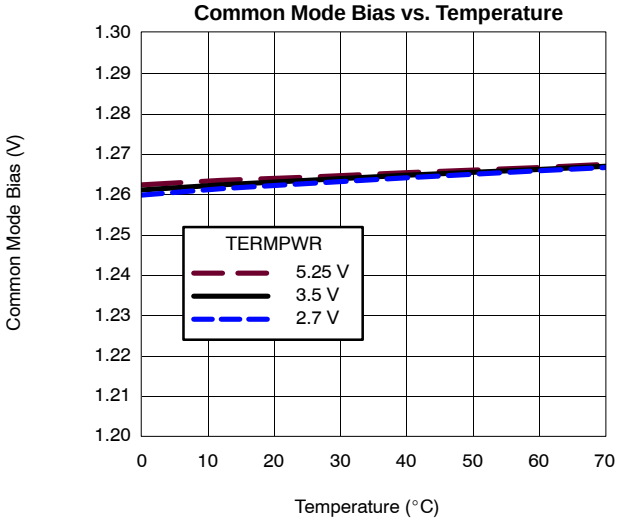
Differential Fail-Safe Bias vs. Temperature



Common Mode Bias vs. TERMPWR

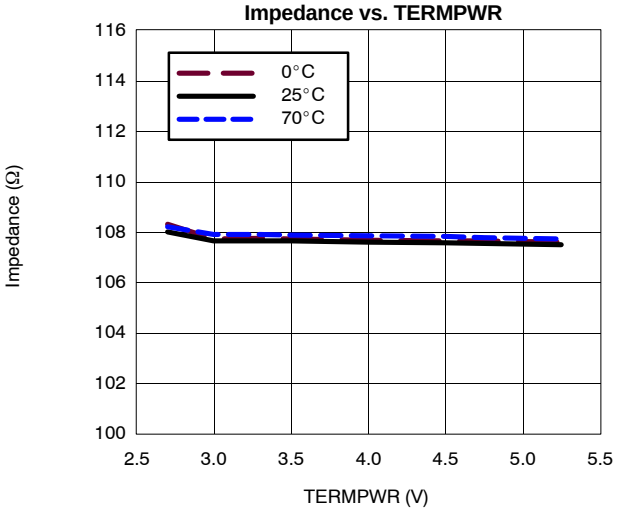


Common Mode Bias vs. Temperature

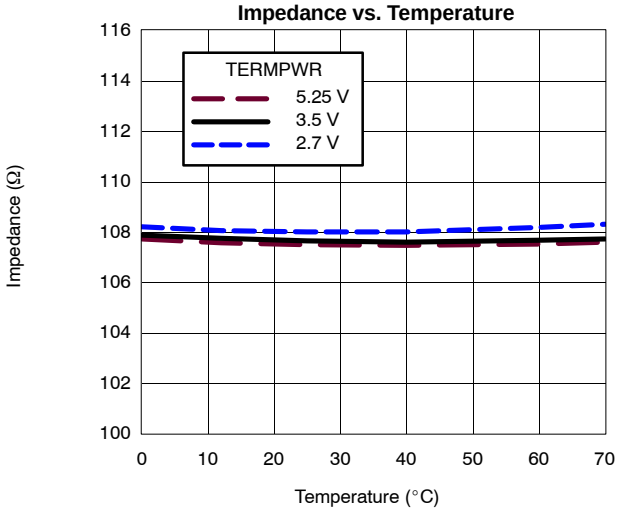


SE TYPICAL CHARACTERISTICS

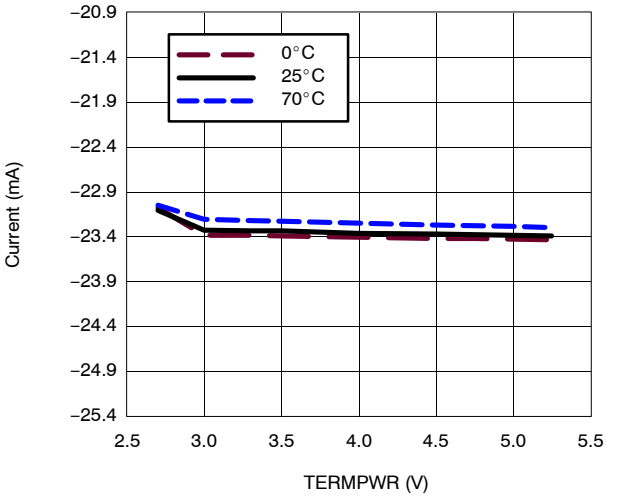
Impedance vs. TERMPWR



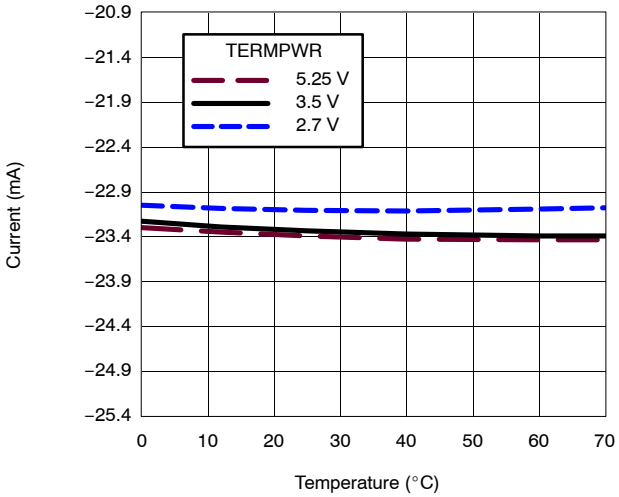
Impedance vs. Temperature



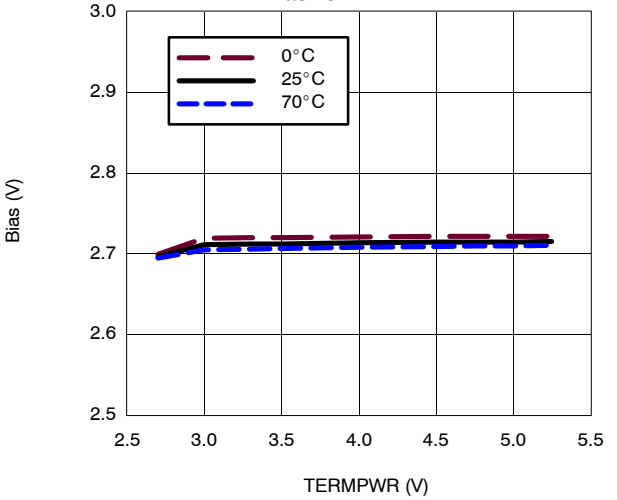
Output Current @ 0.2 V vs. TERMPWR



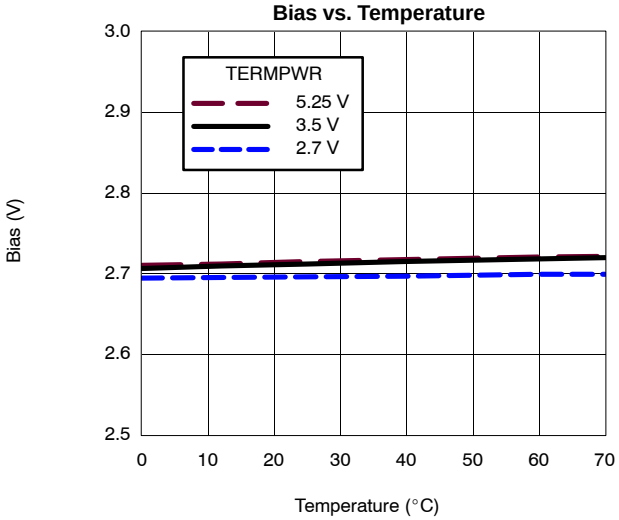
Output Current @ 0.2 V vs. Temperature



Bias vs. TERMPWR



Bias vs. Temperature



DETAILED OPERATION

The SiP5668 is a multimode active terminator IC, which detects the operating mode of the SCSI bus, and switches to the appropriate termination configuration accordingly.

Two SiP5668 terminators are required at each end of a wide SCSI bus to terminate 27 lines (18 data, 9 control). In LVD mode the SiP5668 provides 105-Ω differential impedance and 112-mV differential bias between each TN/TP pair of terminator lines. In S/E mode the SiP5668 provides 108-Ω impedance and 2.7-V pull-up on each TxN pin, and low impedance to ground on each TxP pin. In HPD mode the SiP5668 disconnects from the bus and presents high impedance to all TN/TP lines.

Each SiP5668 IC has a 1.3-V DIFFSENS regulator output that can be used to drive the DIFFSENS line of a SCSI bus. The DIFFSENS regulator attempts to drive the DIFFSENS control signal to 1.3 V, but is current limited so that S/E or HPD devices on the SCSI bus can override the DIFFSENS regulator and put the bus into S/E or HPD mode of operation.

The MODE pin senses the operational state of the SCSI bus by detecting the voltage on the DIFFSENS control line. There is an integrated 200-ms glitch filter on the MODE imput for reliable operation in noisy environments.

On power up, the SiP5668 initially defaults to a high impedance state on the termination pins. If the MODE pin detects S/E or LVD level on the DIFFSENS signal of the SCSI bus the SiP5668 will wait a standard delay (200 ms typical) before changing its operating mode. During regular operation if the MODE pin detects another bus mode change the SiP5668 again waits a standard delay before changing its operating mode. This mode change delay is implemented in accordance with SCSI standards SPI-3 and higher.

Two status lines (S/E and LVD) are provided by the SiP5668. One and only one status line is asserted HIGH when its corresponding mode has been detected; the other status line is driven low. Both status lines are driven low when HPD mode is detected.

The DISABLE pin is used to connect/disconnect the SiP5668. If it is pulled to GROUND the SiP5668 is in connect mode, and operates as a terminator. If it is pulled to TRMPWR or left open the device is in disconnect mode and presents high impedance to the SCSI bus. In disconnect mode the DIFFSENS Regulator is disabled but the mode detection circuitry continues to function and the status lines continue to indicate which mode is detected.

The SiP5668 operates within SCSI specifications with the TERMPWR voltage between 2.7 V and 5.25 V, which enables it to operate in both 5-V and 3.3-V systems. The 2.7-V lower limit guarantees correct performance in a 3.3-V system.

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